The Design of a Charge Integrating, Modified Floating Point ADC Chip

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***Abstract*— One of the challenges posed by calorimeters in high energy physics experiments is digitizing wide dynamic range charge signals at high rate to a specified precision. One response to this challenge is the development of the QIE (Charge Integrator and Encoder) concept. A QIE chip divides the input signal into multiple ranges, with each range integrating a scaled fraction of the signal. The range integrators are offset so that for any given signal magnitude, only one range will be selected as valid. The selected range integrator output is digitized to form a mantissa, and a digital code associated with that range forms an exponent. The resulting modified floating point output format gives approximately constant measurement precision over a wide dynamic range.**

Floating point converter designs are usually tailored for a specific application. A general description of the QIE shows how design parameters are chosen to suit the application. The design of a mixed signal chip that has been produced for a specific experiment is presented.

***Index Terms*—Analog-digital conversion, BiCMOS analog integrated circuits, floating-point A/D conversion, mixed analog-digital integrated circuits .**

I. INTRODUCTION

Calorimeters in high energy physics colliding beam experiments contain many channels of photo-detectors which generate fast, wide dynamic range current pulses. These signals must be integrated and digitized to record the total charge received within each beam crossing time interval. Important specifications for a digitizing readout device are sensitivity, dynamic range, and precision. Due to photostatistics, calorimeters typically have poor energy resolution at low input energy. With increasing input energy, calorimeter resolution improves until it reaches an intrinsic limit, after which it remains fixed. As a result of these characteristics, the number of bits required to span the dynamic range is significantly higher than the number of bits needed to satisfy the precision requirement. Readout electronics need only have enough precision to avoid contributing significantly to the measurement error. Simply integrating the signal and digitizing with a uniform ADC is inefficient, since the resultant steadily increasing precision with larger signals is not useful.

Efficient solutions to this problem usually involve non-uniform A/D conversion. For larger input signal amplitude, the ADC bin width is effectively increased, resulting in approximately constant precision. Different techniques exist for performing non-uniform A/D conversion, but for calorimeter applications, a multiple scaled range technique is usually used. Based on the input signal amplitude, one appropriate range output is selected and routed to a uniform ADC. The ADC output forms a mantissa, and the code of the selected range forms an exponent, resulting in a floating point output format. Several previously reported integrated circuits perform scaled ranging and are used in conjunction with a commercial ADC to provide a floating point output [1]–[2]. The QIE (Charge Integrator and Encoder) concept presented here uses scaled ranging but performs integration of the signal on ranges that are offset to be non-overlapping, which results in a more efficient use of the ADC and a modified floating point output format. The device is completely pipelined so that the charge in each beam crossing period can be integrated and digitized.

Integrated circuit designs using the QIE concept have been previously produced for different physics applications [3]. These designs used a range scaling factor of two, and used a commercial ADC to generate the mantissa. A new mixed signal chip design has been produced in a 0.8-μm BiCMOS process that incorporates a custom non-uniform (piecewise linear) ADC, yielding a completely monolithic solution. The higher range scaling factor combined with the non-uniform ADC achieves approximately constant precision while minimizing the required number of scaled ranges. Although the design is tailored for the Compact Muon Solenoid (CMS) experiment [4] at the European Organization for Nuclear Research (CERN), the design principles are general, and implementations can be varied to suit different applications.

This paper will give a simple introduction to the QIE modified floating point concept in Section II, and a general analysis of the concept for different design parameter options in Section III. Section IV covers the specifications and the selection of appropriate design parameters for the particular device that will be used in the CMS experiment. The circuit design and implementation is presented in Section V, results in Section VI, and conclusions in Section VII.

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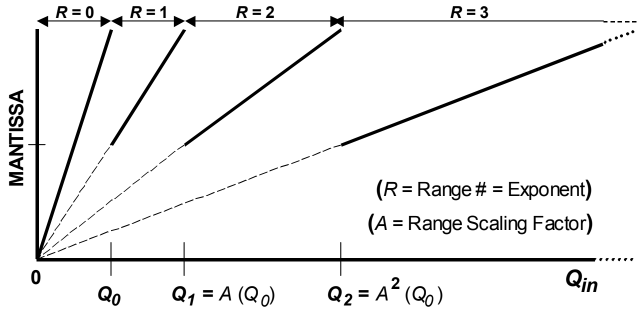

Fig. 1. Typical floating point charge transfer characteristic.

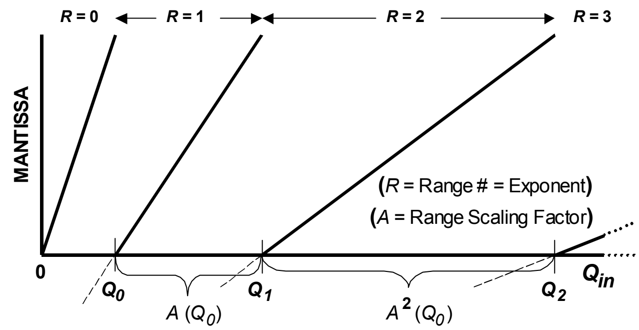

Fig. 2. QIE modified floating point charge transfer characteristic.

II. The QIE Modified Floating Point concept

In a QIE device, input current pulses are received by a front end current amplifier, which also functions as a multi-range current splitter. Each current splitter range output feeds a charge integrator, and the fractional signals are integrated on all ranges simultaneously. Current splitter output ratios and integration capacitance ratios are selected to achieve range-to-range scaling by integer factor A. For a given integrated input charge, the appropriate range output is selected and digitized by the ADC to form the mantissa, with the range code forming the exponent.

If the range integrators are not offset from each other, a standard floating point charge transfer characteristic will be obtained, as shown in Fig. 1 (ADC quantization effects are not shown). In this case, all ranges intersect at the origin, so that any range $R > 0$ uses only a portion of the ADC span.

However, in the QIE scheme, the integrators are appropriately biased so that each range has an associated offset, resulting in a more efficient "modified floating point" output format in which each range utilizes the full ADC span. A QIE charge transfer characteristic is shown in Figure 2 with $A = 2$. In general, the range scaling factor A is a design parameter to be optimized based on the specifications of the application.

III. Analysis

A. General Analysis

The principal objective of the QIE scheme is to provide approximately constant precision over a wide input range. For physics calorimeter applications, the most important specifications are the relative quantization error e_{qr} (the rms charge binning error of the ADC divided by the input charge Q_{in}) and the dynamic range. In general, for a given range scaling factor A, the specified maximum relative error $e_{qr\max}$ determines the required number of ADC bits N. Once N is fixed, the required number of scaled ranges is determined by the dynamic range specification. The effect of the value of A on these requirements will be explored in subsequent sections.

The least count charge Q_{LSB} is defined as the input charge resulting in an output change of exactly one ADC count at the bottom of the most sensitive range, and is set by the physics requirements of the specific application. For a given Q_{LSB}, the input charge which maps to the top of this range is $Q_0 = 2^N Q_{LSB}$, where a uniform ADC with N bits is used to generate the mantissa. For the modified floating point scheme, the input charge Q_R mapped to the top of a given range R is then

$$Q_R = \sum_{x=0}^{R} A^x Q_0 = \sum_{x=0}^{R} A^x 2^N Q_{LSB} \,. \tag{1}$$

On a given range R (neglecting ADC errors), the ADC bin width is $A^R Q_{LSB}$, so the relative error e_{qr} due to the ADC binning effect is

$$e_{qr} = \frac{A^R Q_{LSB}}{\sqrt{12} Q_{in}}. \tag{2}$$

In order to find the required number of ADC bits and number of ranges, (1) can be simplified with an approximation, depending on the value of A.

B. ADC and Range Requirements With Small Scaling Factor (A = 2)

If $A = 2$ and a uniform ADC is used to digitize the mantissa, then for the higher ranges, the input charge Q_R at the top of range R can be approximated from (1) as

$$Q_R = 2^{R+N+1} Q_{LSB} \,. \tag{3}$$

and the input charge Q_{R-1} at the bottom of range R as

$$Q_{R-1} = 2^{R+N} Q_{LSB} \,. \tag{4}$$

Q_R and Q_{R-1} are a factor of two higher than would be obtained with a standard floating point scheme with no range offsets.

Across one given range, the relative error varies inversely with Q_{in}, and the maximum value of the relative error, $e_{qr\max}$, will occur at the bottom of the range. By substituting (4) in (2), the maximum relative error (on the higher ranges) is

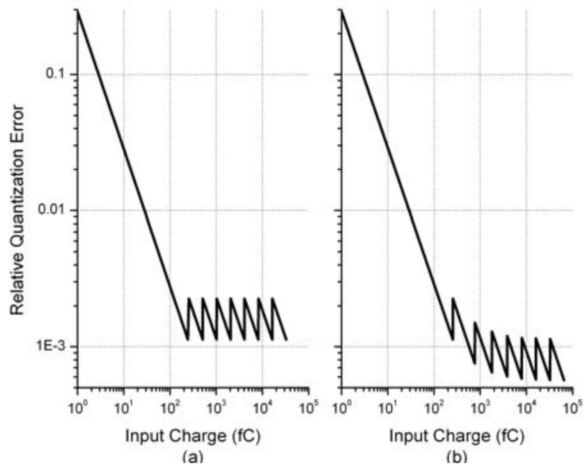

Fig. 3. Relative error plots for (a) standard and (b) modified floating point.

$$e_{qr\max} = \frac{1}{(\sqrt{12})2^N}. \tag{5}$$

The number of mantissa bits required to limit the relative error to $e_{qr\max}$ is then

$$N \geq \log_2 \frac{1}{\sqrt{12}e_{qr\max}}, \tag{6}$$

where N is the minimum required integer.

Since the first range is defined as $R = 0$, the total number of ranges is $(R_T + 1)$, where R_T is the top range. From (3), the top range required to reach a maximum input charge of Q_{MAX} is

$$R_T \geq \log_2 \frac{Q_{MAX}}{2^N Q_{LSB}} - 1, \tag{7}$$

where R_T is the minimum required integer.

Fig. 3 shows example plots of the relative quantization error with $A = 2$, $N = 8$, $Q_{LSB} = 1$ fC, and $R_T = 7$ (eight ranges), for both a standard floating point scheme and the modified floating point scheme. The error is high for small inputs on the lowest range, but decreases and then varies around an average value as the input increases and the ranges change. For both schemes, on the higher ranges, the relative error varies over a range by a factor of two, which is the range scaling factor. However, since the QIE scheme utilizes the full ADC span on each range, it achieves better precision on the higher ranges (where it is needed) and one more bit of dynamic range. Alternatively, the QIE scheme can achieve precision and dynamic range similar to that of standard floating point with one bit lower ADC resolution.

With the choice of $A = 2$, typical calorimeter readout specifications usually result in eight to ten required ranges. This results in a reasonable design configuration, as long as minimizing the number of ranges is not an important consideration.

C. ADC and Range Requirements With Large Scaling Factor (A > 2)

Minimizing the number of ranges can offer significant advantages, such as lower power consumption and fewer calibration constants (each range may require a slope and offset calibration). Also, reducing the number of current splitter elements in the input amplifier results in higher analog input bandwidth.

A larger range scaling factor can be used to reduce the number of ranges. For larger A, (1) can be approximated for a uniform ADC by assuming that the total input charge span is fully covered by the two most significant ranges. Thus the charge at the top of range R is given by

$$Q_R = (A^R + A^{R-1})Q_0 = \frac{A+1}{A} A^R 2^N Q_{LSB}, \tag{8}$$

and at the bottom of range R (top of range $R-1$),

$$Q_{R-1} = (A^{R-1} + A^{R-2})Q_0 = \frac{Q_R}{A}. \tag{9}$$

Thus from the bottom to the top of a range, the relative error e_{qr} varies by factor A, and the maximum error will occur at the bottoms of the ranges. This is given by substituting (9) in (2):

$$e_{qr\max} = \frac{A^2}{\sqrt{12}(A+1)2^N}. \tag{10}$$

The number of mantissa bits required to limit the relative error to $e_{qr\max}$ is then

$$N \geq \log_2 \frac{A^2}{\sqrt{12}(A+1)e_{qr\max}} \tag{11}$$

and the top range is

$$R_T \geq \log_A \frac{AQ_{MAX}}{(A+1)2^N Q_{LSB}}. \tag{12}$$

Larger A reduces the number of ranges, but at a cost of an increase in the number of ADC bits required to achieve a given precision. This is due to the larger variation in relative error across a range. As A increases, the precision and dynamic range performance of the modified floating point

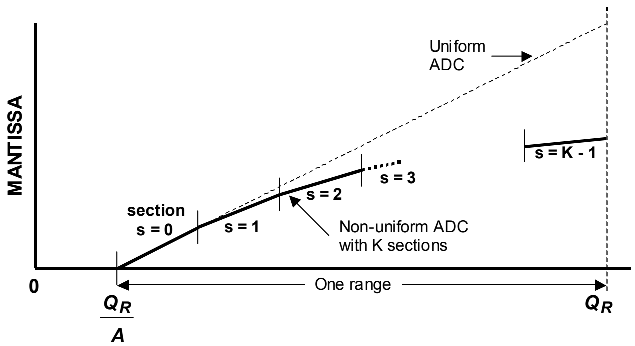

Fig. 4. Transfer characteristic with non-uniform ADC, shown on one range.

scheme approaches that of standard floating point. Using a larger range scaling factor is suited to applications that have only modest precision requirements and will benefit from minimizing the number of ranges.

The following section describes a variation of this approach that uses a non-uniform ADC to reduce the relative error variation and reduce the size of the ADC.

D. Large Range Scaling Factor With a Non-Uniform ADC

With large A, each signal range can be effectively divided into sub-ranges by using a non-uniform ADC with piecewise linear weighted bin widths, yielding the pseudo-logarithmic response shown in Figure 4. This results in a more constant precision across the range and a smaller, more efficient ADC.

With a uniform ADC, the required number of bits N is given by (11). From (9), an upper range covers an input charge from Q_R/A to Q_R, for a total charge span of $(A-1)Q_R/A$. The uniform ADC bin width is then $(A-1)Q_R/(A2^N)$. In the non-uniform approach, the ADC is divided into K sections of equal charge span, each with different bin widths from W_0 to W_{K-1}. W_0, the first section bin width, is the same as would be required with a uniform ADC. The charge span of each section is the total span of the range divided by the number of sections, or $(A-1)Q_R/KA$. To approximate a logarithmic converter, the bin widths should be such that the relative error $e_{qr\max}$ (at the bottom of each section) is equal for all sections. In other words, the ratio of bin width to input charge should be the same at the bottom of section 0 as at the bottom of section s:

$$\frac{W_0}{Q_R/A} = \frac{W_s}{(Q_R/A) + s\left(\frac{(A-1)Q_R}{KA}\right)}. \tag{13}$$

The bin width scaling to give equal $e_{qr\max}$ for each section is thus given by

$$\frac{W_s}{W_0} = 1 + \frac{s(A-1)}{K}. \tag{14}$$

The design of the ADC is simplified and more easily implemented if the bin widths are scaled by integer ratios. This can be accomplished if the constraint $K = A - 1$ is added, forcing

$$\frac{W_s}{W_0} = 1 + s. \tag{15}$$

Since each ADC section covers an equal input charge span, $B_0W_0 = B_sW_s$, where B_s is the number of bins in section s. If $K = A - 1$, the scaling of the number of bins in each section is

$$\frac{B_s}{B_0} = \frac{1}{1+s}. \tag{16}$$

Since $B_0 = 2^N/K$, the total number of bins in the non-uniform ADC is

$$B = \frac{2^N}{K}\sum_{s=1}^{K}\frac{1}{s}. \tag{17}$$

For larger K, fewer ADC bins are required. In fact, for K = 5 or greater, $B < 0.5(2^N)$, which means that the required precision can be achieved with a mantissa of $(N-1)$ bits. In general, B_s will not be an exact integer, meaning that there is some latitude in determining the exact number of bins to be used in each span. The values of W_s and B_s are critical ADC parameters that must be known when reconstructing the input charge from the digital output.

IV. Configuration of a QIE Chip for the CMS Experiment

A. Specifications

Table I gives a list of specifications for the QIE readout chip to be used by the CMS experiment. The gated charge integration time is set by the beam crossing clock, and the detector charge signals arrive synchronously at the beginning of each integration period. Two different detector systems with opposite polarity signals must be accommodated. The systems have the same dynamic range, but different least count charge requirements.

A special selectable relative calibration mode is required, only at the lower end of the ADC, which triples the sensitivity at which small input charges can be measured. This is desired in order to implement a new method of relative detector calibration. Shifts in detector characteristics due to radiation damage, etc., can be tracked over time by periodically measuring the detector response to a stable radioactive source, which can be moved in and out of the detector assembly. The detector output signal is measured directly, with no amplification, by the QIE chip. The measurement accuracy should be better than the 2% relative quantization error of the

TABLE I
SPECIFICATIONS FOR THE CMS QIE CHIP

Specification	Target Value
$e_{qr\max}$, Max. Relative Error (upper ranges)	2 %
Gated Charge Integration Period (1/[Beam Crossing Frequency])	25 ns
ADC DNL (Normal Mode, section 0)	< 0.05 LSB
Inverting Input	
Q_{LSB}, Least Count Charge (Normal Mode)	1 fC / LSB
Q_{LSB} (Calibration Mode)	0.33 fC / LSB
Q_{MAX}, Max. Input Charge	10,000 fC
Small Signal Analog Bandwidth	> 20 MHz
Input Referred rms Amplifer Equivalent Noise Charge (Cin = 30 pF)	< 0.5 fC
Non-inverting Input	
Q_{LSB}, Least Count Charge (Normal Mode)	2.7 fC / LSB
Q_{LSB} (Calibration Mode)	0.9 fC / LSB
Q_{MAX}, Max. Input Charge	27,000 fC
Small Signal Analog Bandwidth	> 40 MHz
Input Referred rms Amplifier Equivalent Noise Charge (5m, 50 ohm input cables)	< 2 fC

TABLE II
DESIGN PARAMETERS CHOSEN FOR THE CMS QIE CHIP

Parameter	Value
Range Scaling Factor (A)	5
Number of Ranges ($R_T + 1$)	4
Number of non-uniform ADC bits (N)	5
Number of non-uniform ADC sections (K)	5
Number of ADC bins, section s = 0	15
s = 1	7
s = 2	4
s = 3	3
s = 4	3

chip. However, the source amplitude is limited due to safety concerns. When applied, only a very small input charge is received from the detector each clock cycle, resulting in an ADC output shift of only a small fraction of a count. Since the charge being measured is smaller than the input amplifier noise and the QIE quantization noise, many acquisitions must be averaged in order to reduce the noise and enable accurate measurement. This method requires an ADC with very low differential non-linearity (DNL), so that the same result is always obtained, independent of the ADC pedestal. Also, the QIE response must be stable over long periods of time.

The signal inputs must be low impedance so that the input charge is collected quickly. Also, the negative input signal path to the integrator must have high enough analog bandwidth so that all of an input charge impulse is collected and integrated within one beam clock period.

B. Choice of Design Parameters

For this particular device, it is important to minimize the number of parallel input transistors in the input amplifier/splitter in order to maintain high analog signal bandwidth. This implies a small number of ranges, which in turn implies a large range scaling factor. A larger range scaling factor requires higher ADC resolution, but since the maximum relative error specification is not too stringent, the number of (uniform) ADC bits N will still be very reasonable with large A. From (11) and (12), setting the range scaling factor to $A = 5$ requires a six bit uniform ADC ($N = 6$) and four ranges. This results in a suitable number of ranges that can be practically implemented with a small number of input splitter elements. A non-uniform ADC is used in order to reduce the ADC size and obtain the required $N = 6$ bit resolution with a five bit mantissa. To achieve integer bin width scaling as in (15), with equal $e_{qr\max}$ at the bottom of each ADC section, the ADC should be divided into $K = A - 1$ sections. However, for $K = 4$, the total number of ADC bins required is slightly more than half of 2^N. Therefore, for this design, $K = 5$ is chosen so that the range can be easily covered with 2^{N-1} bins. As a minor consequence, the maximum relative errors of all the ADC sections will not be exactly equal. Table 2 summarizes the parameter choices for this particular design, along with the number of bins allocated for each section of the non-uniform ADC.

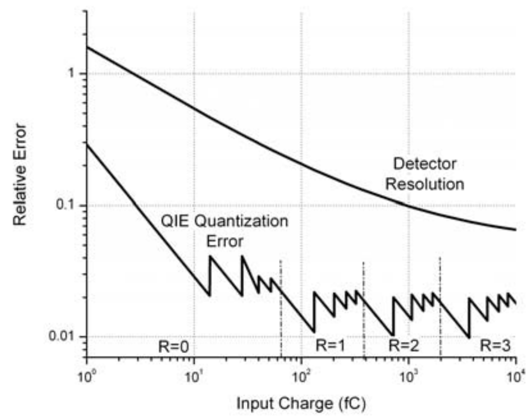

Fig. 5. Detector resolution and QIE chip quantization error

Fig. 5 shows the inherent resolution of the CMS detector for which this readout chip is designed. Also shown is the relative quantization error of the four-range chip with non-uniform ADC. The chip error contribution is always well below the detector resolution.

V. CIRCUIT DESIGN AND IMPLEMENTATION

A. Pseudo-differential Configuration

Fig. 6 is a simplified block diagram of the complete QIE ADC chip that meets the specifications presented in the previous section. The entire analog portion of the chip, from the input through the ADC, is designed pseudo-differentially.

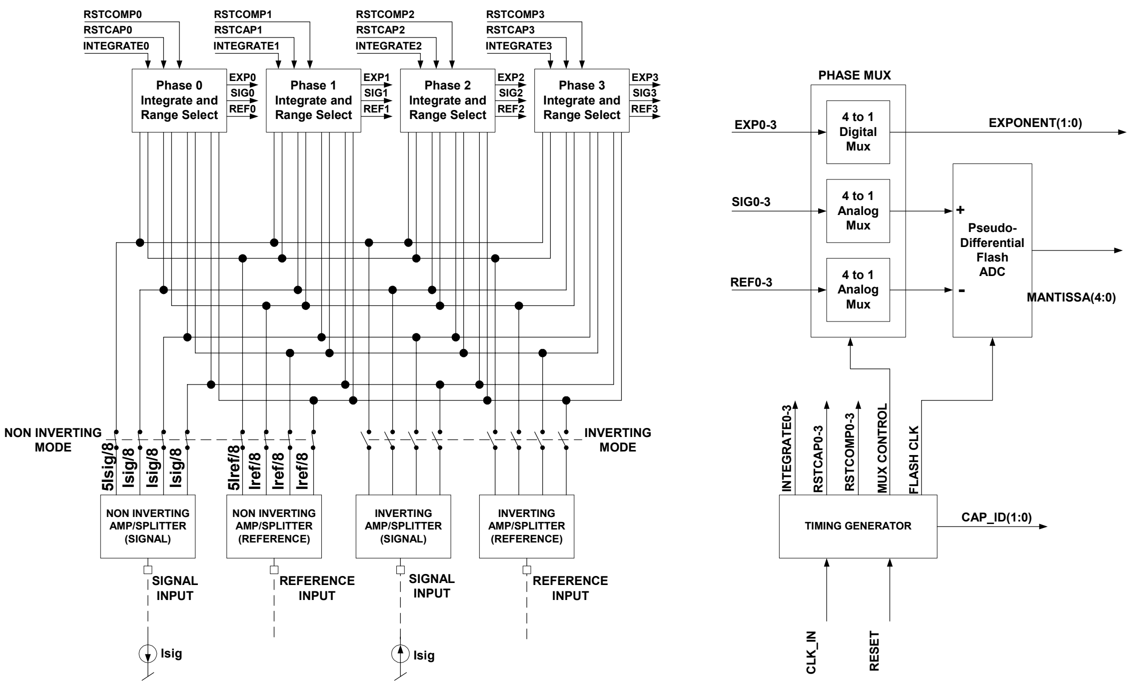

Fig. 6. Block diagram of the complete CMS QIE chip

The chip has two selectable input sections to be able to accept input signals of either polarity, in order to accommodate different types of detectors in the experiment. Fig. 6 shows the non-inverting input selected. Each input section consists of two inputs, called SIGNAL and REFERENCE. The input current pulse from the detector is connected via a cable to the SIGNAL input, and is referred to ground. The REFERENCE input serves as a dummy, but the internal circuitry and external cabling are identical for both inputs. The REFERENCE input does not collect detector signal charge, but like the SIGNAL input, it does collect charge induced by noise and unintended coupling. Both inputs feed identical integrator circuits. A pseudo-differential flash ADC then digitizes the difference between the signal and reference integrator outputs. This configuration is insensitive to shifts in bias current, temperature, power supply voltage, clock frequency, etc. In addition, external and on-chip common mode noise pickup is mostly rejected. This allows very small input signals to be accurately digitized in a mixed signal environment.

B. Input Amplifier/Splitter

A simplified diagram of each amplifier/splitter section is shown in Fig. 7. Non-inverting mode accepts negative input current and inverting mode accepts positive input current, so that the splitter outputs always supply negative currents to the subsequent circuitry. Each splitter consists of eight identical NPN transistors with paralleled B-E junctions, and the collectors are grouped with a 5:1:1:1 weighting into four outputs, one for each range. Bipolar transistors must be used in order to insure that the split ratio remains constant over a wide range of signal amplitudes. The parallel splitter elements are incorporated into a feedback amplifier in order to provide the proper bandwidth and input impedance.

In the non-inverting input amplifier, input current simply passes through the splitter elements, modified only by the

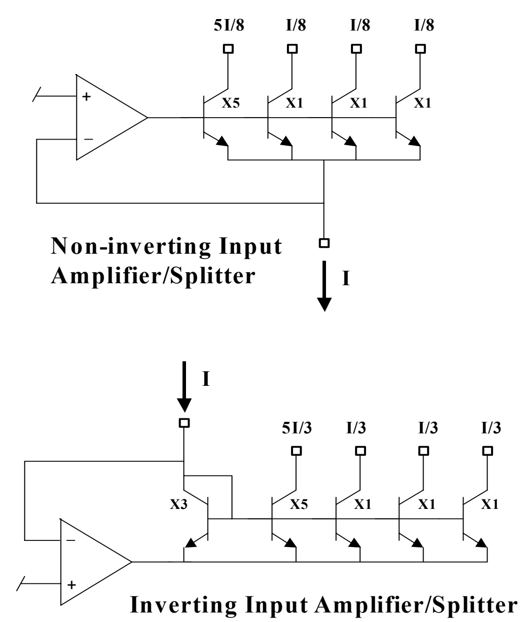

Fig. 7. Amplifier/Splitter configurations for both signal polarities

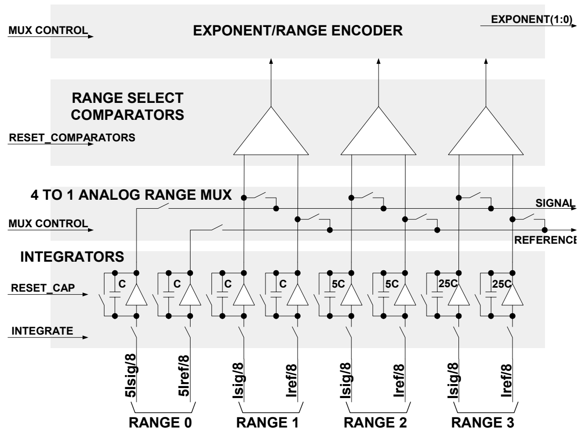

Fig. 8. Integrate and Range Select circuit

small loss due to the NPN base current. In the inverting input amplifier, the splitter is driven by a current mirror in order to invert the input current. The current ratio of the mirror is set to deliver a gain, since the inverting input for this application requires higher sensitivity than the non-inverting input.

C. *Integrate and Range Select*

The four current splitter range outputs feed an Integrate and Range Select circuit block that has four ranges of integration, as shown in Fig. 8. The least count charge sensitivity of the chip is directly proportional to the input amplifier/splitter gain, and inversely proportional to C, the integration capacitance on the lowest range. Range scaling with $A = 5$ is accomplished by a combination of 5:1:1:1 current splitter ratios and 1:1:5:25 integration capacitance ratios. Internal bias circuits generate the appropriate integrator reset offsets, resulting in non-overlapping ranges as shown in Fig. 1. A signal input always results in a positive-going integrator output.

Four identical Integrate/Range Select phase blocks (0 – 3) are used to form a pipeline, so that an input signal is always gated to one of the four blocks. A given block performs each of the following four functions sequentially at the clock frequency: 1) perform gated integration by connecting the splitter outputs to the range integrators for one clock period, 2) hold the integrator outputs by disconnecting the splitter from the integrators, then select the appropriate range with the range comparators, 3) encode the range exponent and multiplex the selected range output to the ADC to initiate digitization, and 4) reset the integrators in preparation for the next gated integration.

Bias circuits offset the reset points of the signal and reference integrators of each range in such a way that the range selected for readout is the highest range in which the signal integrator output is more positive than the reference integrator output. Since there can be range-to-range variations in the scaling factor A, and other circuit non-idealities, some range overlap is built in to avoid missing codes at the range transitions. The output pedestal can be adjusted with a simple DAC which modifies the difference between the signal and reference integrator reset points on range 0.

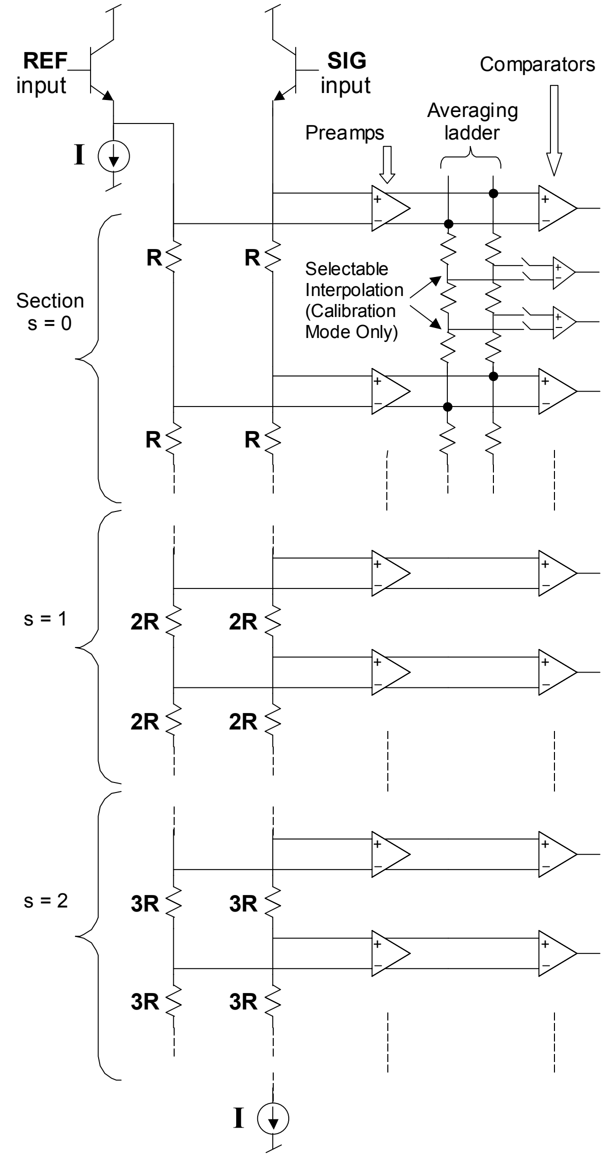

Fig. 9. Pseudo-differential non-uniform flash ADC

D. *Non-uniform Pseudo-differential ADC*

The speed and resolution requirements of the ADC suggest a flash architecture as the best approach. A differential flash architecture [5]-[6] is easily modified to be pseudo-differential, and sections with different bin widths can easily be implemented. Fig. 9 is a simplified diagram of the ADC. The ladders are driven by matched emitter followers, which serve as buffers from the multiplexed integrator outputs to the ADC. Since an input signal to the chip always results in the ADC SIG input moving positive with respect to the REF input, the comparators can all be referenced to the REF follower output, resulting in a pseudo-differential configuration. The REF ladder is necessary only to cancel bias current effects. As in (15), the integer scaled bin widths of the different sections are realized simply by grouping the appropriate integer number of unit ladder resistors. Preamps are used to drive the comparators in order to present a constant load to the ladders, and to effectively reduce the comparator offsets.

The special calibration mode of the chip requires higher resolution and very low DNL. The DNL is much improved by the use of an averaging ladder [7]. In addition, the averaging ladder is easily segmented to allow interpolation, tripling the resolution in the desired region. Since the calibration method uses only very small input signals, the averaging ladder with interpolation is added only on the lowest section of the ADC. In calibration mode, only the lowest section comparator outputs are encoded to form the mantissa.

E. Timing Generator

A timing generator provides all the necessary digital signals to control the clocking of all the phase blocks and the ADC. A digital Cap ID output code identifies which of the four integration capacitors, or pipelined phases, is associated with the mantissa and exponent. The digital output is delayed from the input pulse by four clock periods.

F. Layout

A microphotograph of the chip is shown in Fig. 10, with major layout sections labeled. Since this is a sensitive mixed signal design, the digital outputs are low level differential. For maximum isolation, the digital outputs are along the top edge, the analog inputs along the bottom edge, analog supply and bias pins on the left edge, and digital supply and control pins on the right edge. The substrates of the digital and input amplifier/splitter sections are resistively isolated by biased collector implants encircling each section. Separate local substrate connections are used in each section for independent referencing to the external ground. An on-chip bypass capacitor is added across the digital power supply to reduce high frequency digital transients.

VI. Results

A production run for the CMS experiment of more than 20,000 QIE chips has been received. The chips have been packaged and tested, with a yield of better than 80%. The least count charge sensitivity is within 10% of the target value on all wafers.

Due to random NPN transistor mismatches in the input amplifier/splitter, the range scaling factors can differ from nominal by up to 5% (typical is 2% or less). Transfer characteristic slope and offset calibration constants are thus required for each of the four ranges. The pedestals, or offsets, of each of the four pipelined phases match to better than ½ LSB, and the slopes of the phases match at the 0.2% level.

At the low end of the ADC (section 0), where the averaging ladder is implemented, the DNL is 0.05 LSB (in the normal mode). The chip will function at well above the nominal 40 MHz clock frequency. However, at higher frequencies, the DNL begins to degrade, and above 75 MHz, the ADC begins

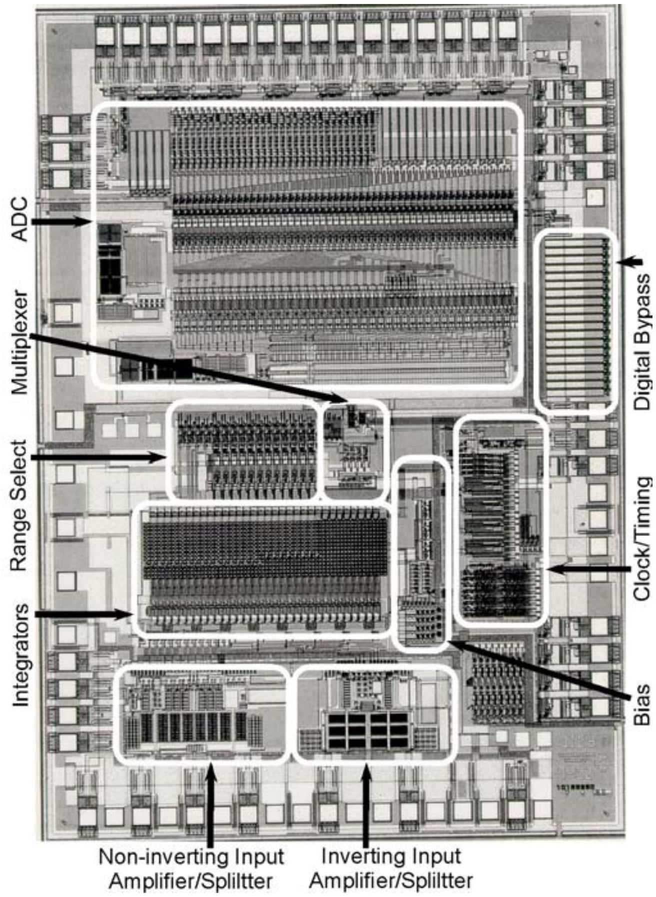

Fig. 10. Chip microphotograph

to miss codes.

The input referred amplifier noise specifications in Table I are met at the required bandwidths, with one exception. The non-inverting input noise is measured at 2.3 fC, slightly higher than expected. However, on an earlier prototype run with the same input amplifier design, the same measurement yielded a noise of less than 2 fC. It is believed that this is due to a process variation in run-to-run noise characteristics. Reducing the bandwidth with a simple bias adjustment lowers the effective amplifier noise, if desired.

If proper attention is not given to printed circuit board layout techniques, ground referencing, and power supply bypassing, coupling from both on- and off-chip digital sources increases the noise and results in a non-Gaussian output data distribution. With good techniques, output data are fit very well with a Gaussian distribution, indicating insignificant coupling. One power supply can be utilized for both analog and digital power rails on the QIE without compromising the performance. The power dissipation is 330 mW with a 5 volt supply.

The QIE response is stable with temperature, due to the pseudo-differential configuration. For an increase in ambient temperature of approximately 40C (much larger than the expected variation in the CMS experiment), the output pedestal for each phase changes by 0.1 counts or less. The

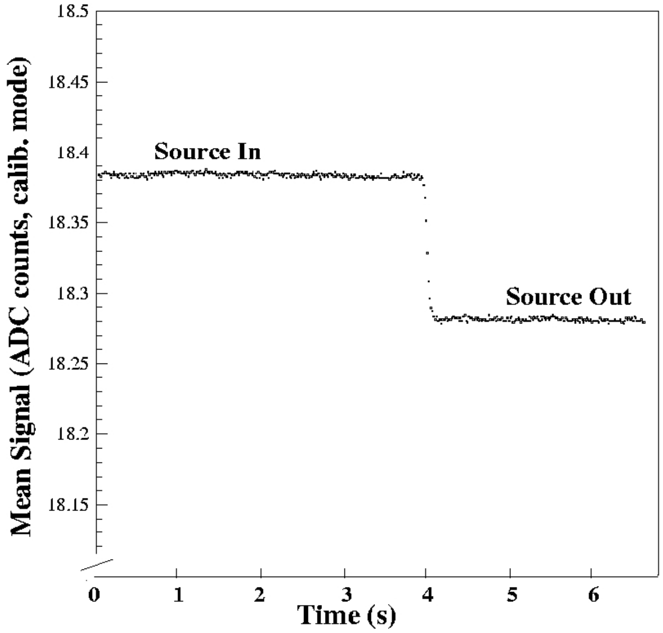

Fig. 11. Relative detector calibration test with a radioactive source.

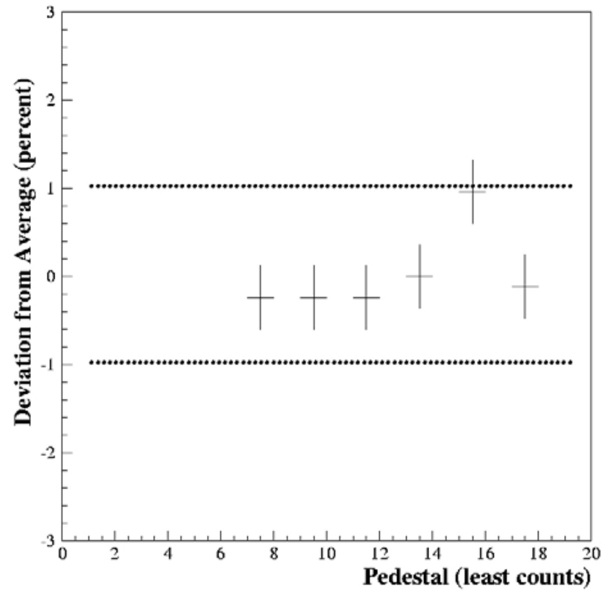

Fig. 13. Source measurement deviation with ADC pedestal.

transfer characteristic slopes change by less than 1%.

The stability of the QIE chip is demonstrated by the results of the relative detector calibration method tests, performed using a prototype detector assembly. A signal is provided by a small moveable radioactive signal source with a stable mean amplitude and Poisson distribution. A scintillator converts the radiation to light, which is fed to a photo-detector via optical fiber. A QIE chip is used to integrate and digitize the charge generated by the photo-detector in each clock period. For the relative calibration tests, the chip was clocked at 35 MHz, giving a signal integration time of 28.6 ns. Calibration mode was selected, giving a least count charge of 0.33 fC, with an arbitrary ADC pedestal of approximately 18 counts. The QIE output noise due to the input amplifier/splitter has a distribution significantly wider than the ADC bin width in calibration mode. By averaging a large number of acquisitions, a measurement error much lower than the ADC quantization error is achieved. To show that a precision amplitude measurement can be made on a small integrated charge from the detector that is significantly smaller than Q_{LSB}, many QIE data points were collected. Each data point consists of approximately 500,000 output acquisitions collected in about 14 ms and averaged to obtain the mean. A stream of 500 data points, taken over 7 seconds, is plotted in Fig. 11. Data collection was started with the source inserted, and then several seconds later the source was extracted swiftly by hand. The data show a resultant shift of 0.0862 ADC counts (in calibration mode), which is 0.028 fC, or 180 electrons. Since this is the charge integrated in 28.6 ns, the average input signal current from the source is 1 nA.

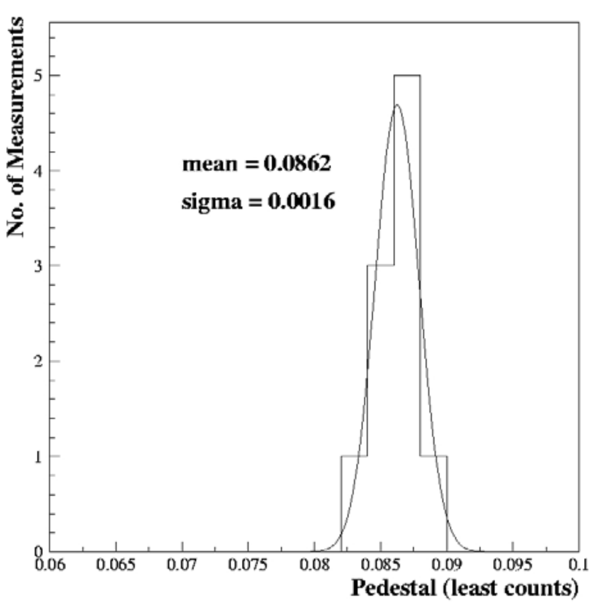

Fig. 12. Relative detector calibration stability over one month.

Fig. 12 is a histogram of this measurement result when repeated on four different days spread over a one month period. The source amplitude measurements agree to better than 2%, which is less than 4 electrons in the 28.6 ns integration time. This variation is believed to be dominated by mechanical alignment of the detector apparatus, since much smaller variations (< 1%) were observed over the time scale of several hours when mechanical disturbance was kept to a minimum.

Non-zero DNL errors in the ADC will cause the source measurement result to vary with the ADC pedestal, affecting the obtainable accuracy. This is investigated by repeating the measurement shown in Fig. 11 for different ADC pedestals. Fig. 13 shows the deviation in percent from the average measurement result as a function of the ADC pedestal on one chip (in calibration mode). The data points do not deviate by more than 1% of the source signal. The ADC performance is adequate to achieve measurement of this source to a desired accuracy of better than 2%.

VII. Conclusion

A general analysis of a modified floating point architecture for wide range, charge integrating ADCs has been presented. The architecture can be tailored to meet the specifications of a variety of different applications. The design of a single chip solution specifically for the CMS experiment at CERN is presented as an example. Test results show that very small input charges can be reliably digitized in a mixed signal environment.

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