

JLAB LLRF 3.0 DEVELOPMENT AND TESTS*

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Abstract

The JLAB LLRF 3.0 system is being developed to replace legacy LLRF systems in the CEBAF accelerator. The new design builds upon 25 years of design and operational RF control experience (digital and analog), and our recent collaboration in the design of the LCLSII LLRF system. The new cavity control algorithm is a fully functional phase and amplitude locked Self Excited Loop (SEL). This paper discusses the progress of the LLRF 3.0 hardware design, FPGA firmware development, User Datagram Protocol (UDP) operation, and recent system tests on the CEBAF Booster cryomodule without and with a beam.

INTRODUCTION

The CEBAF Accelerator at Jefferson Lab provides electron beams to four different physics (experimental) halls at energies up to 12 GeV. This is accomplished using two linacs with over 400 superconducting cavities (SC) in 53 cryomodules. The linacs are connected with recirculating arcs. Three of the experimental halls can receive up to five passes and a fourth can receive 5.5 passes [1]. The overall delivered dp/p rms. energy spread is 5×10^{-5} at currents up to 400 uA (cw).

As part of the CEBAF improvement plan, a new modified cryomodule, C75, has been developed using an existing older cryomodule [2]. The new cryomodule cavity's Q_{ext} is 1.5×10^7 and has a Q_0 of 8×10^9 . Average cavity gradient for C75 cavities is approximately 16 MV/m. In addition to the cryomodule upgrade, the plan calls for upgrading the RF zones with new LLRF systems (LLRF 3.0), which will replace the old analog LLRF (LLRF 1.0) designed in late 1980s. Every cavity is powered and controlled individually similar to the older RF systems. The cavity amplitude and phase field stability remains unchanged and must be smaller than 0.04% and 0.5 deg rms. respectively, for measured frequencies > 1 Hz.

LLRF 3.0 DESCRIPTION

The new LLRF system design builds upon experience from the older CEBAF LLRF designs, and the recent participation in the LCLS-II LLRF design. The system utilizes a modular architecture concept, where the RF receiver, RF transmitter, fast digitizer and the FPGA carrier are separate printed circuit boards.

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RF Transceiver

There are three high frequency receiver channels (1497 MHz) and one high frequency transmitter channel (1497 MHz). The RF receiver and transmitter use heterodyning in a double balanced, level 13 frequency mixer. The RF receiver channels are designed to provide very high channel to channel isolation (>90 dB). The RF receiver board generates a 70 MHz IF (intermediate frequency) signal that is sent to the fast Digitizer ADC inputs. The RF transmitter board uses 70 MHz IF signal from the Digitizer DAC output to generate 1497 MHz signal.

The RF receiver and transmitter are in the same chassis as the digitizer and FPGA carrier. This was done to keep the cost low and allow the new system to fit into the existing racks. The down side of this is, an added crosstalk of 6 dB to the receivers from the transmitter, which is still within the LLRF requirement of 80 dB. The overall RF receiver noise figure is 30 dB with an additive phase noise contribution of 0.05 deg.

Fast Digitizer and FPGA Board

Digitizer has four inputs to the ADC, two DAC outputs and a clock generator. AD9653 is used for ADC to process the 70 MHz inputs from RF receivers, DAC9781 for the DAC to generate the 70 MHz for RF transmitter and LMK03328 for the clock generator. Input to the clock generator is 70 MHz master reference. LMK03328 generates 93 MHz for ADC clock and 186 MHz for DAC clock. These frequencies are programmable as LMK03328 has two independent PLLs. Digitizer is an LPC (low pin count) FMC Mezzanine card and can be used with any FMC carrier card.

FPGA board is designed based on Intel Cyclone 10GX 672 pin FPGA. This board uses a MAX10 FPGA for power sequencing and monitoring. This board is a dual LPC FMC carrier. This FPGA is available in four different sizes for resources (85k Logic Elements, 105k, 150k and 220k). This board is compatible with three of the four mentioned models (105k, 150k, and 220k). It is flexible in this sense that user can choose one of the three options at the time of assembly without changing the design. Cyclone 10GX FPGA has ten high speed transceivers. Eight out of the ten transceivers are routed to 2xQSFP (Quad small form-factor pluggable transceiver) connectors. Other two channels are routed to 1xSFP and Marvell gigabit Ethernet PHY. This PHY can be accessed using RJ-45. This board also has 2x40 pin GPIO connectors and 2 Pmod connectors for general purpose use and expanding the functionality. FPGA board can be connected to a server using the SFP module or RJ-45 for communication over Ethernet. QSFP modules

are useful, if there is a need to exchange information between the boards at high speed (eg. 2.5 Gbps).

Chassis Design

All components are placed on a thick aluminum plate (Fig. 1) in order to provide adequate thermal cooling. Air flow is induced below the plate using a small “PC” chassis fan. In addition, the system has a diagnostic board (slow ADC, DAC, TTL I/O etc.). The chassis is powered using external DC power supply to limit the power supply induced noise.

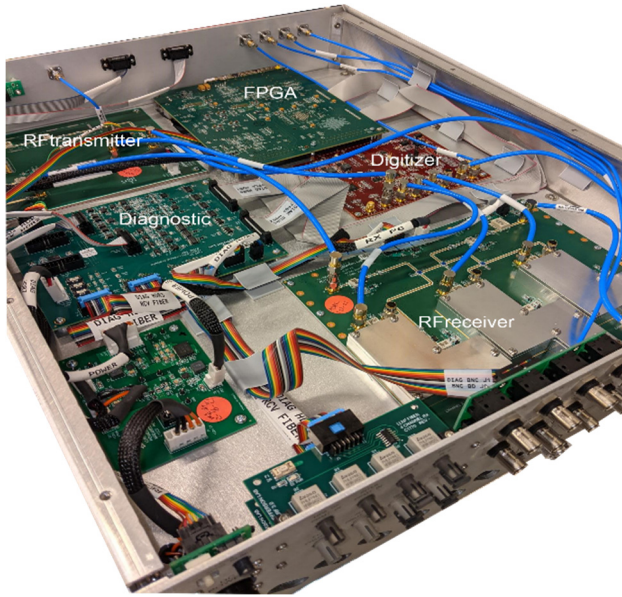


Figure 1: Filed Control Chassis.

Figure 2 shows the block diagram of the single RF Station powering and controlling one cavity. RF chassis communicates with an IOC using UDP protocol. RF chassis in a zone (8) are connected to an IOC over a private network. All the chassis can transfer the data at 1 Gbps as the link between the server and the switch is 10 Gbps.

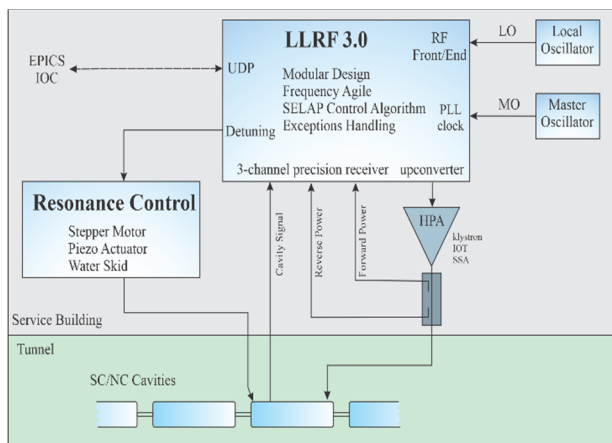


Figure 2: RF Station overview.

Control Algorithm

The control algorithm is based on digital Self Excited Loop concept [3-5] and extended by an amplitude and Phase Lock feature. This replaces an analog GDR (Generator Driven Resonator) based systems (LLRF 1.0 and LLRF 2.0). To distinguish this from GDR topology we use name SELAP (SEL with amplitude and phase locked). Figure 3 shows block diagram of this algorithm, first developed for LCLS-II LLRF project [3]. In JLAB we developed full (cavity + SELAP controller) Matlab model to better understand dynamical behavior of this topology, followed by VHDL firmware.

As one can see when the magnitude PI controller output is constant and the phase PI controller equals 0, the system is in free running SEL mode. Applying magnitude feedback, the amplitude is locked (stabilized), although system is still in SEL mode. This mode (called SELA) helps with compensating small amplitude modulation caused by SEL mode imperfections.

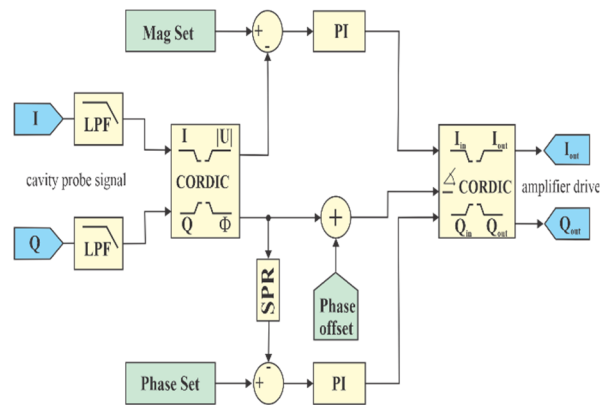


Figure 3: Locked Amplitude and Phase (SELAP) concept.

Once the phase loop is closed (SELAP), the system will compensate any cavity detuning by adding an offset vector (Q in in the Fig. 3). In practice, the system remains in full SELAP mode as long as it has enough RF power. If the system clips/saturates the RF power, it falls back and runs in SELA mode. Once detuning lessens below power saturation (Resonance Control action), the system seamlessly locks back to SELAP. Cavity phase information, depending on the status of phase lock, needs to be processed by so called Stateful Phase Resolver (SPR) [6]. The SPR output is equal to $\pm\pi$ when the phase is spinning counter clockwise, counterclockwise or follows the cavity phase when sufficient RF power is available.

UITF TESTING

Before installing the new LLRF system in the CEBAF accelerator, it was tested on a cryomodule in the Upgrade Injector Test Facility (UITF) [7]. The system was tested on a 7-cell SC (Superconducting) cavity with external Q of 9×10^6 ($1/2$ bandwidth = 78 Hz). The most anticipated part of the test was to run cavity in SELAP mode and observe the transition while the tuner is changing the tune of the cavity from -70 Hz to +70 Hz.

During simulation (Fig. 4), the narrow region in the middle of the graph reveals enough RF amplifier power to fully lock the cavity phase. When detuning rises again, forward power grows until it loses phase lock and the system reverts to SELA operation. The UITF tests verified the behavior seen in simulation.

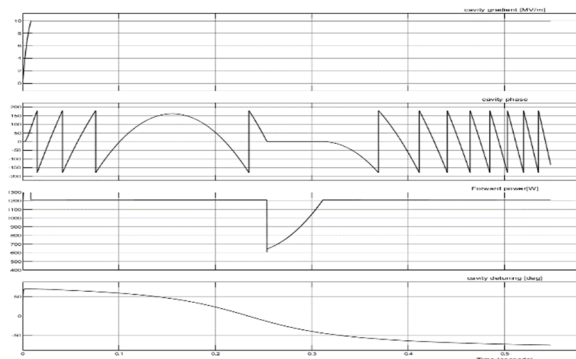


Figure 4: SELAP operation.

Cavity field regulation was measured using third party instrumentation and includes the LO (Local Oscillator) noise, which is typically subtracted from results presented in many other papers.

Operating with microphonic background detuning of 6°RMS (or 8 Hz RMS), cavity field stability was better than 0.15° in phase (Fig. 5) and 0.01% in amplitude (Fig. 6). These two values exceed the CEBAF accelerator requirements (0.5° , 0.04%). As one can see in Fig. 5, fundamental mode $6/7\pi$ is present. We did not apply any additional, digital filtering (notch) because of the sufficient isolation ($> 70\text{ dBc}$) from that mode.

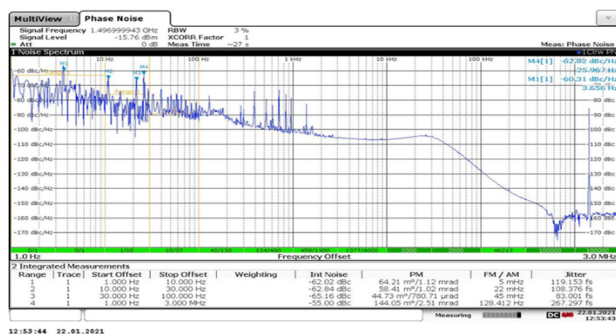


Figure 5: Cavity field phase noise [SELAP].

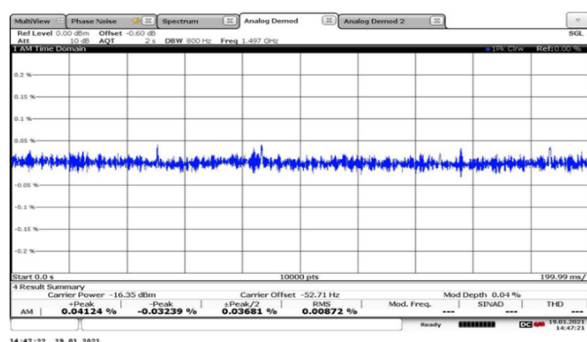


Figure 6: Cavity amplitude [SELAP].

CONCLUSION

The new design builds upon our own experience as well as our collaboration on LCLS-II LLRF project. The modular architecture can easily accommodate new operational frequencies as needed in CEBAF. The upgraded firmware greatly improves superconducting cavity operability. Recovery from an RF trip is instant (once conditions causing trip have been resolved) and does not require any human interaction. We anticipate this feature will reduce the CEBAF RF trip recovery time by a factor six to eight. The LLRF system was successfully tested on an SC cavity with beam, where it surpassed cavity field control requirements.

ACKNOWLEDGEMENTS

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