

Verification of digital integrated circuits taking into account pad models

N.N. Nevirkovets¹, N.M. Chernetskaya², D.V. Kostygov³, Y.V. Belyaev⁴, and A.A. Mikhteeva⁵

¹ PhD student, Engineer, State Research Center of Russian Federation Concern CSRI Elektropribor, JSC, Electrotechnical University “LETI”, Saint-Petersburg, Russia

² Student, Engineer, SRC of Russian Federation Concern CSRI Elektropribor, JSC, Electrotechnical University “LETI”

³ PhD student, Researcher, SRC of Russian Federation Concern CSRI Elektropribor, JSC

⁴ PhD, Head of Department, SRC of Russian Federation Concern CSRI Elektropribor, JSC

⁵ PhD student, Researcher, SRC of Russian Federation Concern CSRI Elektropribor, ITMO University

E-mail: designcenter.spb@mail.ru

Abstract. The digital integrated circuit is the main part of different sensors. It performs signal processing, controlling of a system and provides interface with external devices. Timing analysis is a basic verification method of digital integrated circuits. A new technique of digital blocks timing analysis taking into account the models of contact pads is proposed. The results of the I2C interface unit development using the proposed technique are presented.

Introduction

Miniaturization and increasing requirements for electronic devices facilitate the development of integrated technologies, which put in the forefront a problem of improving the reliability of integrated circuits (IC) at the stage of their design. To obtain an IC satisfying the technical requirements, it is necessary to perform a number of launches at the factory, which makes the IC development more expensive. To reduce the number of iterations of manufacture and to accelerate the product launch, it is necessary to minimize risks of errors at design stages. That requires adding extra checks of the IC blocks and increases the time spent on verification.

Integrated circuits are used in the sensors that are part of the inertial measurement modules used in integrated navigation systems [1]. In these systems the IC performs functions for processing data coming from sensitive elements and it also provides interaction with external devices.

Interface blocks are the most important modules in digital ICs. These blocks provide data transfer between the IC and other devices, which is why it is crucial for high quality ICs to exclude functional and timing errors induced by interface blocks.

To reduce the probability of errors, various verification methods are used at different design stages; the methods of verification include static and dynamic timing analysis techniques [2]. The basis of static timing analysis in modern automated design systems is the algorithm for traversing an oriented weighted graph [3] corresponding to some part of the combination synchronous circuit, which allows determining the critical paths of the combinational circuit. The goal of static time analysis is to find the shortest and the longest paths of signal propagation from inputs to outputs of the circuit. The result of the analysis is a set of critical paths of the combinational circuit.

Dynamic methods of timing analysis are based on simulation of the circuit operation and are carried out at each stage of the traditional design flow of digital IC blocks [4]. Existing methods of timing analysis do not consider changes in timing characteristics of digital IC blocks when they interact with IC chip contact pads. This paper proposes a verification technique of digital blocks that takes into account the pads models.

1. The digital IC blocks analysis technique taking into account the influence of contact pads

The proposed technique consists of the following stages:

- 1) developing the topology of digital blocks;
- 2) developing a test environment for modeling with contact pads;
- 3) calculating parasitic parameters of digital blocks;
- 4) adding contact pads and extra analog elements.

Fig. 1 shows the traditional design flow for digital integrated circuits with additional verification steps in red square. These steps allow a deeper analysis of the behavior of signals in digital circuits.

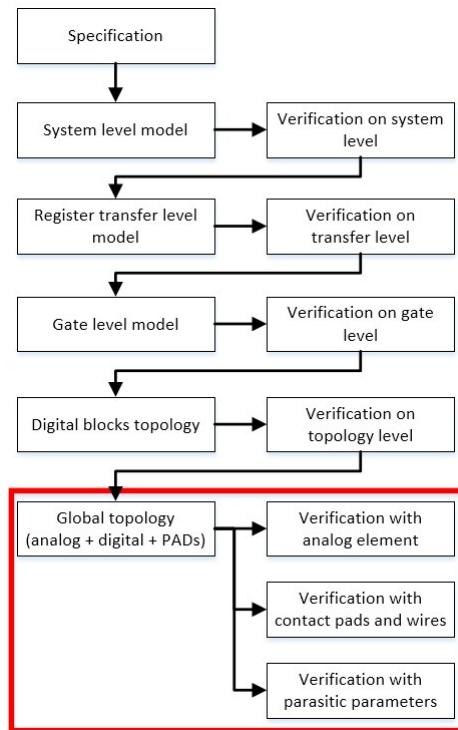


Fig. 1. Proposed technique of digital IC blocks timing analysis

The simulation is carried out in the Cadence Virtuoso computer-aided design system, which is usually not included in the traditional digital blocks design flow of ICs [5, 6]. Simulation in Virtuoso allows checking the behavior of the entire system, taking into account the spice models of standard cells and contact pads of the IC. In addition, this kind of simulation makes it possible to combine digital and analog IC parts and to investigate their interactions. Simulation results could lead to correct of the IC topology.

2. Designing the I-squared-C interface using the proposed methodology

The technique was used in the design of the I-squared-C (I2C) interface block, which is a part of the IC for the micromechanical inertial sensor.

The electrical circuit of test environment (Fig. 2) consists of an I2C interface module, bidirectional contact pads, resistors, and test module. The I2C interface (I3) is a bidirectional interface which uses

two open-drain lines, Serial Data Line (SDA) and Serial Clock (SCK), pulled up with resistors. To generate a high-impedance signal state, which is not recommended for use inside the IC [7], contact pads (I18, I19, I20, I21) of the AMS factory are used [8]. Resistors (R0 and R1) with a resistance of 10 kΩ are external discrete components which are connected to the lines SCK and SDA. The test module (I2) generates control signals and data to transfer to the interface and check the data coming through the interface.

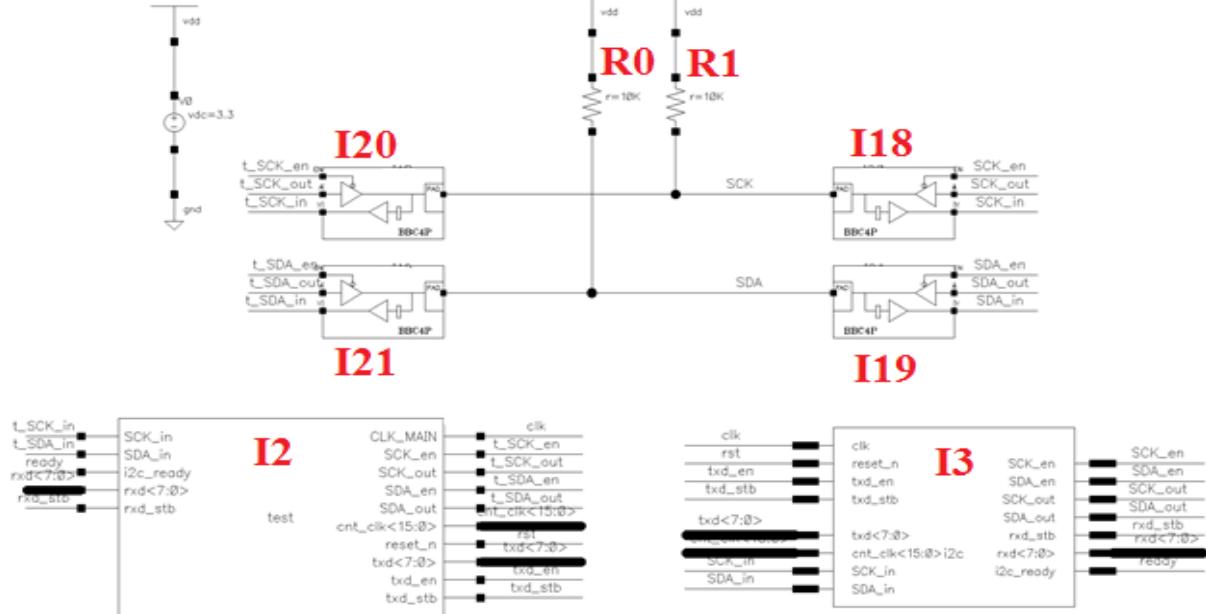


Fig. 2. Electrical circuit of I2C test environment

Fig. 3 is a timing diagram obtained during the simulation of data packet transmission for IC over I2C interface, where the transmission starts at 1.5 μs and ends at 46 μs.

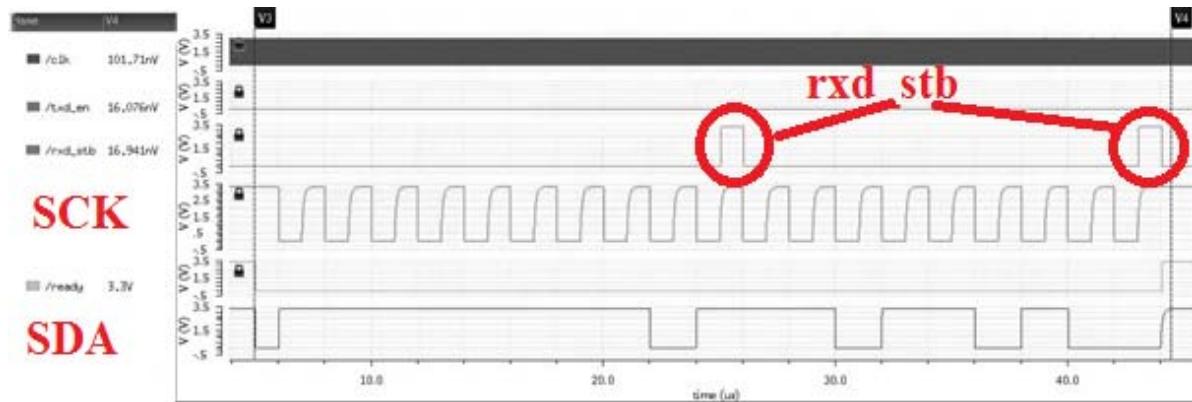


Fig. 3. The result of the simulation of data reception via the I2C interface

Fig. 3 shows that the signal rxd_stb means successful reception of transferring data by the slave device. Attention should be paid to SCK and SDA signals connected to the contact pads of the integrated circuit; the voltage on them increases gradually due pull up of the buses to the power supply through an external resistor.

The analysis of the I2C digital block during verification at transistors level has made possible to detect error in automation control unit. This error is not allowed to confirm the reception of data packet through interface.

Conclusion

The technique for analyzing the functioning of digital ICs taking into account the influence of contact areas on the time characteristics of the circuit is proposed. This technique allows detecting and then eliminating the errors which are not detected in the traditional design flow. The blocks developed according to this technique are employed as part of IC for a micromechanical inertial sensor.

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