Université Paris-Sud 11

LAL-09-117
25 sept 2009

MEMOIRE D'HABILITATION A ENCADRER DES RECHERCHES

« Front-End Electronics in calorimetry : from LHC to ILC »

Christophe de LA TAILLE

soutenu le 25 septembre 2009 devant le jury :

Pr Stavros KATSANEVAS
Dr Bruno MANSOULIÉ
Dr Veljko RADEKA : rapporteur
Dr Félix SEFKOW : rapporteur
Dr Marc WINTER : rapporteur
Dr Guy WORMSER

Laboratoire de l'Accélérateur Linéaire
Orsay Micro Electronics Groups Associated IN2P3-CNRS

REMERCIEMENTS

Je remercie tout d'abord les membres du jury : *Veljko Radeka*, *Felix Sefkow* et *Marc Winter* d'avoir accepté en plus de leurs multiples responsabilités, la charge d'être rapporteurs de ce travail. Je remercie également *Stavros Katsanévas*, *Bruno Mansoulié* et *Guy Wormser* de me faire l'honneur de faire partie du jury.

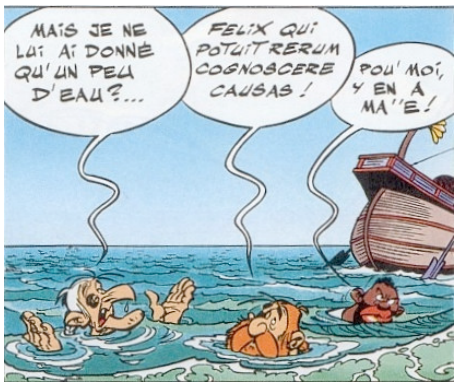
Le travail décrit couvre de nombreuses années de développement d'instrumentation, démarré sous la conduite de *Bob Chase*, *Alex. Hrisoho* et *Veljko Radeka* et je les remercie encore de leur enseignement et de leur soutien.

L'expérience ATLAS a servi de base à de nombreux développements nouveaux en calorimétrie tant les défis étaient nombreux à relever pour exploiter le formidable potentiel de découverte du LHC et construire les meilleurs détecteurs pour la meilleure physique. *Daniel Fournier* a été le père du calorimètre argon liquide « accordéon » et a toujours veillé à ce que les moindres détails soient tirés au clair pour que la performance reste optimisée. Je lui suis reconnaissant de la confiance qu'il m'a accordée pour les développements instrumentaux et les responsabilités qu'il m'a confiées dans la collaboration. Je remercie aussi *Laurent Serin* dont la rigueur et l'opiniâtreté ont permis que l'on obtienne toujours le maximum de la performance.

Le LHC démarrant tout juste après une quinzaine d'années de construction qu'il faut déjà développer la génération suivante : l'ILC et de nouveaux concepts de calorimétrie dédiée au « particle flow ». Là aussi, physique et instrumentation se complètent pour permettre les meilleurs détecteurs et j'ai beaucoup apprécié de travailler avec *Henri Videau*, *Jean-Claude Brient* et *Félix Sefkow* et la confiance mutuelle qui permet les meilleures collaborations.

Tous les développements décrits n'auraient jamais pu voir le jour sans l'aide quotidienne de *Nathalie Seguin-Moreau* et *Gisèle Martin-Chassard* qui ont depuis le début veillé à ce que rien ne soit négligé avant de passer à de nouvelles expériences et ont permis de donner corps et succès aux différents développements décrits ici.

Enfin les années passant, avec l'augmentation du nombre de projets et la complexification des ASICS, c'est toute une équipe d'une douzaine de personnes[1] qui forment le pôle de micro-électronique OMEGA et permettent la réalisation de circuits toujours plus performants dans des collaborations sympathiques. Qu'ils soient tous remerciés ici pour leur aide et leur implication dans les circuits réalisés.



Comme tente de le montrer ce rapport, la recherche est un métier formidable où l'on apprend tous les jours quelque chose de nouveau, surtout quand tout ne fonctionne pas (immédiatement) comme prévu ! « *Felix qui potuit cognosecere rerum causas* ».

∞

[1] *Pierre Barrillon, Sylvie Blin, Stéphane Callier, Selma Conforti Da Lorenzo, Frédéric Dulucq, Julien Fleury, Gisèle Martin-Chassard, Ludovic Raux, Nathalie Seguin-Moreau, Damien Thienpont, Yan Xiongbo*

INTRODUCTION

1. ATLAS and the Large Hadron Collider (LHC)

I have had the luck to start my research work on ATLAS calorimetry in 1990, when what is now the largest particle physics experiment in the world[2] (Figure 1) on the LHC was in its early phase[3] of coming from "artist views" and "conceptual drawings" to the first pieces of hardware that had to show that the calorimeter would be feasible.

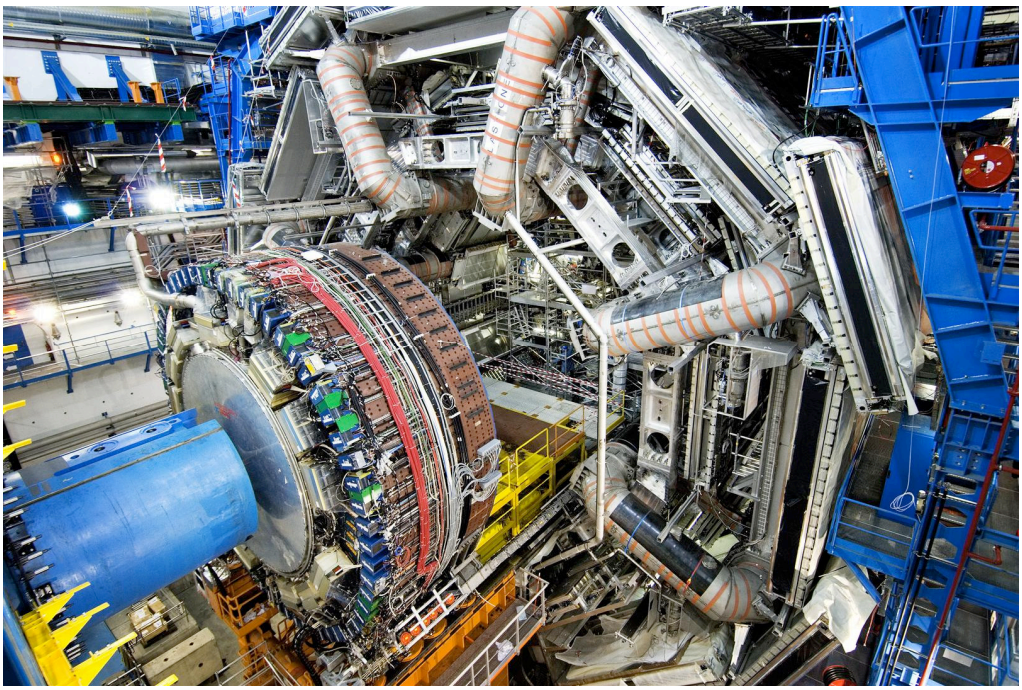


Figure 1 : view of the ATLAS experiment in 2008 at CERN, during insertion of the end-cap calorimeter (left).

The LHC (Large Hadron Collider) will be (is) the most powerful particle accelerator in the world, reaching energies of 14 TeV. It is installed in the 27 km long circular tunnel at CERN formerly used with electrons of 200 GeV for the LEP experiments which allowed detailed studies of the standard model for particle physics until its close-down in 2001. The LHC will allow to go above well above the present limits (currently set by LEP and by the US Tevatron) both in energy and luminosity and access to the last

∞

[2] ATLAS is a worldwide collaboration of 2000 physicists from 200 countries. The detector housed at CERN (Geneva) measures 20x20x60 m^3, weighs 50 000 tons and has cost 500 M€.

[3] The first talks on the LHC date from 1984, but the official R&D only started in 1990, at the Evian workshop

missing element of the standard model : the Higgs boson. But more important, it should go beyond this model and hopefully discover the first new particles predicted by new models such as super-symmetry.

As often, calorimeters were crucial detectors to exploit the physics potential of the accelerator and in particular fulfil the first goal of the LHC which is the Higgs boson discovery in the most probable mass region of 120-200 GeV. However, it required a strong R&D effort in order to handle the huge collision rate of 40MHz and the high beam energy of 14 TeV, which on top generated a high radiation environment. Moreover, the small branching ratios for the Higgs boson detection in two photons or four leptons requires a high measurement accuracy, better than 1% on the calorimetric energy.

As will be seen in all this document, electronics performance plays an important role in the detector performance and physics. In the calorimeter resolution (Figure 2) :

$$\frac{\sigma(E)}{E} = \frac{a}{E} \oplus \frac{b}{\sqrt{E}} \oplus c$$

the first term (a/E "noise term") is due to the electronics noise and the last one ("constant term") comes mostly[4] from non uniformities in the readout electronics that can be largely corrected by a good electronics calibration. This last term becomes all the more important at the LHC since the energy reached is unprecedented. The electronics performance is thus essential to obtain a good uniformity and stability energy response, as shown in Figure 2

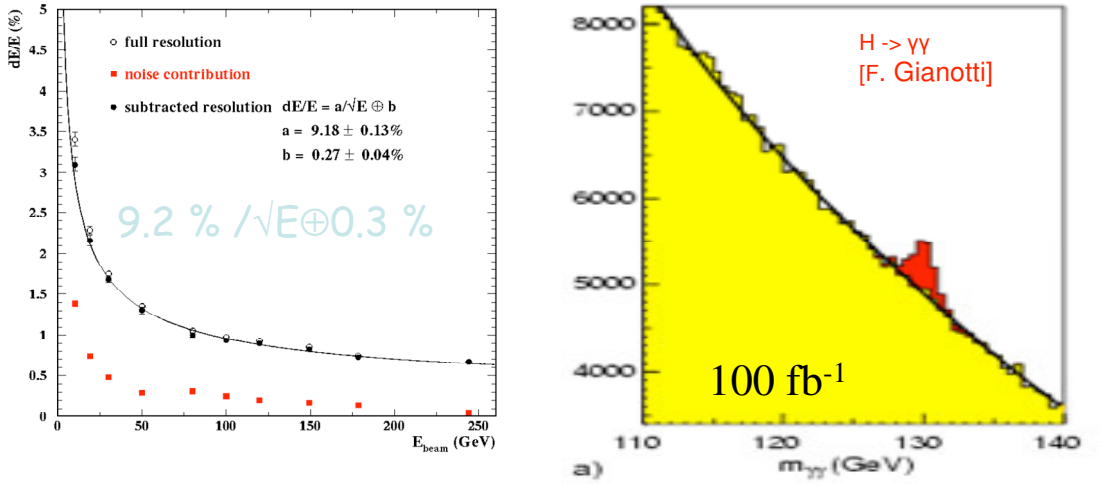


Figure 2: Left : Energy resolution as a function of energy, measured on ATLAS module 0. After quadratically subtracting the noise term coming from the electronics,, the resolution goes from the black dots to the red ones and can be fitted as 9%/E (+) 0.3%.. This small constant term is essential to get good resolution at the very high energies reached by the LHC and is also partially dependent on electronics performance. Right : signal from a Higgs decaying in 2 photons measured in the calorimeter. The signal appears in red on top of the irreducible physics background in yellow. The width of the red "spike" is determined by the calorimeter resolution, which needs to be around 1% at 100 GeV in order to resolve in from the background. (plots from [1])

For the electromagnetic calorimeter, the liquid argon technology has rapidly been chosen by the ATLAS proto-collaboration for it excellent stability, precision and uniformity. The slow speed issue had been overcome by the accordion geometry proposed by *D. Fournier* which shaped the absorbers in zigzag in order to form a projective tower while getting the signals on the front and rear face with minimal inductance[5].

I worked at the beginning on the preamplifiers and shaping. As there is no gain in liquid argon, preamplifiers are key elements for low noise performance. Several technologies were in competition among several groups (AsGa, JFET, Bipolars…) and in the end the noise performance turned out not to

∞

[4] Mostly but not only, as mechanical dispersions, dead material… also affect the constant term. The main difference with respect to electronics is that this cause of non-uniformity does not vary in time and can thus me more easily corrected

[5] It also minimized the projective cracks that bring the signals out.

be the main parameter for choice, as much as reliability, dead space and power dissipation also affected the overall performance. The performance and choice of preamplifiers will be described in Chapter 1, section 2. The shaping, essential to optimize the signal to noise ratio will be described in section 3, from a theoretical point of view and then in the practical realization of an ASIC in BiCMOS 1.2 µm AMS. After a few years of R&D, progress in analog pipelines made possible to digitize several samples on the waveform instead of the sole peak value so far used. This allowed the new technique (in our field) of digital filtering called "multiple sampling" introduced by *B. Cleland* to improve the signal to noise ratio and adapt to the changing luminosity. The first results turned out to be not as good as predicted by theory and with *L. Serin* and our PhD student *Y. Jacquier*, we tried to understand what was happening and study how close we could come to theory. This is described in section 4 of Chapter 1.

As all people working in calorimetry know, calibration is an essential feature of precision measurements over a huge number of channels. Liquid argon benefited of the reputation of being "easy to calibrate" as there is no internal gain and the cryogenic operation provides very stable temperature conditions. The main source of signal variations resides in the readout electronics which is followed and corrected by applying a known (and stable) reference electrical signal to the input. With the fast shaping, large dynamic range and high radiation levels at LHC, it turned out to be not so easy to generate 0.2% accuracy pulses over a 16 bits[6] over around 200 000 channels ! This required a long effort, which was spurred by *L. Serin* and described in Chapter 2. The pulse distribution is explained in the first section, in particular concerning the influence of the cables bringing-in the pulses. The pulse generators which need to generate signals mimicking the liquid argon pulse with an excellent precision both in amplitude and pulse shape over 16 bits are described in the second section. A first version was developed in discrete components for module 0 tests. It was subsequently moved in radiation hard custom integrated circuits as described in the third section. The performance in ATLAS environment is shown in conclusion.

In the end, an excellent electronics calibration was not enough to bring the uniformity on large modules at the 0.5% targeted level. Testbeam data showed that many effects in the signal path created non uniformities at high speed readout. It was then necessary to refine the detector modelization and simulate and then measure all the parameters coming in the model. This is the content of Chapter 3. The fisrt section studies the complete (multi-coupled) transmission line modelization and extracts a simpler RLC lumped model. It also shows how these parameters have been measured on all the 100 000 channels of the calorimeter The second section introduces the calculations of physics and calibration signals in order to correct for the bias introduced in the calibration signal (0.2%/nH) by this parasitic inductance of a few tens of nH. The third section deals entirely with crosstalk issues. In the front sampling of the calorimeter, the fine strips exhibit a capacitance to the neighbors that is of the same order than the capacitance to ground. With the fast shaping used, it gave rise to 5-10% crosstalk, which had to be modelized and corrected for. It also leads to noise correlation between channels, that could have jeopardized the fine algorithm of γ/π^0 rejection that is essential for the Higgs identification in the 2 photons mode. Finally, one part retraces the steps taken by the "crosstalk task force" of which I was in charge to bring the crosstalk everywhere in the middle and back samplings, down to below 1%, starting from sometimes much higher values. There, many unusual sources were giving crosstalk , mostly from inductive effects that showed up due to the fast shaping.

2. ILC and CALICE

The LHC had not yet started that physicists were already thinking at the next generation of experiment. In order to study in detail the Higgs boson that is to be discovered at LHC, a lepton collider has been proposed at the end of the 90's to provide clean data with an accelerator of electrons tuned on the mass to be studied. In order to avoid the prohibitive losses by synchrotron radiation, a linear accelerator is necessary and the progress of accelerating cavities, reaching 40-50 MV/m made possible an affordable machine. In 2003, the TESLA proposal described in its technical design report (TDR) how

∞

[6] The electronic calibration is also used to correct non linearity (at the 0.1% level) in the readout chain.

such machine could be built with existing technology which is also now used for free electron laser light sources.

The detectors are also very different from the LHC as the emphasis comes to measuring precisely jets in the final state. In order to improve the energy resolution on jets and also avoid mixing them, an algorithm of particle flow has been proposed around *H. Videau* and *JC Brient*, in which the various components of hadronic showers (charged and neutral) are identified and measured individually. The algorithm requires an excellent granularity in order to achieve good particle identification and separation, hence the term of "imaging calorimetry". The huge number of channels (typically 100 millions) that stems from this requirement together with the need of very compact detectors necessitate a strong and interesting R&D effort that was started in 2001 in the framework of the CALICE collaboration.

In Chapter 4, we describe the development of the readout ASICs for the three calorimeter proposals. The first section is devoted to the ECAL, with the physics prototype readout by ILCPHY3 whereas the technological prototype will be readout by SKIROC (Silicon Kalorimeter Read-Out Chip). The second section describes the development of HARDROC for the DHCAL technological prototype that is the first prototype to operate a $1m^2$ detector with 10 000 channels of embedded electronics. The third section describes the Analog HCAL composed of scintillating tiles and silicon photomultipliers. The physics prototype has been realized in 2003 and equipped with an ASIC FLCSiPM that we have developed. Work is now moving to the technological prototype readout by a chip named SPIROC (Silicon Photomultiplier Integrated Read-Out Chip)

3. Multi-anode Photomultiplier readout

The appearance at the end of the 90's of photomultipliers with segmented anode (multi-anode PMTs) of 16 to 64 pixels of a few square millimeters allowed a cheaper readout of large number of optical fibers inserted in large scintillator planes. With the large number of channels, it was also natural to try to integrate the readout electronics inside an ASIC in order to keep the cost reasonable. This was quickly adopted by the OPERA experiment for reading out its scintillating planes of the Target Tracker detector. We entered the experiment in 1998, under the leadership of *JP Repellin* to provide the readout ASIC called OPERA_ROC, that was the first ASIC developed to readout such new detectors. We chose to use a variable gain current conveyor in order to correct for the large gain dispersion in the different channels of the photomultiplier. The corrected signal would then feed discriminators to generate a trigger signal as well as a charge integrator to provide a multiplexed charge measurement. This chip is described in the first section of Chapter 5.

After the large volume production and successful operation in the Gran Sasso tunnel, the chip was interesting the ATLAS collaboration for its absolute luminosity measurements, realized with scintillating fibres at very small angle read out by the same Hamamatsu 64 channels PMT. The BiCMOS 0.8 μm technology used for OPERA_ROC was getting obsolete and the chip was moved and upgraded in the more recent 0.35 μm SiGe BiCMOS, with excellent performance. This chip called MAROC and its implementation are described in the second section.

This sophisticated and highly ibntegrated chip pushed for a further step in integrating more and more functions in a chip and on detector, leading to "smart photodetectors" with integrated electronics and digital outputs. This turned out to potentially interest the next generations of neutrino experiments, to equip huge areas of photodetection at reasonable cost and a demonstrator was funded in an ANR[7] project led by *JE Campagne* named PMm^2. A chip named PARISROC was developed and successfully tested by our PhD student *S. Conforti* and is described in the last section.

∞

[7] « Agence Nationale pour la Recherche », distributing funding on selected projects

CHAPTER 1

ATLAS FRONT-END ELECTRONICS

1. Introduction

Calorimetry at LHC required a strong R&D effort in order to handle the huge collision rate of 40 MHz and the high beam energy of 14 TeV which on top generated a high radiation environment. Moreover, the small branching ratios for the Higgs boson detection in two photons or four leptons requires a high measurement accuracy, better than 1% on the calorimetric energy [1].

For the electromagnetic calorimeter, the liquid argon technology had rapidly been chosen by the ATLAS proto-collaboration for it excellent stability, precision and uniformity. This technology had notwithstanding the reputation of being slow because of a confusion between risetime and signal duration and also because of the large parasitic inductance necessary to gang together the different layers necessary to form a tower as pointed out by a paper by *V. Radeka* in 1990 [4].

The first point has been addressed by electronics shaping and will be developed in § 3. The second was solved by the accordion geometry proposed by *D. Fournier* which shaped the absorbers in zigzag in order to form a projective tower while getting the signals on the front and rear face with minimal inductance (cf Figure 3) [2].

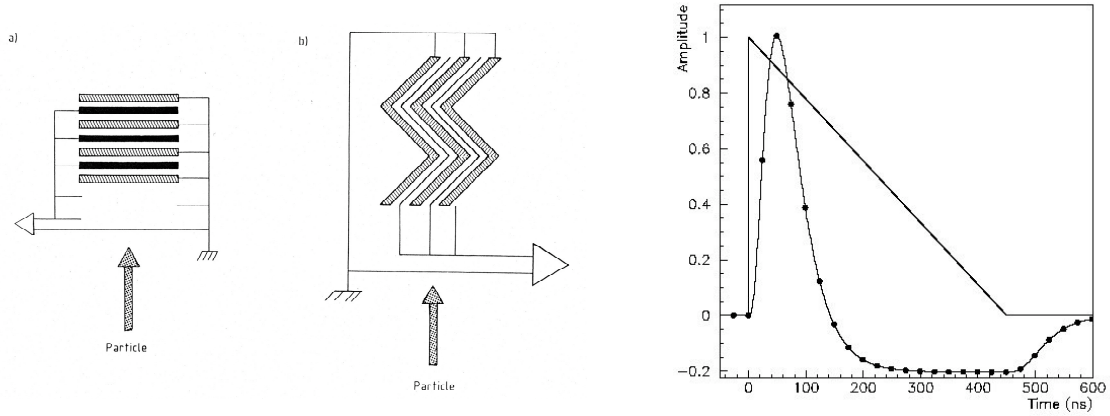


Figure 3: traditional and "accordion" absorber geometry and liquid argon pulse before and after electronics shaping

For the readout electronics, the preamplifiers received (as usual) a high attention as their noise performance determines the energy resolution at low energy. Several groups proposed competing

technologies and architectures, in particular charge or current sensitive, which will be summarized in section 2, with a particular emphasis on the ØT preamp which we proposed in Orsay and that is described in more details in § 2.3. and [5].

After the preamplifier, the signal is shaped in order to optimize the signal to noise ratio. Here, one unusual source of noise is the pileup of minimum bias events, due to the high luminosity operation which requires clipping the long decay of the liquid argon pulse (cf § 3). Conversely, reducing the electronics noise requires to cut down the bandwidth. Minimizing both noise contributions leads to an optimum shaping time which varies with the luminosity. Fortunately the introduction of multiple sampling (or digital filtering) by *B. Cleland* in 93 [6] has allowed to operate at the minimum noise in (almost) all conditions. The shaper is also used as a multi-gain amplifier in order to split the large 16 bits (10^5) dynamic range into 3 linear ranges of 12 bits. We have been in charge in Orsay to develop and produce the shaper, which was my first experience in microelectronics and is described in § 3 and [8]. The signal is then stored in an analog memory, digitized after LVL1 trigger and sent out on optical fibres to the Read Out Drivers (RODs) that process the data. The overview is shown in Figure 4.

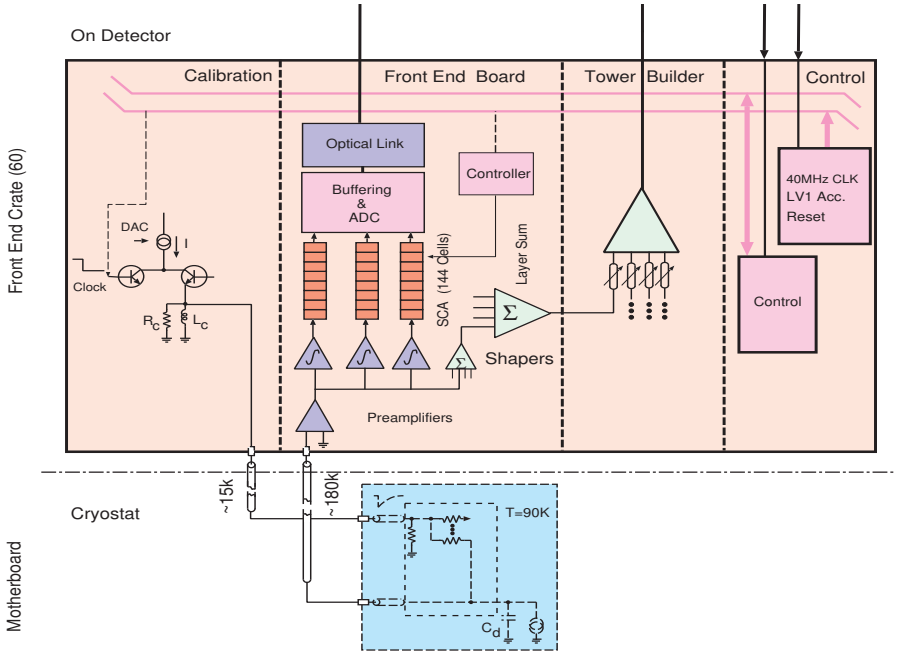


Figure 4: synoptic diagram of ATLAS LAr readout. In blue, the on-detector electronics which consists only of calibration resistors and connectors. 180 000 cables bring calorimeter signals outside of the cryostat, while ~20 000 bring the calibration signals in. On the cryostat itself, specially designed crates house front-end boards that readout the signals, calibration boards that generate the calibration pulses, tower-builder boards that perform analog sums for the LVL1 trigger and controller boards.

Several prototypes were realized to progress on the comparison of different options and validation of choices.

∞ In 1990 a small prototype was built (Figure 5) to validate the accordion concept on test beam as well as the behaviour at fast shaping. It was readout by charge preamps designed by BNL and fast shapers (30 ns) we designed at Orsay. The goal was to check that a good resolution could be obtained ($10\%/\sqrt{E}$) and in particular a local constant term of 0.3% that would prove that the corrections necessitated by the accordion geometry were accurate. The fast readout of 30 ns was essential also to prove that LAR could be *fast* and the accordion geometry was really reducing the parasitic inductance that slowed the signal. By the end of 1990, the test was a success[3] and a larger prototype could be built.

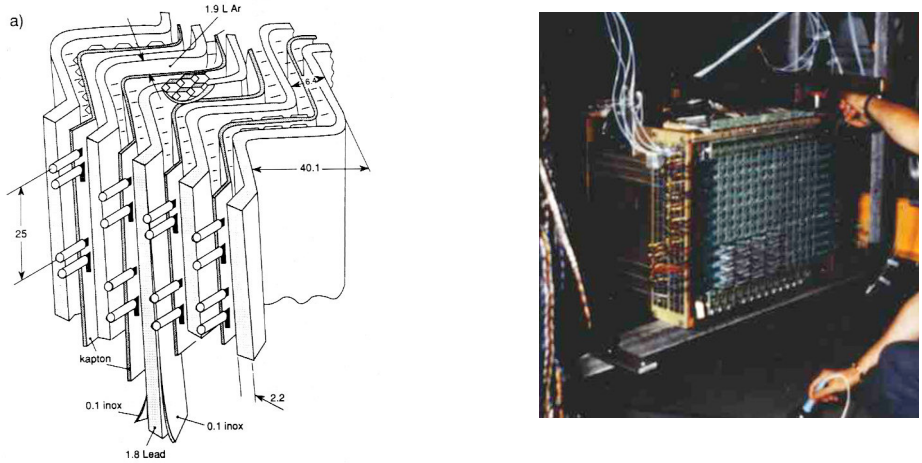


Figure 5 : Principle of accordion readout and picture of the first cubic prototype in 1990

∞ In 1991-1993 a 2 m long prototype was built by the RD3 collaboration to study the feasibility of the calorimeter in large dimensions (Figure 6). The main issues concerned of course the mechanics and the electrodes that collected the signal, but there were also many issues on electronics. As will be detailed in §2, several preamplifiers were proposed by different groups, including one by us and the tests would help for the choice. We were again in charge of developing the fast shapers, now for 3000 channels, still in the form of small hybrids, which in the end occupied a cubic meter ! The theoretical calculations on the shaping and optimum shaping time occupied us for some time as it strongly affects the noise and will be recalled in §3. After the shaper, the signal was in a first period sampled at the peak and digitized by Lecroy CAMAC ADCs and later on stored in the first prototypes of analog memories. This allowed to get several samples on the waveform and to combine them to do some digital filtering (cf § 3.3.) to approach very closely the theoretical optimal filter and improve significantly the signal to noise ratio. This approach was very new in the domain and we made several studies to convince ourselves of the strengths and weaknesses of the method which is also detailed in §3. The detector also needed an electronics calibration system to correct for non uniformities and non linearity in the readout, which will be described in Chapter 2.

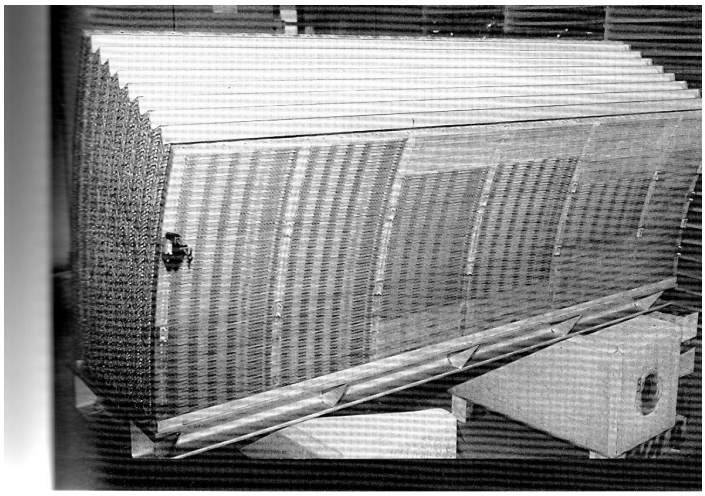


Figure 6: View of the 2 m barrel prototype

∞ From 1994 to 1996, two years were necessary to optimize by simulation and with the 2 m results the geometry and granularity. Many factors were coming in, such as physics performance, interaction with other sub-detectors, cost… The result is summarized in Figure 7 below which shows the granularity, segmentation in depth and arrangement of the electronics on the cryostat.

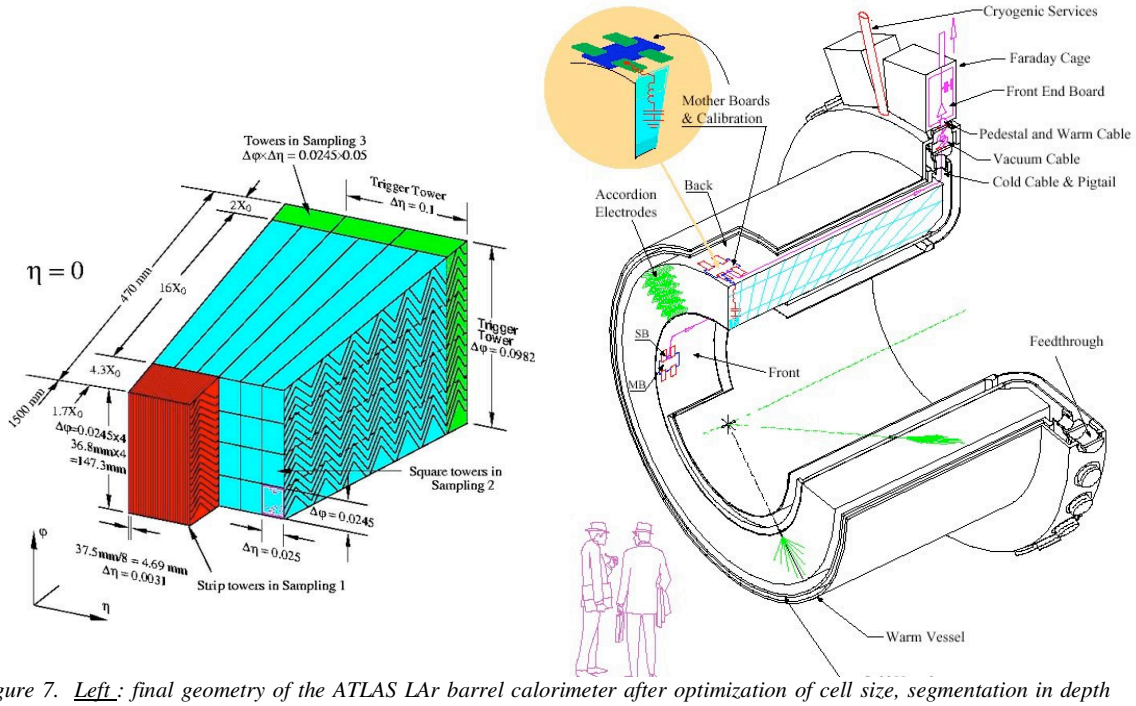


Figure 7. Left : final geometry of the ATLAS LAr barrel calorimeter after optimization of cell size, segmentation in depth and in eta-phi. The red part corresponds to the front finely segmented strips, the blue to the middle cells where most of the electromagnetic shower is contained and the green to the back compartment used at high energy. Right : overall view of half-barrel calorimeter with the feedthroughs at the end to bring-out the signals.

* In 1997 it was now time to build a real module 0, as shown in Figure 8. It did not look very different from the 2 m prototype (3 m instead of 2), but bore in fact several key differences in the signal path that would necessitate long efforts in analysis, as will be detailed in chapter 3. In particular, the crosstalk was severely deteriorated. By that time, the final electronic architecture could be tested with radiation soft components. In 1999 the first module 0 was ready with its electronics to go into test beam.

The module 0 was used to take testbeam data during several years and many important analysis results were obtained, not always without effort ! As an example, the calorimeter uniformity is shown in Figure 9.

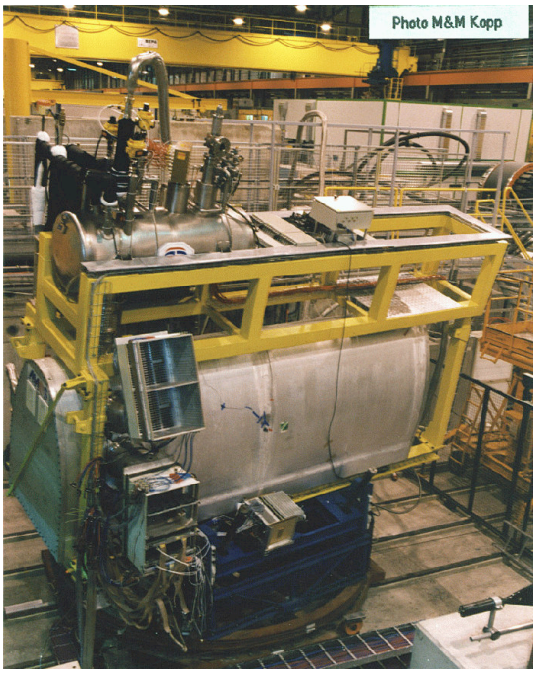


Figure 8 : module 0 in testbeam at CERN in 1999 in its dedicated cryostat.

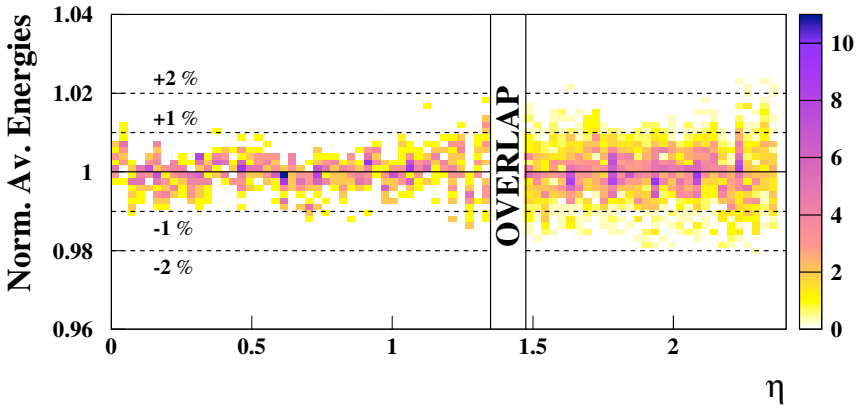


Figure 9: normalized energy response over the full calorimeter. The rms is 0.6% over morea than 2 000 channels .

From 1998 to 2001 radiation hard components were developed and qualified in DMILL BiCMOS 0.8 µm, a military process developed by CEA. My group in Orsay had the responsibility of the shaper chips (80 000), three calibration ASICs and the calibration boards. We also had to organize the multi-chip production runs in DMILL and the test of all these chips.

From 2002 to 2004 the calorimeter was assembled and tested. The assembly and individual test of the 32 barrel modules and as many endcaps was surprisingly fast in view of the time it took to build the module 0 and the whole detector could be closed in 2003. Once the calorimeter was complete we had to intervene once more to measure on the 200 000 channels the calibration resistors, the detector resonant frequency and feedthrough grounding quality, both in the warm and then in the cold. These measurements, essential to reach the 0.7% calorimeter accuracy are detailed in chapter 3.

Final production of all the electronics was done and the boards progressively installed. For us, this concerned mostly the 130 calibration boards which were completed and tested in 2005, with a few surprises in the production phase that are described in chapter 2.

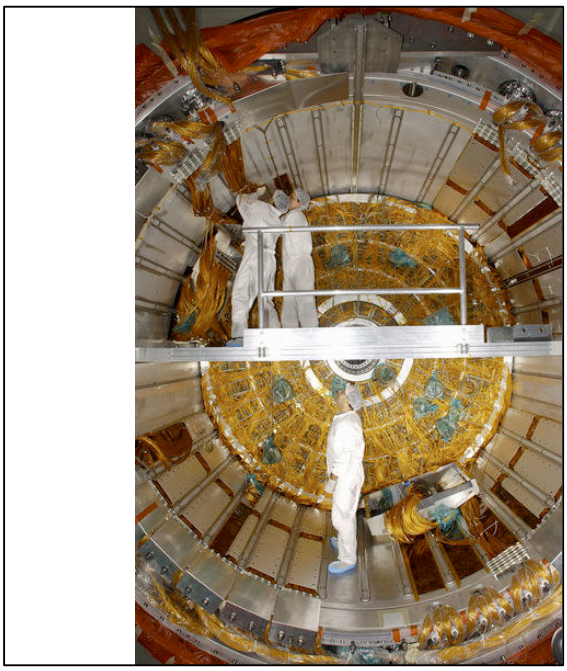


Figure 10 : barrel calorimeter assembly

2. Preamplifiers

The three main issues for the preamplifiers were the following :

∞ Low noise : due to the large detector capacitance (400-1200 pF) the series noise is totally dominant and the series noise spectral density was targeted lower than e_n<0.3 nV/√Hz

∞ Large dynamic range : the maximum signal is 1 nC and the noise corresponds to 20 fC. This constraint turned out to be very difficult for charge preamplifiers.

∞ High speed : the optimum shaping time is around 25-50 ns, as will be shown in § 3

∞ Good radiation hardness : doses up to 1 kGy[8] and fluences of 10^{13} N/cm² (1 MeV/eq.)

2.1. Charge sensitive preamplifiers

The charge preamps had the difficulty of accepting the maximum signal of 1 nC. With a feedback capacitance of C_F=33 pF, the preamplifier saturated at 100 pC corresponding to 10% of the total charge. This saturation was acceptable as these events are very rare provided the preamp would not stay "dead" for a long time. The charge preamps proposed by BNL were following the classical "*Radeka topology*" of folded cascade entirely built with Si NJFETs (*cf* Figure 11) specially developed for this purpose by Interfet. The model NJ450 exhibits a large transconductance g_m=20 mA/V at 5 mA drain current with a relatively high capacitance of 60 pF. It operated at liquid argon temperature (89 K) although the optimum temperature for the noise was 120 K. We measured (Figure 12) these preamplifiers during a stay at BNL and found interesting behavior of transconductance and series noise versus temperature[9]. In the end, these preamplifiers were not used for ATLAS but equipped the NA48 liquid krypton calorimeter.

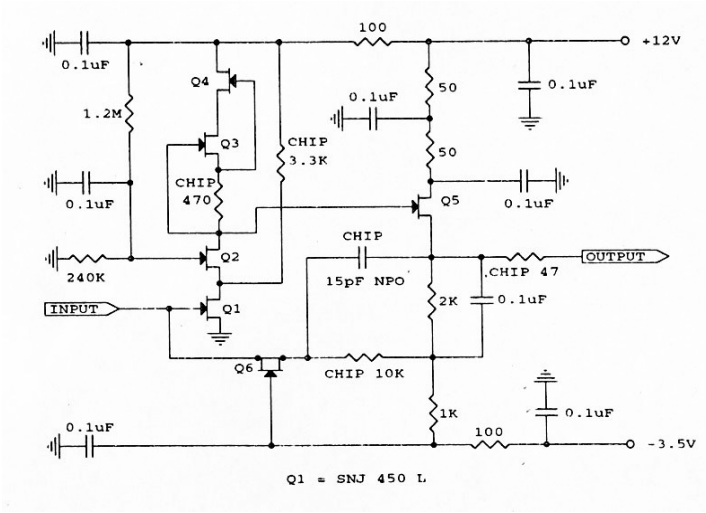


Figure 11 : Schematic of JFET Charge preamp used in NA48 and ATLAS prototype as proposed and designed by BNL.

∞

[8] 1 kGy = 100 krad

[9] The noise density follows nicely the theoretical value of $4kT\gamma/g_m$ until 120 K. Below, it rises again to reach higher values at liquid nitrogen temperature than at room temperature, presumably due to non thermal equilibrium of the carriers with the lattice.

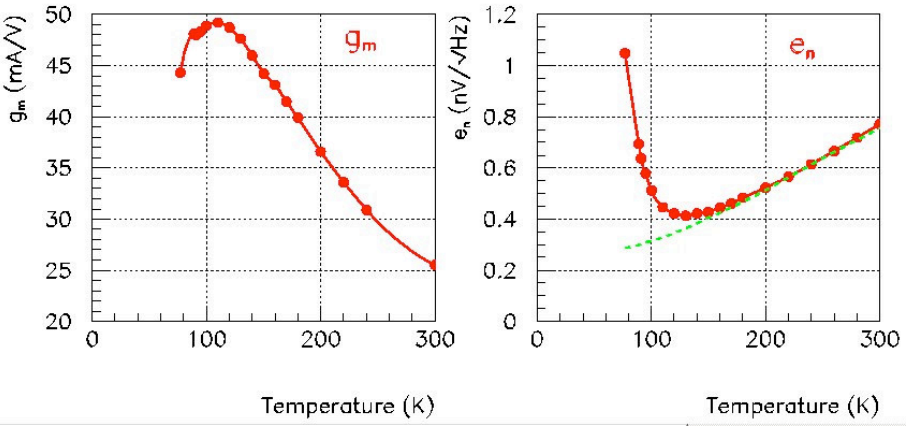


Figure 12. Left : transconductance g_m (at I_D=5 mA) of NJFET InterfetNJ450 as a function of temperature. Right : measured series noise e_n. It can be seen that the series noise departs from the theoretical thermal noise (green curve) below 120 K

2.2. GaAs current sensitive preamplifiers

To overcome the limitation of charge preamps with the huge maximum incoming charge, a non-integrating configuration was proposed, referred to as current sensitive preamplifier, replacing the feedback capacitor C_F by a resistor R_F. In this configuration the preamp input impedance can be modelized as an inductor[10] : $Leq=R_F/\omega_c$ where R_F is the feedback resistance and ω_c is the preamplifier bandwidth. This configuration is of course easily oscillatory with a capacitive detector and the faster the amplifier, the more stable it is[11], which has pushed in favor of GaAs technology. Besides, the superior mobility in GaAs has a beneficial impact on transistor channel white noise. The traditionally poor 1/f performance of these transistors was alleviated by the operation at high frequency (~10 MHz) and lower temperature. These preamplifiers were developed by the Milano group led by *D. Camin* and showed series noise as low as e_n<0.2 nV/√Hz. The schematic was similar as the JFET one shown in Figure 12, except for the feedback element now a resistor R_F = 1.5 kΩ and a compensation feedback capacitor C_F~10 pF to ensure stability. They were also proposed and finally chosen (Figure 13) for the Hadronic End Cap.

One additional advantage of current sensitive preamplifiers in this case was the smaller sensitivity to second stage noise as shown in, which is due to the larger amplification at high frequencies (cf § 3)

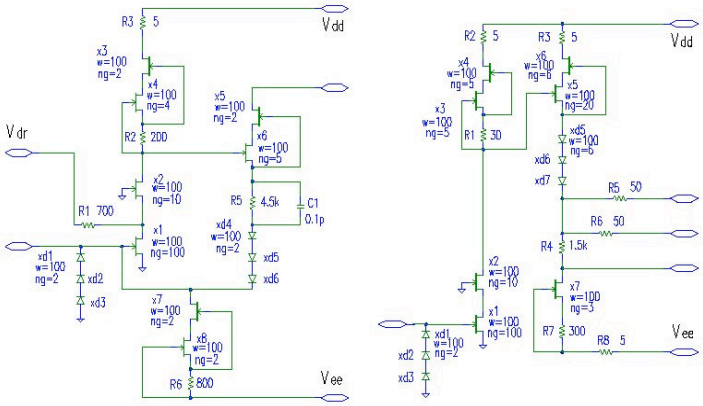


Figure 13: GaAs current sensitive preamplifier used in the Hadronic End Cap, developed by Munich MPI group

∞

[10] The input impedance of the shunt-shunt configuration is Z_F/G. With the usual gain roll-off with frequency as $G(\omega)=G_0 / (1+j\omega/\omega_c)$ the input impedance becomes $R_F/G_0 + j\omega R_F/\omega_c$ which is the series combination of a small resistance R_F/G_0 (usually negligible) with and inductor R_F/ω_c

[11] The smaller equivalent inductance (R_F/ω_c) allows a smaller damping resistor $\sqrt{Leq/C_D}$, usually realized with a small C_F

2.3. Remote current-sensitive line-terminating preamplifiers (ØT) (PhD Y. Jacquier)

An unexpected consequence of operating at high speed with large detector capacitance was that a transmission line between detector and preamp did not degrade the noise with the usual penalty of ~100 pF/m. Putting away the preamplifier largely alleviates constraints of radiation hardness, power dissipation inside the liquid argon with the risk of bubbles and allows maintenance operation in case of dead channels. The reason is explained on the plot in Figure 14 that shows the impedance Z of a line of characteristic impedance R_c and length t_d, terminated by the detector capacitance C_D :

$$Z = \frac{1 - \omega . R_C C_d \tan \omega . t_d}{j\omega . C_d + j \tan \omega . t_d / R_C} \qquad (1)$$

As the series noise scales as e_n / Z, it can be noted that at the central frequency of the filter (~10 MHz) the impedance of a detector capacitance of C_D=1 nF is smaller than the cable impedance, thus the noise can be lower with a cable than with the detector capacitance alone.

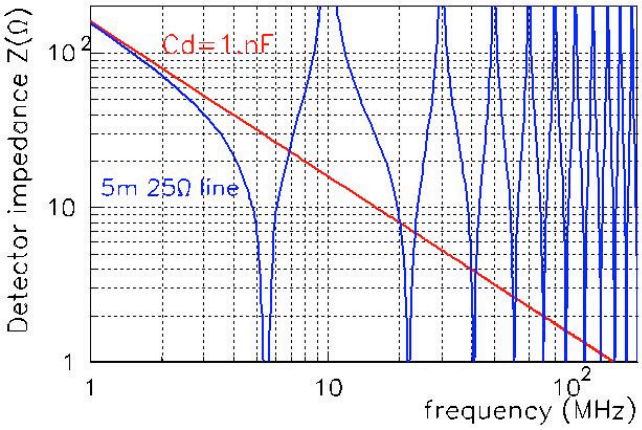


Figure 14: detector impedance as a function of frequency at the input and output of a 5 m cable.

This new approach led to two publications in NIM [5][6] and was proposed to the collaboration as the "ØT option" meaning "Zero Transistor in the cold". The salient points in the two publications concerned

∞ Calculation of the noise with an ideal transmission line between detector and a line terminating preamp. The conditions under which the line does not degrade the noise performance is to have a long line with an impedance higher than the detector at the central frequency of the filter. In other terms, if t_p is the shaper peaking time : $t_d > t_p$ and $R_C C_D > t_p$, which applied to the ATLAS case (R_C=25 Ω, C_D=1 nF, td=25 ns, tp=25 ns)

∞ Calculation with a real line, including signal attenuation due to skin effect in the line and the thermal noise generated by the skin effect resistance. This introduced a noise dependence with the line length, in good agreement with the experimental measurements, especially with the use of miniature coaxial cables in which the skin effect is non negligible.

∞ Design of the line terminating current sensitive preamplifier. In the first paper, a charge preamplifier was used to terminate the line as its input impedance $Rin=C_P/g_mC_F$ is resistive[12] and can be adjusted to 50 Ω. However, the difficulty of handling the full dynamic range and the poor linearity due to the change of input impedance with signal amplitude led to the development of a current-sensitive line terminating preamplifier. This preamplifier was also taking advantage of the excellent series noise of the bipolar technology as the ATLAS parameters (speed and large detector capacitance) were rendering the parallel noise of the base current completely negligible.

∞

[12] The input impedance of an amplifier of gain G(ω) with Z_F feedback is Z_F/G+1. With $Z_F=1/j\ \omega C_F$ and $G(\omega)=G_0/1+j\ \omega/\omega_0$, the input impedance becomes $ZIN=1/j\ G_0\ \omega C_F + G_0\omega_0 C_F$ where the second term dominates at the usual operating frequencies and is purely resistive.

The experimental measurements validating the calculations are recalled in Figure 15

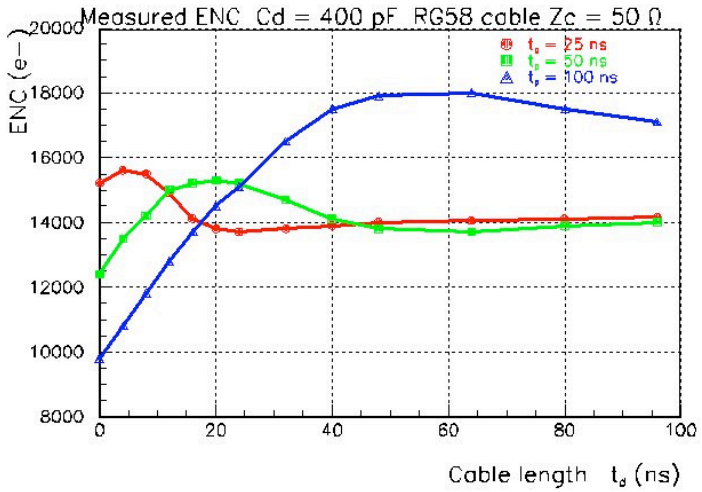


Figure 15: experimental measurement of Equivalent Noise Charge (ENC) as a function of cable length. The three curves are for three different shaping times : 25, 50 and 100 ns. ATLAS corresponds to the red curve (25 ns) which shows no noise penalty with a long line compared to without line. The classical case corresponds to the blue curve (100ns) which shows a linear increase of the noise with the cable length corresponding to an additional capacitance of 100 pF/m.

The preamplifier design started from a common base configuration which is very classical for current conveyor and line termination. The input impedance being $1/g_m$=26mV/I_C can be tuned to the cable impedance by playing on the collector bias current I_C while the series noise is only $e_n^2 = 4kT(1/2g_m+R_{BB'})$. The latter term is known to dominate at large current and several low noise high frequency transistors were tested to select the NE856 by NEC which exhibited the lowest $R_{BB'}$ = 4 Ω. In order to reach the target noise of 0.4 nV/√Hz, corresponding to 10 Ω noise resistance, it is necessary to aim for a transconductance of g_m~200 mA/V (!) and thus operate at Ic~5 mA. However, in that case the input impedance $1/g_m$ = 5 Ω becomes too low to terminate the line and needs to be increased by applying series/parallel feedback with the divider R2/R1. The input impedance can be calculated as Rin=R_F*R1/R2. R1 needs to be order of a few ohms to limit its noise contribution making R2 a heavy load on the output. This in turn needs an ultra low output impedance buffer built with the closed loop configuration of "White follower". This resulted in the schematic below (Figure 16) extracted from [5]. It was subsequently upgraded by BNL to reduce the power dissipation and produced by BNLand Milano in the form of 4-channel hybrids.

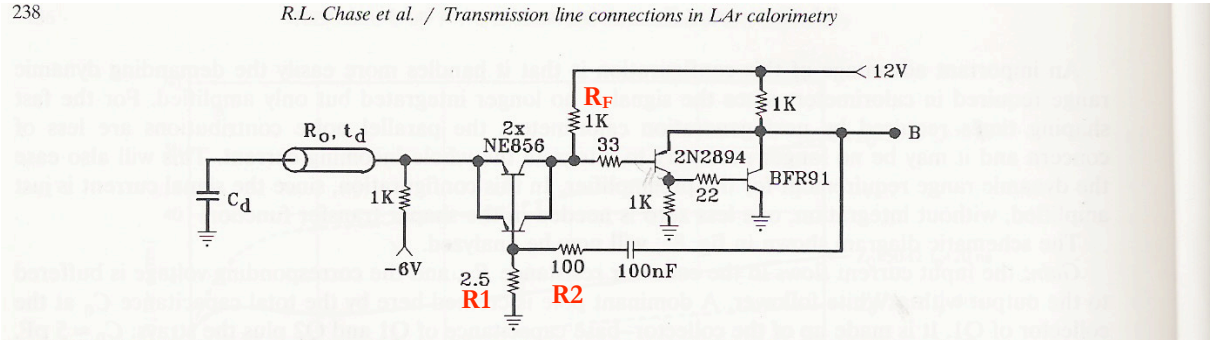


Figure 16: schematic diagram of the first ØT preamplifier

2.4. Preamplifier choice (LArG note 35)

The three types of preamps have been validated in test beam runs and the results were consistent with the electronics measurements performed on test bench. Rapidly, the preamp based on JFETs was dropped as it was more noisy than GaAs technology and did not cope well with the full dynamic range in charge sensitive configuration[13]. The choice remained between ØT and GaAs throughout numerous measurements in 1994-1996.

Very quickly ØT preamps were chosen in the front section as the granularity was much finer[14] to accommodate the space for preamps. Besides it was important in front of the calorimeter to minimize all the dead material and in particular liquid argon which was obtained by removing all the electronics. The impact on the noise was not large as only 10-20% of the energy is deposited in the front section.

The results were summarized in a LAr note #35. As will be shown in the section describing the shaper, the noise in MeV was extremely sensitive to the actual shaping time and several effects needed to be taken into account to make a fair comparison. As explained in § 3.1. the noise is expressed as Equivalent Noise Current (ENI) and fitted on experimental measurements as a function of shaping time[15] for various detector capacitances as $ENI^2 = A/tp^5 + B/tp^3 + C/tp$ (*cf.* Figure 17).

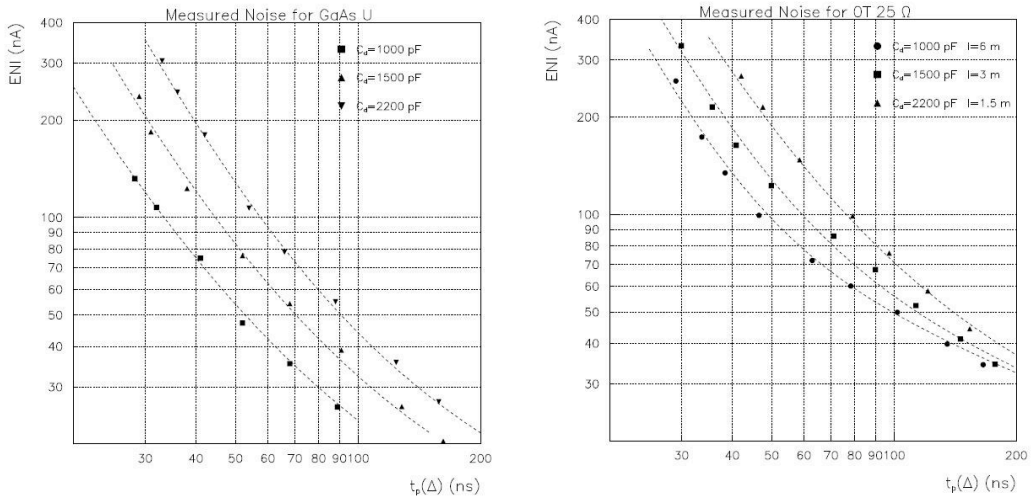


Figure 17: Equivalent noise current ENI as a function of shaping time as measured on GaAs preamplifiers and ØT preamplifiers for various detector capacitances (1, 1.5 and 2.2 nF). The experimental measurements are fitted in order to extrapolate the noise to all the various cells in the calorimeter.

The noise is then calculated in a $\Delta\eta x\Delta\varphi$=3x7 cluster[16], summing 48 front cells, 21 middle ones and 12 back ones (see Chapter 3 for detector segmentation). It was then scaled into Equivalent Noise Energy (ENE) with the detailed calculation of the sampling fractions[17], with typically $I_0/E \sim 3$ nA/MeV. The pileup noise was then added, giving a noise scaling as $C*t_p$ (cf § 3.1.). The total noise as a function of shaping time is then calculated as shown in Figure 23, exhibiting a minimum for an optimum shaping time at a given luminosity.

∞

[13] Si JFET was also not fast enough to be used in current sensitive configuration

[14] To get good position accuracy and π^0 rejection (see chapter 3)

[15] As shown in §3.1, $ENI^2 = A\ e_nCt/tp^3 + B\ i_n/tp$. The first term in tp^5 has been added empirically in order to get a better fit at fast shaping.

[16] The larger dimension in $\Delta\varphi$ is due to the shower "opening" in φ with the magnetic field.

[17] The sampling fraction is typically 0.25 corresponding to 4.2 mm of LAr (0.89 MeV) and 1.5 mm Pb + dead material (2.7 MeV)

This was then calculated over all the calorimeter rapidity, taking into account the variation of detector capacitance as well as the pileup increase with rapidity, as shown in Figure 18, providing an estimation of the electronics noise that is being used in the overall simulation of physics performance.

The small difference of total noise between ØT and GaAs led to the choice of ØT everywhere in the calorimeter to minimize the risk of dead channels in the cold where no maintenance is possible. The ØT preamps have then been taken in charge by BNL and Milano, modified to optimize their power dissipation and fabricated as 4-channel hybrids.

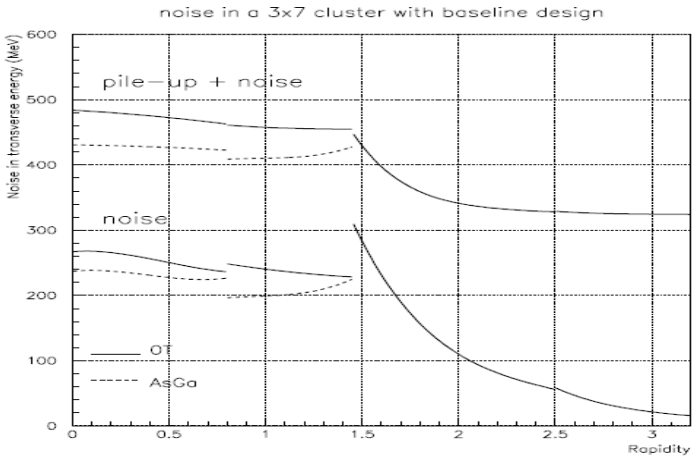


Figure 18: total noise in a 3x7 cluster as a function of rapidity

3. Shaping (3 LArG notes)

The shaping had been proposed very early in the paper from *Radeka/Rescia* [4] to make the long signal from liquid argon compatible with the high luminosity operation. The paper was comparing the benefit of bipolar $(CR)^2(RC)^n$ and tripolar shaping $(CR)^3(RC)^n$ to get rid of the trailing edge of the liquid argon pulse. It was used with a charge preamp in the input and calculated the pileup as a function of speed and urging for bipolar signal shape with zero net area to avoid the baseline shifts in all subsequent AC couplings.

Now, all the usual assumptions of detector signal short compared to the shaping time and preamplifier rise time negligible were not true in the LAr case, on the contrary, the signal was even almost infinitely long (500 ns) compared to the shaping time (20-50 ns). With the move towards current sensitive preamplifiers, it was clear than one less differentiation was needed in the shaper and that Charge Preamp + $(CR)^2(RC)^n$ was equivalent[18] to Curent Preamp + $(CR)(RC)^{n+1}$. However, the noise behaviour of current sensitive preamplifiers were not as well established as those of charge preamplifiers. It was then necessary to perform some theoretical calculations and introduce the notions of Equivalent Noise Current (ENI) and the peaking time to the step or the triangle (tp(Δ)) between 5% and the peak as robust description of the shaping. This replaced conveniently the notions of "effective integration time" necessary to convert ENC into MeV and took well into account all the detector and preamplifier contribution to the shaping time, which is not at all negligible at fast shaping.

∞

[18] The transfer function of an ideal charge preamplifier is $1/sC_F$where as it is just R_F for a current preamplifier. The 1/s term simplifies with the second differentiation of the CR^2RC^n shaper whose transfer function is $(\tau s)^2/(1+\tau s)^{n+2}$

3.1. Theoretical analysis (LArG note 010)

The detailed analysis of shaper architecture and fair way of comparing noise measurements, in particular to take into account the preamplifier rise time were detailed in the LArg010 note [10]. It gave theoretical expressions of signal and noise of current sensitive preamplifiers followed by CR RC^n shapers.

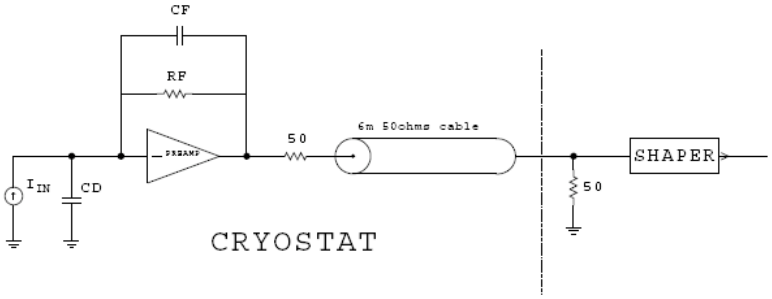


Figure 19 : synoptic diagram of current sensitive preamplifier and shaper CRRC^n. This diagram also applies for ØT preamplifier, for which the cable is located before the preamplifier instead of after.

The transfer function for the GaAs or ØT preamplifiers are very similar and are calculated in the frequency domain with a $CRRC^2$ shaper :

$$H(s) = \frac{R_F}{1+s\tau_{PA}} \frac{s\tau_{SH}}{(1+s\tau_{SH})^3}$$

In which R_F is the preamplifier transimpedance, τ_{PA} is the preamplifier pole[19] and τ_{SH} the shaper time constant. The triangular signal from the liquid argon detector is also described in the frequency domain as well as the exponential pulse from the calibration system (*cf.* Chapter 2) or the step used in testbench measurements. The expressions are then calculated in the time domain by taking the inverse *Laplace* transform to provide literal expressions that can be used in the detector simulation. The effect of the preamp risetime on the overall response as well as the difference between step, triangular and exponential response are shown in Figure 20.

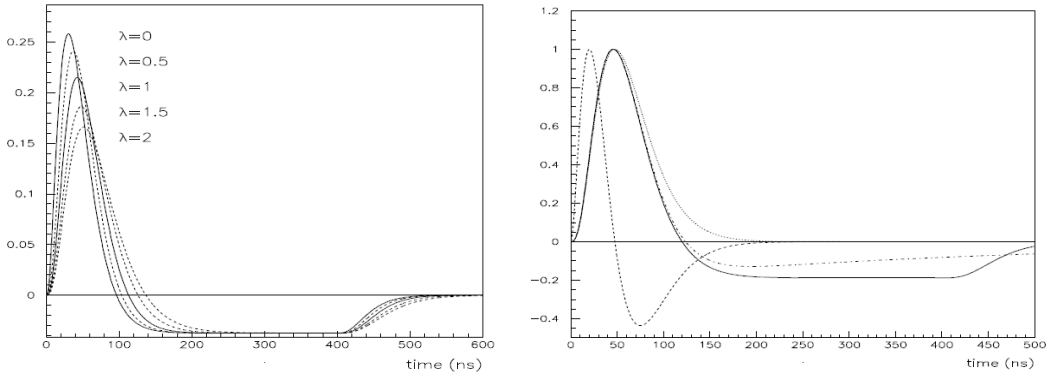


Figure 20. <u>Left</u> : shaper response to the triangular ionization current for various preamplifier time constants ($\lambda = \tau_p/\tau_{sh}$). <u>Right</u> : response to the step, ionization current and exponential calibration pulse

[19] In a current sensitive preamplifier, $\tau_{pa} = R_F C_F$; in the case of the 0T preamp, $\tau_{pa} = R^0 C_D$

The **rms noise** at shaper output is also classically calculated in the frequency domain :

$$v_n^2 = \frac{e_n^2 C_d^2 R_f^2}{\tau_{SH}^3} \int_0^\infty \frac{(\omega\tau_{SH})^4}{(1+\omega^2\tau_{pa}^2)(1+\omega^2\tau_{SH}^2)^3} \frac{d(\omega\tau)}{2\pi} + \frac{i_n^2 R_f^2}{\tau_{SH}} \int_0^\infty \frac{(\omega\tau)^2}{(1+\omega^2\tau_{pa}^2)(1+\omega^2\tau_{SH}^2)^3} \frac{d(\omega\tau_{SH})}{2\pi} \quad (1)$$

These two integrals depend only on $\lambda = \tau_{pa}/\tau_{sh}$ and are noted $J_a^2(\lambda)$and $J_b^2(\lambda)$. It can be noticed that the *rms* noise v_n depends much more strongly on the shaping time (in $\tau^{-3/2}$ and $\tau^{-1/2}$) as with the usual charge sensitive configuration[20] as recalled in Figure 21. As for the signal response, the response to the triangular ionization current I_0 is very similar to the response to a step of amplitude I_0, which gives a response independent of the shaping time and noted $h_{max}(\Delta)$. Thus the noise can be referred to the input as equivalent Noise Current (ENI) defined as ENI = v_n / $h_{max}(\Delta)$. Thus

$$ENI = e_n C_D \frac{Ja(\lambda)}{h_{\max}(\Delta)(\lambda)\tau_{SH}^{3/2}} \oplus i_n \frac{Jb(\lambda)}{h_{\max}(\Delta)(\lambda)\tau_{SH}^{1/2}} \quad (2)$$

in which e_n and i_n are the series and parallel noise spectral densities (nV and pA/√Hz), C_D is the detector capacitance, $h_{max}(\Delta)$ the shaper amplitude and τ_{SH} its RC time constant.

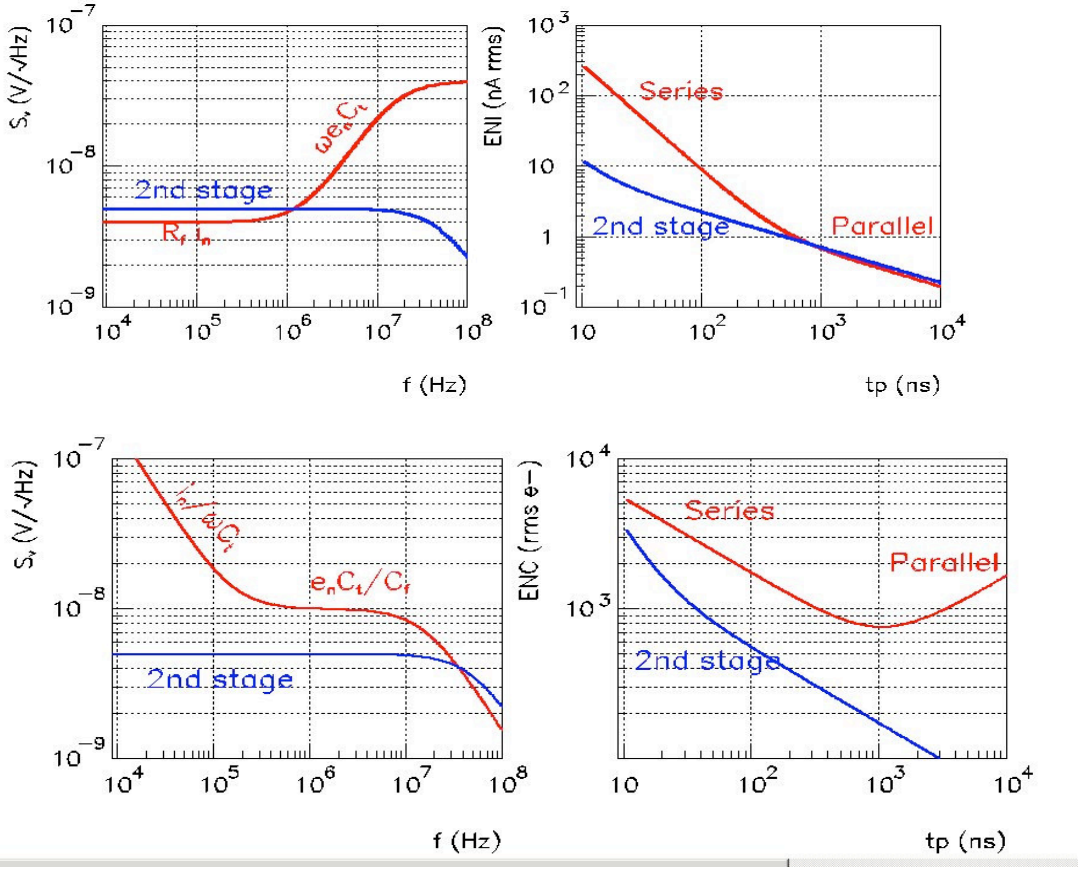


Figure 21: Noise spectral density and Equivalent Noise Current (ENI) of current sensitive (top) and charge sensitive (bottom) configurations. The second stage noise is smaller at short shaping time for current sensitive configurations

[20] The noise can anyhow be referred to the input as ENC, but with the current sensitive configuration, the impulse response $h_{max}(\delta)$ is no longer independent of shaping time, but scales as $1/\tau$. Dividing v_n by $1/\tau$, yields the usual ENC behaviour as $A/\sqrt{\tau}$ (+) $B\sqrt{\tau}$.

Moreover, after calculating the noise integrals for various preamplifier rise time, it has been shown (Figure 22) that they are invariant when the noise is expressed as a function of the peaking time (5%-100%) to the step (or the triangle) which is noted tp(Δ) allowing to write :

$$ENI = e_n C_d \frac{Bs}{t_p^{3/2}(\Delta)} \oplus i_n \frac{Bp}{t_p^{1/2}(\Delta)} \qquad (3)$$

in which Bs and Bp are almost constant, as shown in Figure 22. Similar calculation for higher order shapers CRRC^n gives the same result, making of the peaking time a good estimator of the shaper response as shown in LArG10.

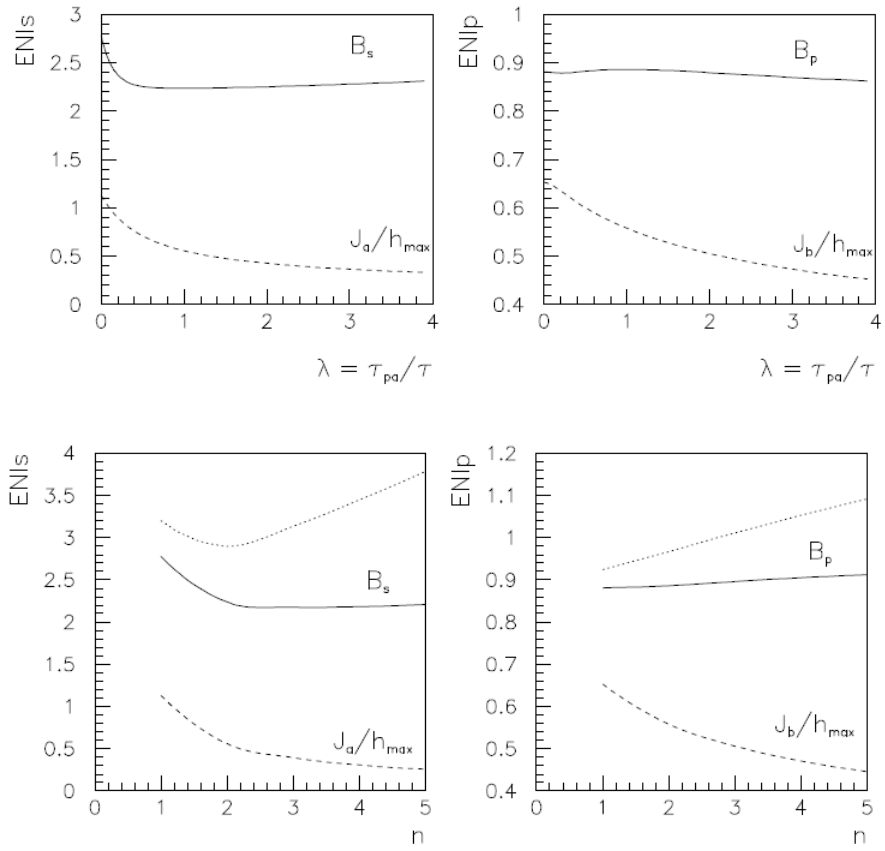


Figure 22: Series and parallel noise coefficients as a function of preamplifier risetime to shaping time ratio λ.(top) and CRRC^n filter order (bottom). The terms Bs and Bp which are used in Equation (3) to calculate ENI are almost independent of λ or n making the peaking time tp(Δ) 5-100% a good estimator of filter response.

The **Pileup noise** is mostly due to the superposition of numerous minimum bias events, whose low energy allows to handle them as a noise source. The calculation is done using *Campbell*'s theorem and the variance of these events is given by [21] :

$$\sigma_{pu}^2 = \iint n(E)V^2(E,t)dEdt = \sigma_E^2 \int h_\Delta^2(t)dt = C\sigma_E^2 I_{pu}^2 = C\sigma_E^2 t_p(\Delta) \qquad (4)$$

The pileup integral I_{pu}^2 is similarly proportional to the peaking time $t_p(\Delta)$ 5-100% and increases with slower pulses as intuitively expected.

∞

[21] The integral assumes a continuous sum on time, disregarding the bunching at 25 ns. The effect is negligible for peaking times longer than 25 ns, below it is of course asymptotic to the irreducible pileup contained inside one bunch crossing.

The **total noise** is the sum of all these contributions and is shown in Figure 23. The total noise exhibits an optimal shaping time at which the noise is minimal[22] : $t_p^{opt} = K\ (e_n C_d/\sigma_E)^{1/2}$ and at this optimum the noise is given by $ENE^{opt} = K'\ (e_n C_d)^{1/4}(\sigma_E)^{3/4}$ which shows that the pileup noise contribution σ_E is dominant. As the pileup noise is changing both in time and in rapidity, the optimum shaping time is varying and this will be done by digital filtering as shown in §3.3.

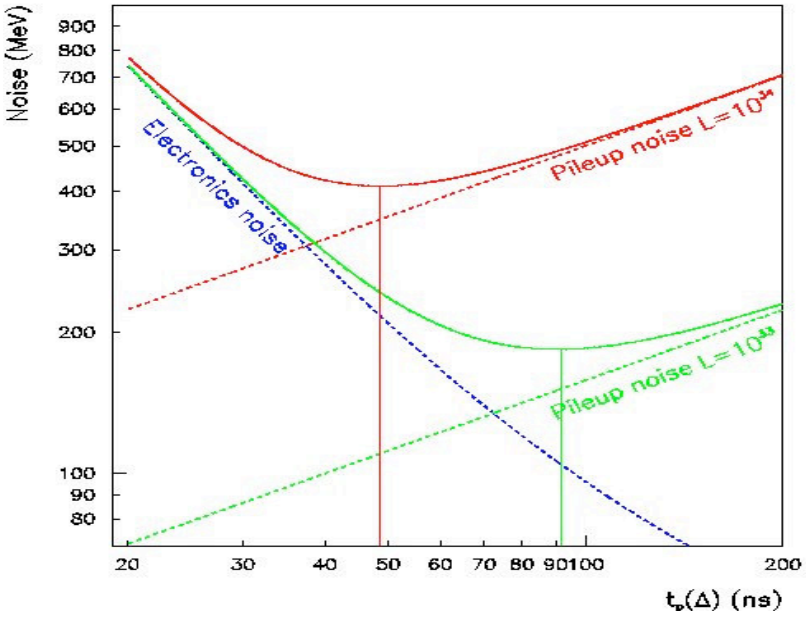


Figure 23: Total noise in a 3x7 cluster as a function of signal peaking time at low ($L=10^{33}\ cm^{-2}s^{-1}$) and high ($L=10^{34}\ cm^{-2}s^{-1}$) luminosity. The noise exhibits a minimum which is dominated by pileup noise.

3.2. Monolithic realization (LArG note 082)

As the readout electronics needed to be located right on the feedthroughs, in the crack between barrel and end-cap calorimeters, real estate was a major concern and it was obvious that the shaper needed to be integrated inside an ASIC. The schematic proposed in LARg10 was directly derived from the circuits realized with surface mount components for testbeam purposes and stubbornly oscillated[23]. A little later, the ØT preamp were chosen to equip the whole calorimeter, simplifying the problem of having to deal with both signal polarities and it was felt necessary[24] to split the 16 bits dynamic range in three linear ranges of 12 bits, with a gain ratio of 1-10-100. Afterwards, this can be considered as an overkill, but at that time the possibility of having large coherent noise in the subsequent stages (SCA, ADCs…) was very much feared. Also, as there was not such a high gain in the preamp, the shaper needed to be low noise (<2 nV/√Hz, almost like a preamp) in order to add a negligible contribution. Moreover, the multiple sampling technique (see §3.3.) relaxed the complexity of the shaping function and a $CRRC^2$ was by far enough, minimizing the number of stages and power dissipation.

All these constraints led to the choice of an architecture based on custom low noise operational amplifiers in BiCMOS 1.2 µm technology. To minimize the noise, the high gain amplifier was mounted in inverting configuration, providing a first gain of 10, with small resistor values (50-500). The unity gain was following the same architecture.

∞

[22] This calculation neglects the parallel noise which is much smaller than the series noise due to the fast shaping.

[23] despite the last sentence of the note !

[24] In principle (and in the end) 2 gains with 12 bits were enough to cover the dynamic range, but coherent noise was very much feared at the time of design which pushed for having a large high gain of 100 and thus 3 gains.

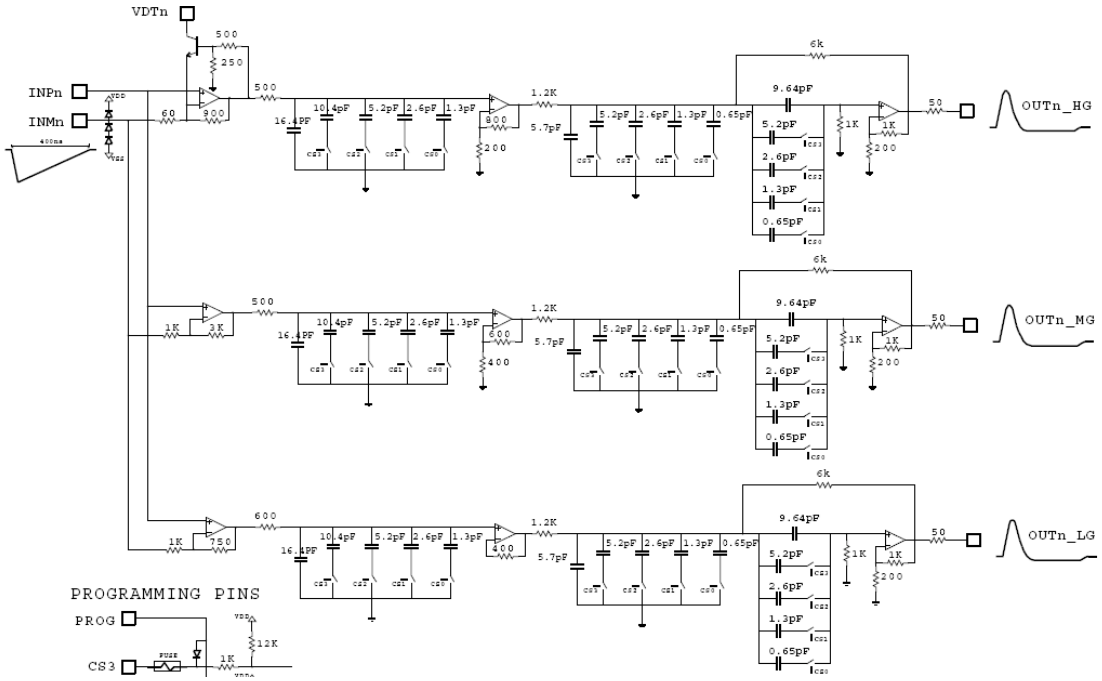


Figure 24 : schematic diagram of the LAr Trigain CRRC² shaper.

Two prototypes were realized before the series production in 1999 of 65 000 chips. Between these two prototypes, the power supplies had been reduced, the RC values had been made tunable with fuses so that each shaper could be made identical irrespective of the large fluctuations on R and Cs of monolithic processes[25]. A linear mixer was also included, performing the analogue sum of the 4 channels in order to prepare the signal in a 0.1x0.1 tower for the LVL1 trigger.

The performance is described in LArG92. An example of waveforms can be seen in Figure 25, showing the peaking time adjustment range. The 4 bits allowed the peaking time to span from 20 to 40 ns, giving a step of 1 ns for the peaking time or 0.5 ns for the time constant. In view of the results from digital filtering described in §3.3. , the time constant was also slowed down[26] to τ_{SH} = 15 ns.

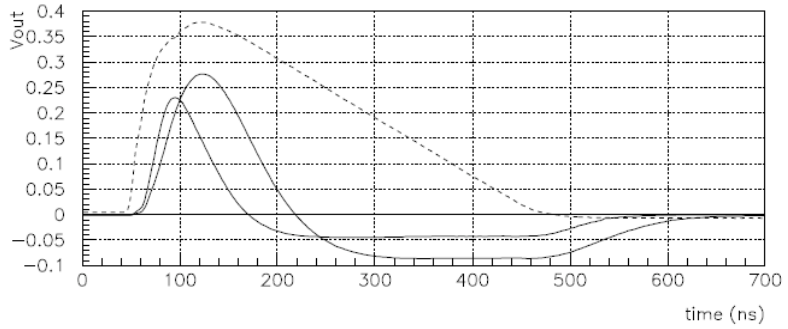


Figure 25: shaper waveform for minimum and maximum peaking time adjustment. .In dashed line the input signal from the ØT preamplifier used to drive the shaper

∞

[25] Typically ±20% for resistors and capacitors

[26] despite *D. Fournier*'s resistance !

The three gain values were 0.8, 8 and 82 and the noise respectively 250 µV, 350 µV and 850 µV giving a dynamic range of 3 V/850 µV/82 = 400 000 = 18.5 bits

As shown in Figure 26, the linearity is within ± 0.1% on the three gains and the crosstalk at the 0.1% level.

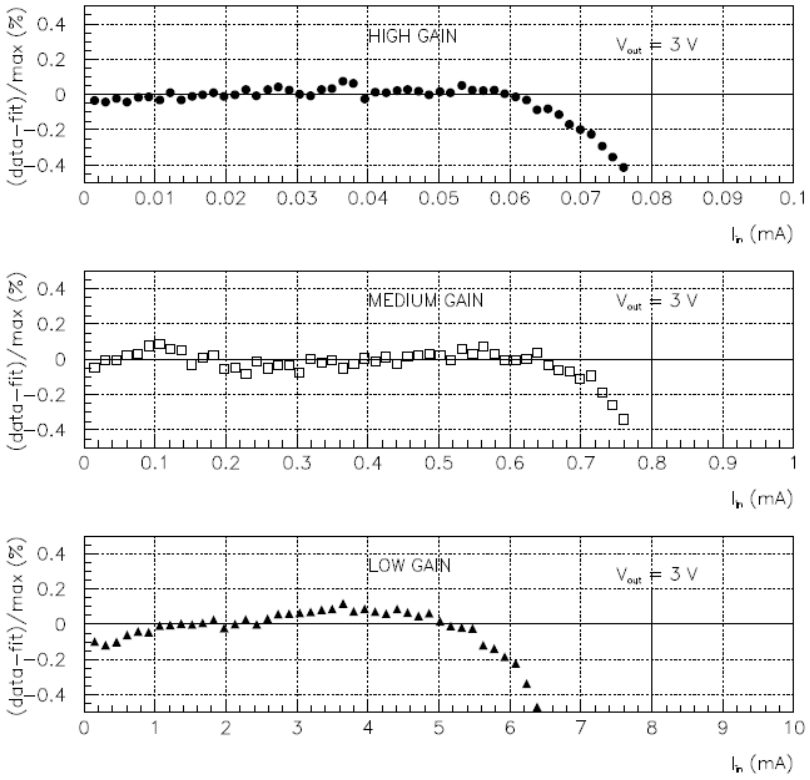


Figure 26: linearity of the shaper + ØT preamplifier on the three gain ranges.

In 1998, 80 000 shapers were produced in an AMS 1.2 µm BiCMOS dedicated run. They were packaged in QFP100 plastic package and tested by a robot developed by the Grenoble group (Figure 27) that allowed to test automatically this large quantity in around 6 months. The yield was found to be 85%. Later, when all the chips were soldered on the Front-End Boards, it was observed that a few per mil of the chips had instabilities in the shape, traced to fuses partially blown, that tended to reconnect.

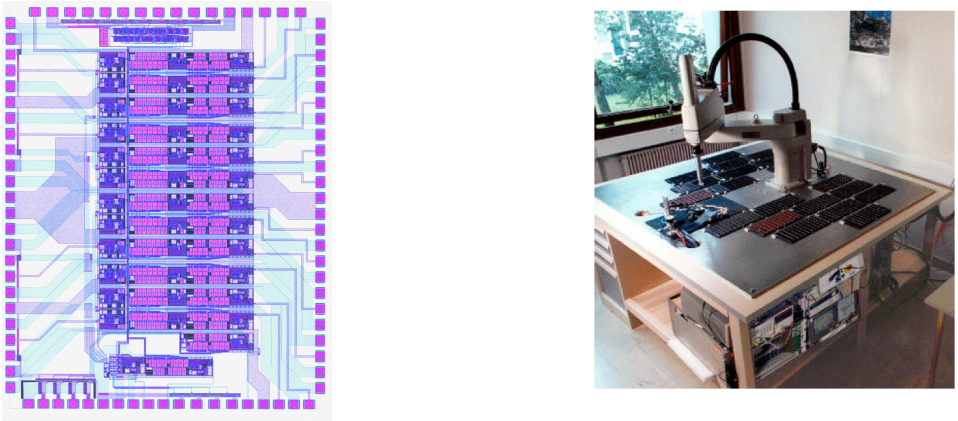


Figure 27: shaper layout (4 channels) and view of the robot developed by Grenoble group to test automatically the 80 000 chips

3.3. Multiple sampling or digital filtering (LArG 80, PhD Y. Jacquier)

The multiple sampling technique was introduced in our field[27] by *B. Cleland* in 1993 [7]. It was a way to approach very close to the theoretical optimum filter by digital signal processing which rendered the old approach of complex filters completely obsolete. Moreover, it was flexible and adaptative, it could thus allow to always run at the optimum signal to noise ratio, on the whole calorimeter regions and adapting to the change in luminosity as the machine tuning progresses.

The calculation has been detailed several times to optimize the amplitude measurement knowing several samples on the waveform and combining them with optimized weights to form the energy. It showed than in our practical case, when the experiment would start at low luminosity, the noise could be lowered by more than a factor of 2.5 which sounded unbelievable ! Naively, we were imagining that "summing" a few samples would increase the amplitude but the noise would only increase by the square root of the number of samples. This naïve approach was completely missing the role of the noise autocorrelation function.

To convince ourselves, we needed to make the calculation ourselves with the help of *L. Serin* and our PhD student *Y. Jacquier* and to do testbench measurements and actually reach the calculated values. After that, the first experimental measurements on the test beam data turned out to be very disappointing and more work was needed to understand them, in particular how could we evaluate the digital filtering transfer function and compare it with classical analog filters.

In the course of this study, several questions arose, such as :

- What is the transfer function of the digital filter, what is its effect on the signal ?
- What is the noise improvement for different shaping times used ?
- How many samples are necessary on the waveform ?
- How does it compare to an optimized analog shaper ?
- On what luminosity range can it improve the signal to noise ratio ?
- For what luminosity should the analog shaper be optimized ?
- Is the analog shaper really necessary, can't we use directly the preamp signal ?
- How accurately needs the signal shape to be known ?

All these issues have been addressed in a detailed LAr note LArg80 (1998) **Erreur ! Source du renvoi introuvable.**. Without going into technical details, the pulse amplitude A is obtained by combining linearly n samples S_i on the waveform g(t) with a weight a_i and requesting the normalization $\sum a_i g_i = 1$. The optimum weights are obtained from the noise autocorrelation matrix Rij with :

$$A = \sum_{i=1}^{n} a_i S_i \quad \text{with } a_i \text{ given by : } \quad a_i = \sum_{j=1}^{n} R_{ij}^{-1} g_j \qquad (5)$$

The autocorrelation function can be calculated literally as shown in *Jacquier's* thesis [8] and it is shown in Figure 28, in the case of the electronics noise of the ØT preamplifier, without any pileup noise. In that case, the coefficients calculated to reduce the noise are typically $a_i = \{0.17, 0.34, 0.4, 0.31, 0.28\}$, which corresponds to a "sliding window" or close to an average over the 5 samples. The resulting waveform can be calculated at all time using Equation (5 left) and is displayed in Figure 28, showing a slower (and more symmetrical) waveform by a factor close to two. As will be discussed later, it is also possible to accelerate the pulse, also by a factor of two, for operation at very high luminosity.

[27] It was known in other domains as "digital filtering" or Finite Impulse Response (FIR) filters

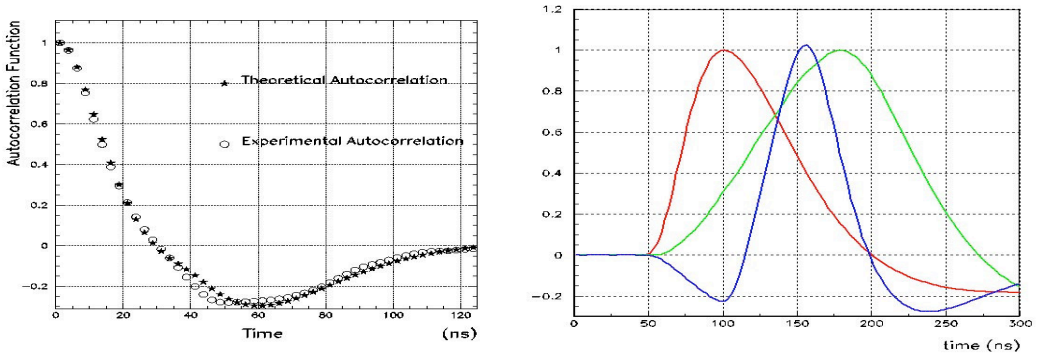


Figure 28 Left : autocorrelation function of ØT preamplifiers. Right : signal before and after digital filtering. The red curve is the signal before digital filtering, from which the 5 samples g_i={0, 0.63, 1, 0.8, 0.4) are taken. The green curve is the signal after digital filtering at low luminosity, applying coefficients a_i={0.17, 0.34, 0.4, 0.31, 0.28}, resulting in a twice slower signal and reducing the electronics noise by a factor 1.8. The blue curve is the output waveform at maximum luminosity, applying coefficients a_i= (-0.75, 0.47, 0.75, 0.07, -0.19) resulting in a faster and narrower waveform, minimizing the pileup noise.

To see it in a more "electronics way", it is possible to calculate the transfer function using the *z-transforms* : $H(z) = \sum a_i z^{-i}$ and letting $z = \exp(j\omega T_{ech})$, in which T_{ech} is the sampling period = 25 ns in the case of ATLAS. This is represented in Figure 29, in the case of low luminosity, showing that the digital filter is cutting down the high frequencies (low pass filter), slowing down the signal and reducing the electronics noise. The bumps at multiple of the sampling frequency (40 MHz) correspond to the classical aliases of the sampled spectrum that are folded over multiples of f_{ech}.

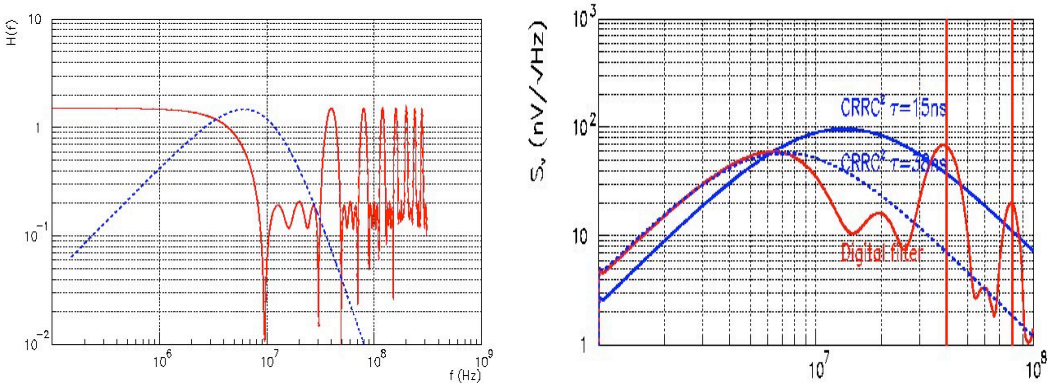


Figure 29. Left : digital shaper transfer function corresponding to the slower pulse as obtained with the z-transfrom. Right : noise after digital filtering. The bumps at multiples of the sampling frequency (40MHz) produce aliases of the noise that have a sizeable contribution to the overall rms noise.

Then the noise spectrum after preamp + analog shaping + multiple sampling could also be plotted and an example is shown in Figure 29. The bumps (aliases) at multiples of 40 MHz explained why the results were not as good as expected in testbeam as the analog filter was too fast compared to the 40 MHz sampling frequency and leaving HF components that were folded by the digital filter.

The noise improvement for different analog shaping times can then be measured and is represented in Figure 30. It can be seen that if the original signal is very fast (10-20 ns) the digital filter is slowing it down by a large factor (more than 2) but the noise is not much improved because of aliasing. The best results are obtained with analog shaping around 20-40 ns where a factor close to 2 is obtained, whereas with a slower signal (50-100 ns) the signal and noise are almost unchanged, as the samples are too close apart, being highly correlated.

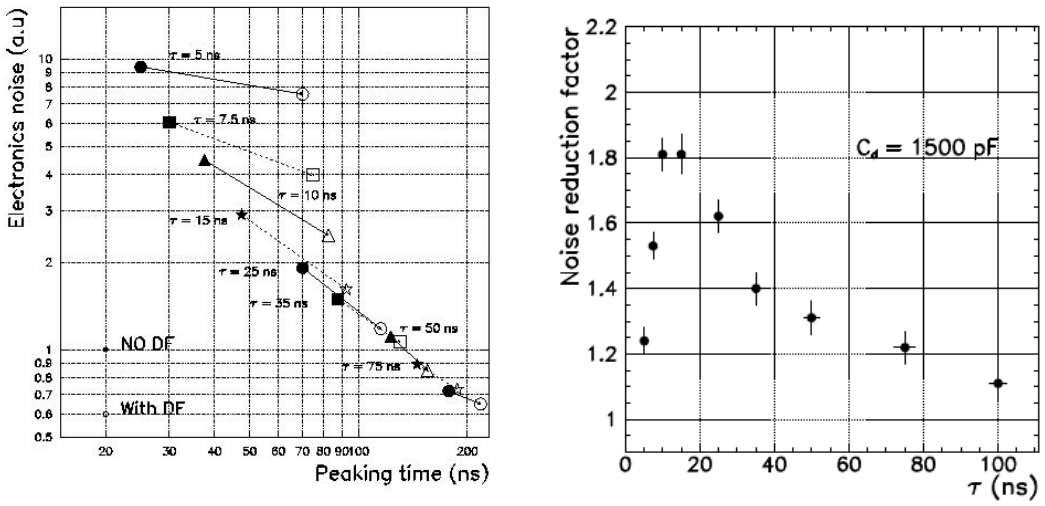


Figure 30: Noise reduction as a function of analog shaper peaking time

The last exercise[28] consists in adding (in simulation) the pileup noise in the autocorrelation function, as shown in Figure 31, resulting in a much longer autocorrelation. The fraction of each noise source scales with the luminosity.

At low luminosity ($L=10^{33}$ cm^2s^{-1}) the pileup noise is small compared to the electronics noise and the digital filtering gives positive coefficients in order to minimize the electronics noise and slow down the signal. At high luminosity, the algorithm gives some negative coefficients in order to substract residuals of previous events and accelerate the signal. The resulting waveforms are shown in Figure 28, exhibiting a twice faster pulse.

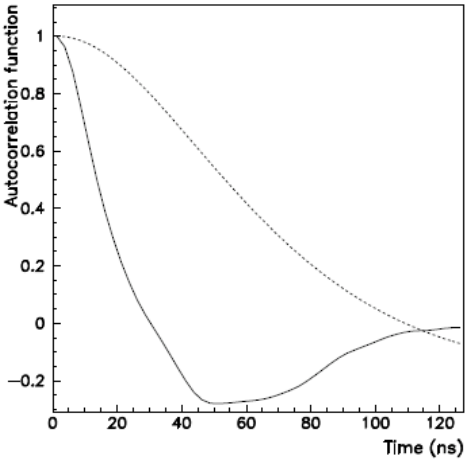


Figure 31: noise autocorrelation function : solid line : electronics noise, dashed line : pileup noise.

For each luminosity, the total noise can then be calculated after optimization and is displayed in Figure 32. It can be seen that the noise after digital filtering (dashed line) is minimum over a wide luminosity range of 10^{33} to 10^{34} cm^2s^{-1}. It compares to the total noise if no filtering is done (solid line) as being always well below, and particularly at low luminosity (large electronics noise reduction). An interesting comparison is also with the optimal hardware shaping (green solid curve), if it were possible to change it dynamically and throughout the detector. It intersects the black solid curve at $L=10^{34}$ cm^2s^{-1}, as the hardware shaping is optimized for this high luminosity. It can be seen that the digital filter is better than the optimized analog filter on the whole range 10^{33} $cm^2s^{-1}$to 10^{34} cm^2s^{-1} by around 10% and that it is only below 10^{33} that the analog filter is better again, mostly because there are not enough points taken to further slow down the pulse at very low luminosity.

∞

[28] Unfortunately, most of the analysis in ATLAS are made with the multiple sampling coefficients tuned for low luminosity operation which tends to alleviate all the systematic effects that appear at high speed, such as detector inductance impact on calibration and physics waveforms (cf Chapter 2 and 3)

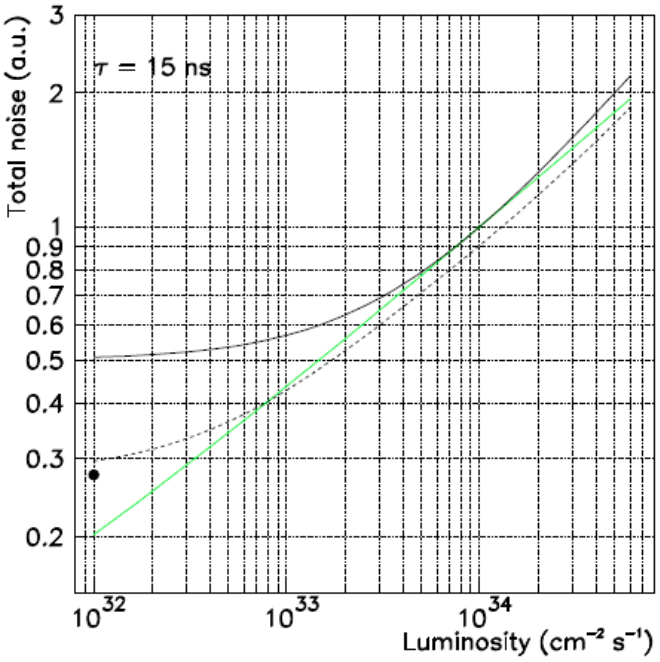


Figure 32: total noise after optimal filtering for various luminosities

4. Conclusion on ATLAS Front-End electronics

From the first prototypes to the production of all the final electronics chips and boards, more than ten years were necessary to overcome all the technical difficulties, in particular due to the speed, large dynamic range and radiation hardness encountered at the LHC. The architectural choices (current sensitive preamplifiers, fast shapers, analog memories, warm voltage driven calibration…) were made relatively early (1994-1996) and the design has barely changed compared to what was written in the TDR (1996) where most issues and problems had been found. The relatively long time between design and production was largely due to the difficulties of mastering the radiation hard DMILL process and the long irradiation and qualification tests. In 2001, all the analog ASICS were being produced in DMILL, but several digital chips had to be moved to DSM (deep sub-micron) 0.25 μm technology.

All ATLAS electronics was produced in 2003-2005 and finished to be installed in nov 2005. It has been running continuously since 2007, with only 0.06% bad or dead channels. As always, most difficulties lied in (commercial) power supplies and connectors.

Although the LHC has not yet really started, that studies are well advanced to increase the maximum luminosity from 10^{34} $cm^2s^{-1}$to 10^{35} cm^2s^{-1}. The ten-time increase in pileup and radiation levels is very cumbersome for the tracking detectors, but as shown just above, the calorimeter can easily cope with this rate, provided no un-foreseen degradation happens on a component with radiation. In effect, all the technologies used are now obsolete and it could not be reproduced or redesigned. It will thus be important to start the R&D effort to redesign all the on-detector electronics, just to be ready in case of failure and we share a R&D program with BNL, Nevis, Munich to redesign the front-end in SiGe.

As the tracker will also need to be redone for SLHC, we joined the R&D program, led by Fermilab to study new technologies of 3D electronics.

CHAPTER 2

ATLAS ELECTRONIC CALIBRATION

1. Introduction

Traditionally, Liquid Argon calorimetry is *"uniform, stable and easy to calibrate"*. This last point compares to detectors with internal gain where the gain is always difficult to track. In liquid Argon, it is traditionally possible to inject an accurate electric charge that corresponds to the charge created by an electromagnetic shower and to equalize all the readout channels. This used to be done with calibrated capacitors and precise voltage steps in the previous experiments and no matter how the charge arrived, only the total charge counted.

In fast calorimetry this ceased to be true and the electronic calibration started being more difficult, all the more since the requirement on overall constant term was more stringent than before due to the high energies reached. In order to correct for readout non uniformities, the calibration pulse should

- ∞ Follow the same path as the physics (or ionization) signal
- ∞ Have a similar shape as the physics signal
- ∞ Be accurate to the precision requested by the energy resolution and distributed uniformly.

Besides, the calibration pulse is used to inter-calibrate the 3 gains of the readout and must thus be very linear and is used to correct for the non linearity of the readout chain.

Very early, it was recognized that the injection of a current signal through a resistor was much more convenient than through the traditional capacitor : it is easy and relatively inexpensive to buy 0.1% accuracy resistors which solved the always difficult problem encountered with the traditional injection capacitor. Moreover, the parallel noise was no longer a concern and it did not require elaborate circuitry to generate the correct signal shape. Concerning the signal shape, the fast shaping compared to the ionization signal duration did not require an accurate triangular shape and an exponential decay with the same time constant as the decay was found to be sufficient.. Two problems remained :

- ∞ Distribute the pulse uniformly over the 200 000 channels
- ∞ Generate high precision pulses over the 16 bits dynamic range

The first issue is addressed in §2. and the second in §3. and 4. as three versions of pulser have been made, starting from a 12 channel CAMAC version followed by a similar version ATLAS size but radiation soft for module 0, finished by the final radiation hard ATLAS version.

2. Pulse distribution

The first and determinant issue was to see whether a precise pulse could be brought inside the cryostat, right onto the electrodes without losing its accuracy or if the pulse had to be generated *in situ*.

2.1. Effect of cables

The main concern for a remote location of the pulse generator was of the course the cable that brought the signal inside, over several meters. In particular, is was well known especially after the work on the ØT preamps, that the cable characteristic impedance R_C could not be specified better than ±5% and that was difficult to measure better than a few percent [13]. If the cable had to be at the permil level it would have been hopeless. Fortunately, for the calibration pulse, the cable could be terminated on its characteristic impedance at both ends (which was not the case for the signal for noise problems) and in that case the voltage at the output depends only to the second order on the cable impedance. To be more precise, a voltage V_0 sent from a source impedance R_0 into the same load R_0 through a cable of impedance $R_C=R_O(1+x)$ with x « 1 gives a voltage V :

$$V = \frac{V_o}{2}\frac{1+x}{(1+x/2)^2} \approx \frac{V_o}{2}\left(1-\frac{x^2}{4}\right) \qquad (1)$$

This was of course a great relief, especially when some experimental measurements comforted it, as shown in Figure 33 and as expected a 5% *rms* dispersion on the cable impedance gives 0.1% on the amplitude. Another comforting measurement on the right plot was the amplitude at the end of a real bundle of cables, which remained within 0.1% at warm and at cold.

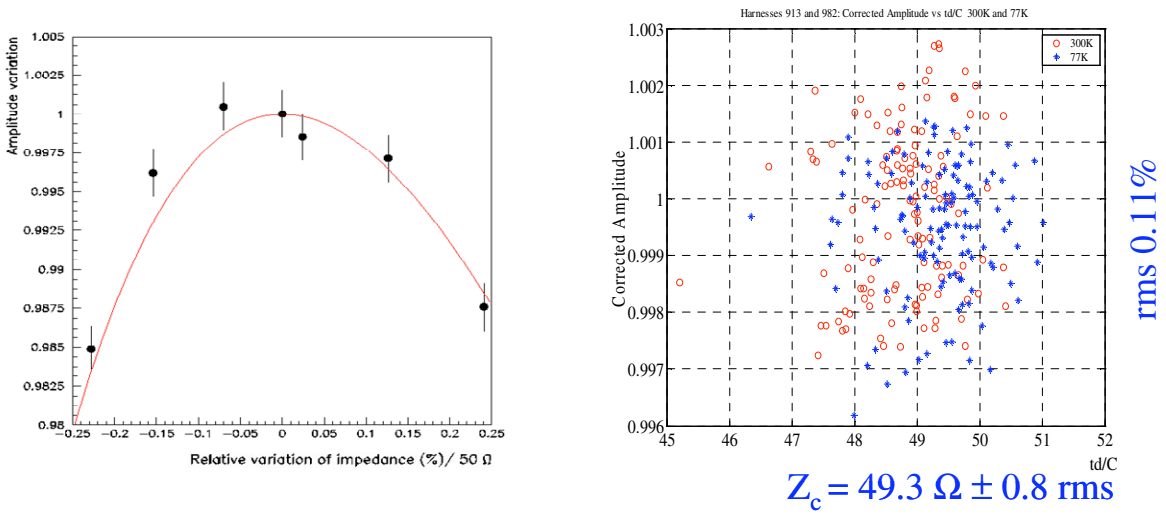


Figure 33. <u>Left</u> : signal amplitude at the end of a cable of mismatched impedance Rc terminated in 50Ω.
<u>Right</u> : signal amplitude at the end of a calibration bundle in the warm (red) and in the cold (blue)

In effect, if the cable impedance is a second order effect, the skin effect which is not negligible in these miniature coaxial cable, is a first order effect, which has to be corrected. This is illustrated in the measurement from Figure 34, performed with a bundle of the final ATLAS calibration cables. The amplitude is measured for different cables lengths at room temperature and in liquid nitrogen. The attenuation is well visible at room temperature for the longest cables (typically 5 m) and improves by almost a factor of 3 in the cold[29]. The propagation velocity also varies with temperature, but only by -3%.

∞

[29] This can be expected as the copper resistivity decreases from 1.8 to 0.25 from 300K to 77K, but the skin depth scales as the square root of the resistivity, giving a net effect improvement of 2.2.

The attenuation at warm and at cold have been fitted as straight lines, as shown in Figure 34, giving :

- T = 300 K dV/VdT = - 1.2%/K v = 5.50 ns/m
- T = 80 K dV/VdT = - 0.5 %/K v = 5.35 ns/m

It will thus be corrected off-line. After correction the overall dispersion of the calibration pulse amplitude has also been measured on 25 harnesses of 64 cables, giving an *rms* of 0.15%

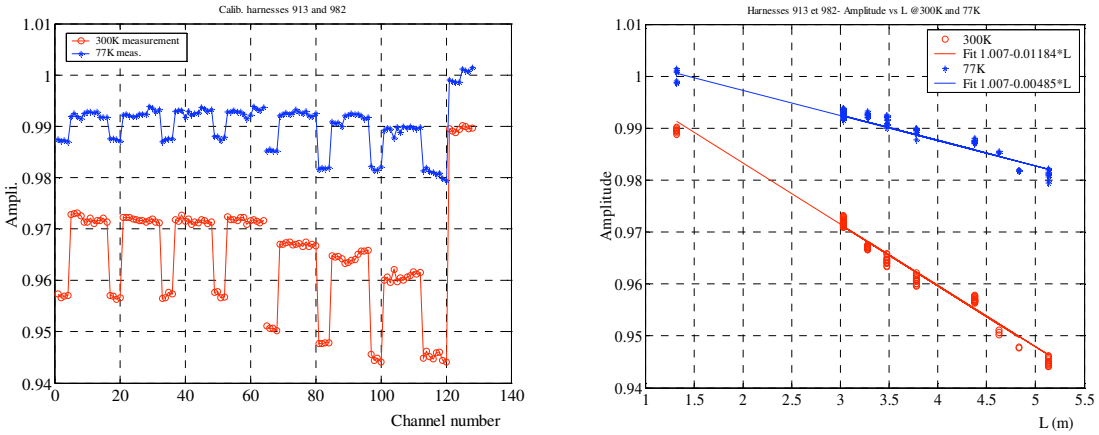


Figure 34. Left : calibration pulse amplitude at the end of the calibration harness, showing the attenuation due to skin effect in the warm (red) and in the cold (blue). Right : attenuation as a function of cable length warm and cold. The effect of several % needs to be corrected offline.

Several additional effects, worrisome with ‰ accuracies have been verified, in particular the effect of the feedthroughs and their 33 Ω characteristic impedance (Figure 35) and all the various connections. The simulations have shown that their effect was negligible, however once again their DC resistance came as a first order effect (typicaly 2 Ω in a 100 Ω chain) and resulted in a tight specification and quality control.

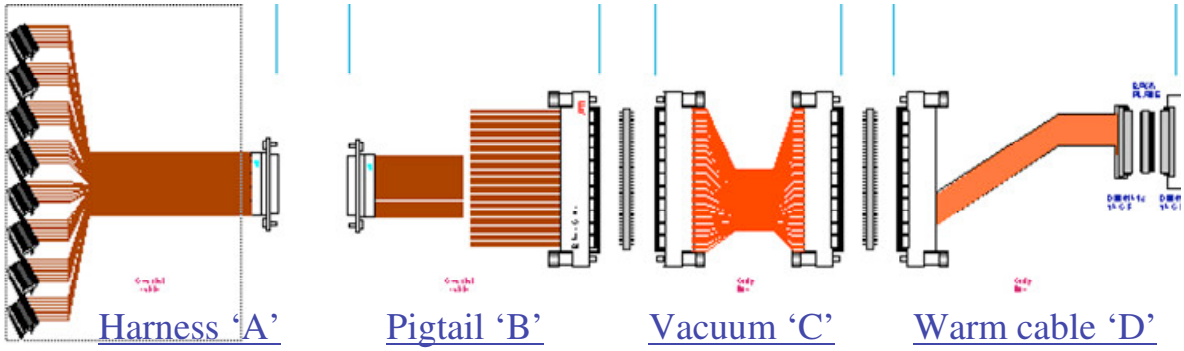


Figure 35 : synoptic diagram of the calibration signal path, made of several different cables : Harness A from motherboards to patch panel, Harness B form patch panel to feedthroughs, harness C inside the feedthrough and Harness D from Feedthrough to calibration boards

As usual, simulations are comforting but the real physicists believes only in (his) measurements and the calibration pulses were all measured on the mockup that was setup at BNL in april 2003 with the final calibration boards (Figure 36). Although the signal did not look so good at the end of the cable, all the waveforms were recorded, the LArG shaping was applied by software[30], the cable attenuation of -1%/m was corrected for and the result gave a uniformity of 0.44%, which should further improve in the cold.

[30] By a simple convolution with the impulse response of a CRRC² shaper with tau=25 ns.

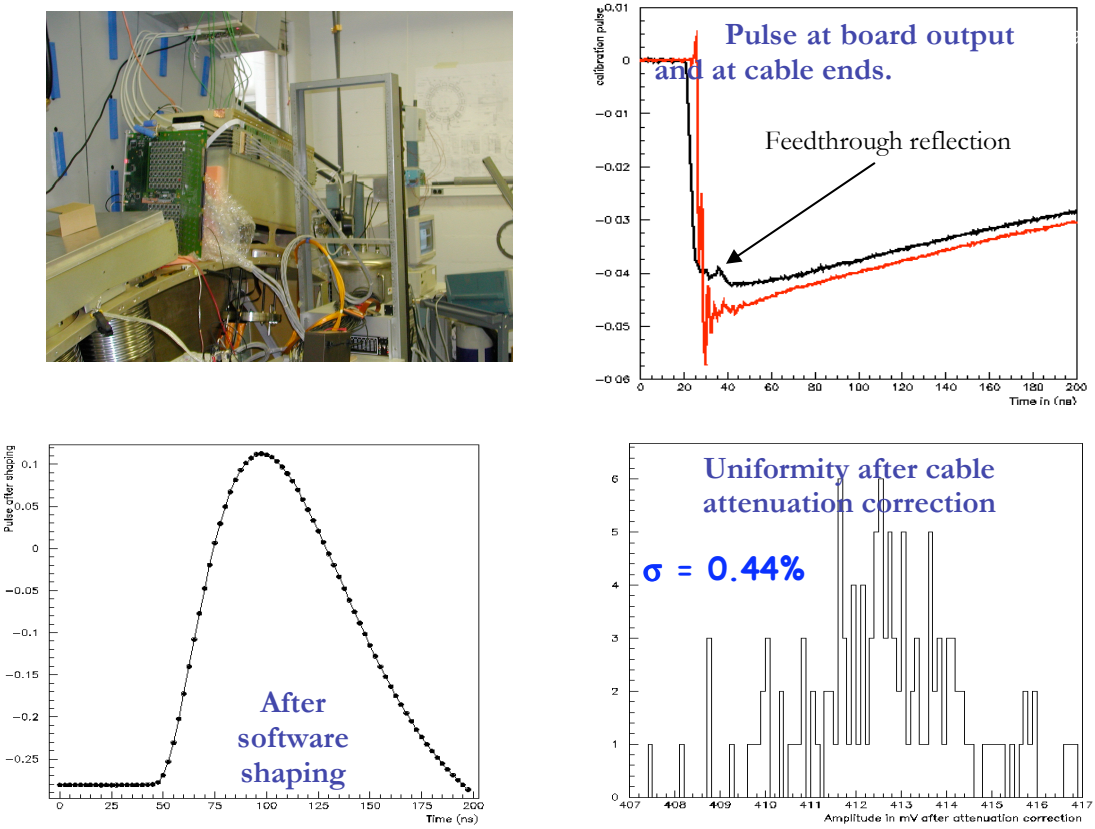


Figure 36: Overview of the calibration mockup at BNL (top left). Example of calibration pulse recorded at the beginning and end of the calibration distribution path. Pulse shape reconstructed after digital filtering simulating LAr readout chain and reconstructed amplitude uniformity

2.2. Pulse distribution on motherboards

Having an accurate pulse at the cable output is nice, but it still has to be delivered to several distant channels (Figure 37) through the calibration injection resistors R_{INJ}. As these are 3 kΩ, 1 kΩ and 500 Ω, 16 channels could be pulsed in the front and 8 in the middle or back (see Figure 7) for detector segmentation). These were grouped in resistive networks designed by BNL and produced by Sfernice with 0.1% accuracy and low temperature coefficient (-70 ppm).

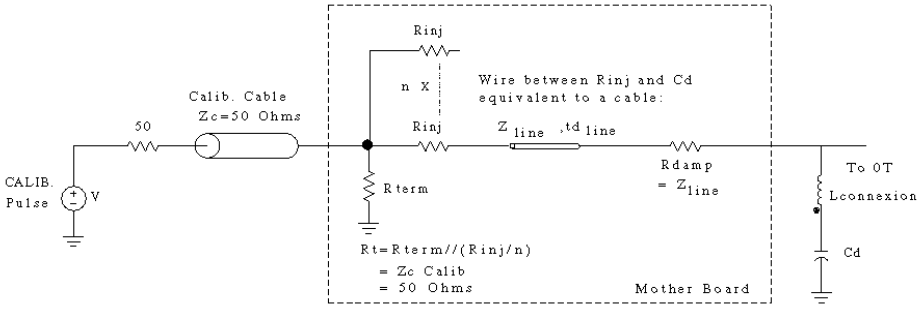
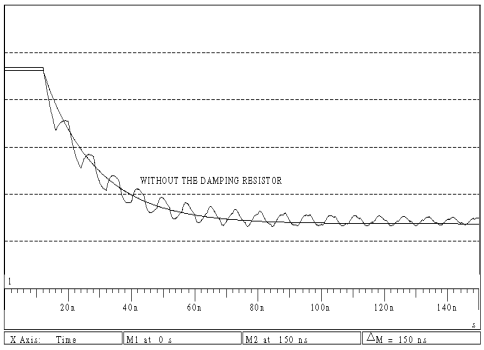


Figure 37 : principle of calibration pulse distribution. The calibration line is terminated by a resistor R_{TERM} and drives 8 to 16 injection resistors R_{INJ}. The lines on the motherboard that bring the calibration pulse to the detector are equalized in length and terminated in series at their receiving end by a 50 Ω resistor R_{DAMP}

The networks incorporate the injection resistor itself (R_{INJ}) and a termination resistor so that the input impedance of the network be precisely 50 Ω . Moreover, as the line on the PCB that connects the injection resistor to the detector is already a few ns long and is not terminated, it makes wiggles on the calibration pulse and it was necessary to add a damping resistor of its characteristic impedance 50 Ω at its receiving end called R_{DAMP}. The injection resitor is thus $R_{INJ}+R_{DAMP}$. Three types of networks have been produced with the following values (at cold) :



Front : 16 resistors of 2950 Ω and a termination resistor of 214.3 Ω

Middle A and Back : 8 resistors of 950 Ω and a termination resistor of 83.3 Ω

Middle B : 8 resistors of 550 Ω and a termination resistor of 250 Ω

The termination resistor value is a first effect on the signal amplitude (as well as the injection resistors). Hence, they have all been measured to 0.1% accuracy, including several times in-situ, on the feedthroughs with an automated developed setup developed in Orsay. A scanner board that plugged into the feedthroughs connectors allowed to scan all the channels through a GPIB interface and perform a three-points measurement[31] to reach the required accuracy.

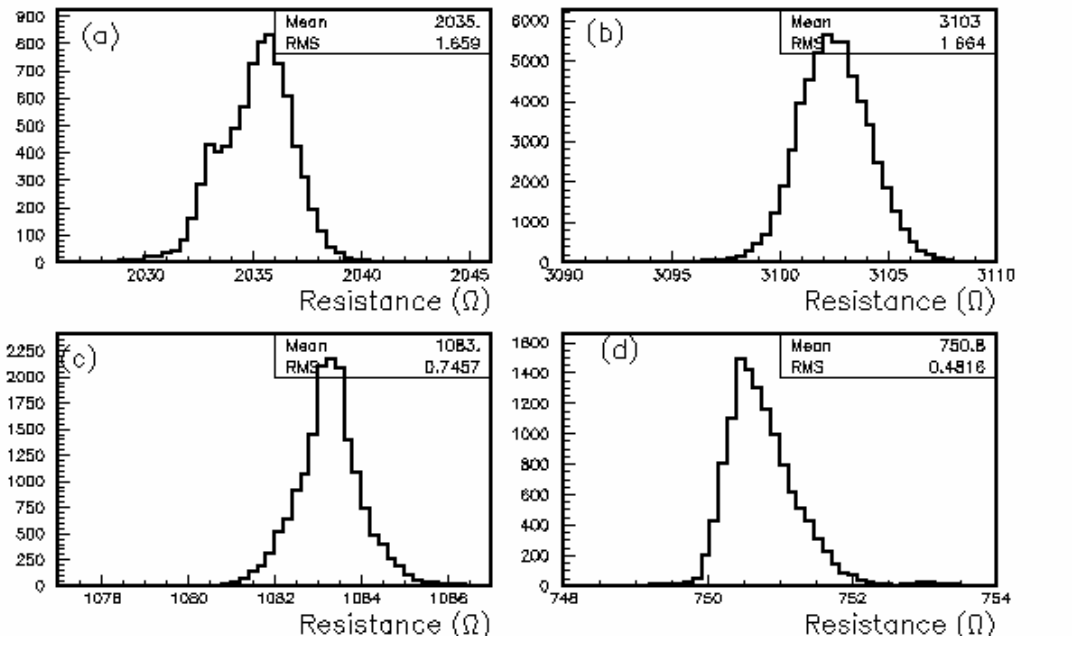


Figure 38 : measured values of calibration resistors in Presampler, Front, Middle and Back sections of the calorimeter. The dispersion is always lower than 0.1%, as requested.

Finally, the crosstalk was measured to be lower than 0.1%, dominated by low profile connectors, which is also a very important measurement (cf Chapter 3, section 3). Some faulty feedthroughs initially produced much larger crosstalk through the ground return impedance that would have rendered the calibration almost useless.

∞

[31] The DC current was injected with the calibration input and the resulting voltage was measured on each channel, producing a three-points measurement (the ground is common for both current and voltage probes).

3. Module 0 pulse generator design

The pulse generator aims at providing 1 ns risetime pulses up to 5 V in 50 Ω load with a 0.2% absolute accuracy or uniformity between channels, a dynamic range of 16 bits and a linearity at the 0.1% level. To cover the 16 bits, when the maximum pulse is 5 V, the minimum one (LSB) is around 80 μV. The pulse generator is derived from the H1 pulse generator designed by *B. Chase* and composed of a precision DC current source I_{DAC} transformed into a pulse by a High Frequency switch (Figure 39).

3.1. HF PNP switch

The pulse is made from a precise DC current I_{DAC} flowing into a 0.1% precision resistor R_0 = 50 Ω and when the current is cut, the voltage goes from $-R_0 I_{DAC}$ to 0 producing a negative steep voltage step. One important improvement was made by adding an inductor in parallel with the resistor R_0, producing the exponential pulse decay matched to the ionization current decay but also improving greatly the linearity as the voltage remains constant to almost zero when the current I_{DAC} is changing. The pulse is made by the inductor stored magnetic energy discharging into the resistor R_0. This was also important to minimize the power dissipated in R_0 which produces non linearity.

The pulse obtained is shown in Figure 40, with indeed a nanosecond fall time and a decay time given by the inductor of L = 10 μH, t_{CAL} = 320 ns, matched to the drift time in LAr. It can also be seen that the signal doesn't start from zero, but from a small DC value, given by the parasitic series resistance of the inductor R_L. However, this element does not change the absolute pulse amplitude[32] which is given only by I_{DAC} and R_0.

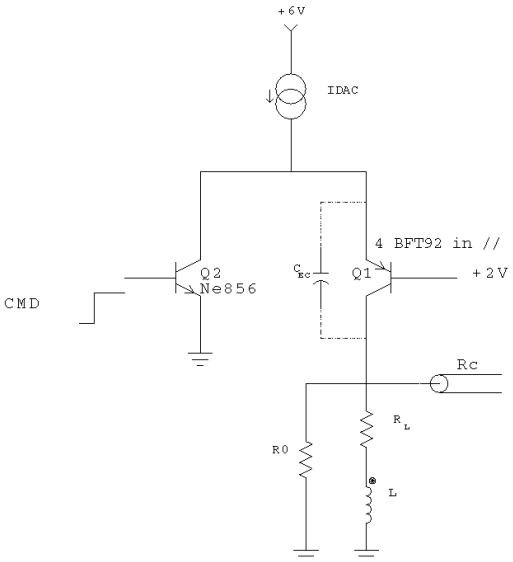


Figure 39: simplified schematic of the pulse generator

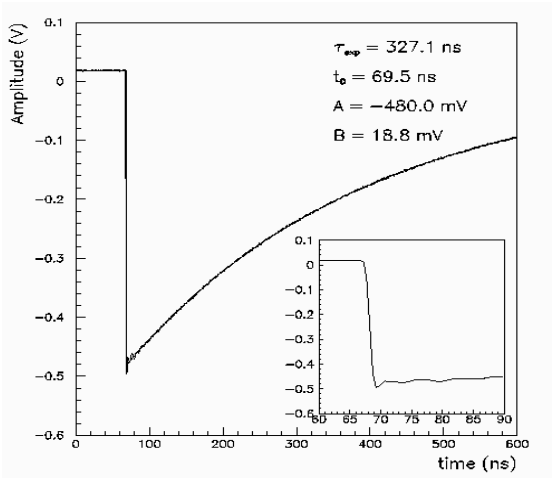


Figure 40 : calibration pulse shape

Indeed the pulse is defined by

- **Vout(t) = (R_L || R_0/2) I_{DAC} t<0**
- **Vout(t) = - R_0^2/4(R_L+R_0/2) I_{DAC} exp(-t/t_{cal}) t>0**

In which

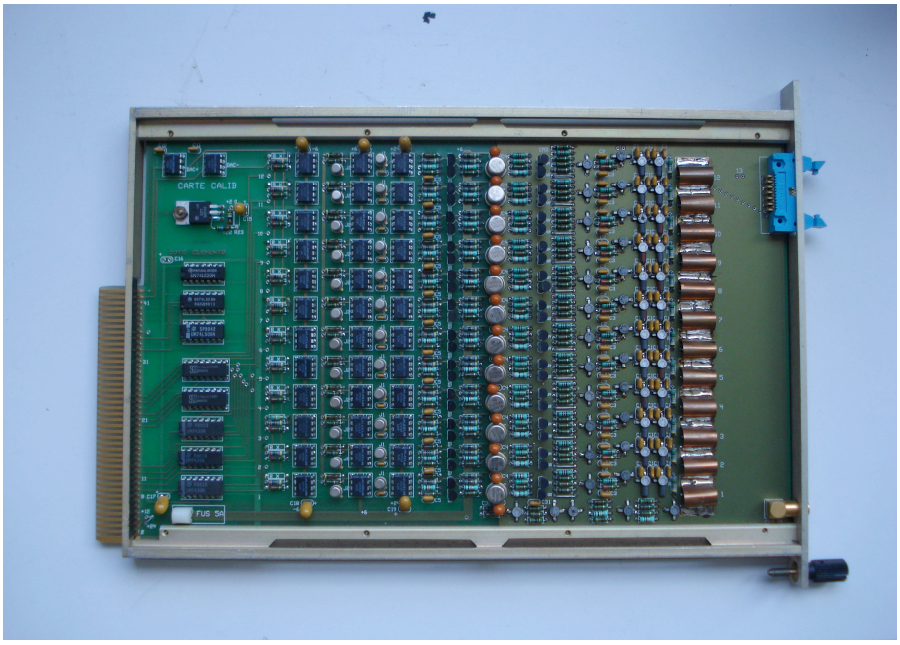
- R_0 = 50 Ω ± 0.1%
- R_L = 1.8 Ω ± 2%
- I_{DAC} = 3 μA - 200 mA
- t_{CAL} = 2L/R0 = 317 μs
- L = 9.3 μH ± 0.15

All these component values have been measured on the module 0 calibration boards described in the next section and dispersions are *rms* values on these measurements.

[32] The resistance is in series with the current generator loaded by R0/2, the voltage across R/2 is still I_{DAC}*R0/2. What changes is that the pulse does not start from 0V but from (RL//R0/2)*I_{DAC} but actually decays to 0V. This small change departure from a pure exponential pulse will be modelized in the pulse reconstruction

3.2. DC current source

The first design (Figure 41) was done in CAMAC in 1994 with discrete components for the test beam. The precision current source used commercial low-offset opamps. To produce 5 V into 25 Ω, the maximum current I_{DAC} needs to go up to 200 mA and power dissipation issues quickly become determinant. The current source is thus made around a 5 Ω precision resistor and an opamp regulating a DAC voltage up to 1 V across it. The DAC Least Significant Bit (LSB) is thus[33] 16 µV and it is important to use an opamp with an offset lower than this value, we used the OP07. As the HF switch was using bipolar transistors, it was necessary to compensate for their base current, which was measured in a separate branch and added to the reference current.



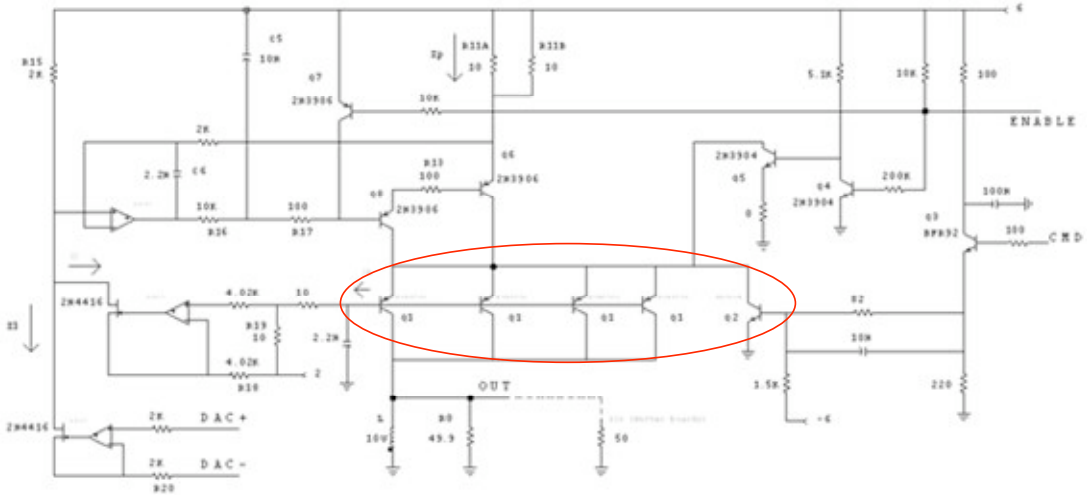


Figure 41 : photograph and detailed schematic of the first CAMAC calibration pulse generator used in the testbeam of the 2 m prototype in 1992-1994. The same schematic was kept for Module 0 calibration boards, but the apparition of surface mount components allowed to implement 128 channels on a 400x500 mm board.

[33] 1 V/65 536 = 16 µV

3.3. Module 0 board realization

The boards were the full ATLAS size (400x500 mm) and had to fit 128 channels. In order to be as uniform as possible, all the analogue channels were identical and fitting in a width of 5 mm to accommodate 64 channels on both sides, which was very challenging at the time[34]. As can be seen in Figure 42, a large area was taken by the inductors which needed to be 2 cm apart in order to make crosstalk by mutual inductance negligible.

The digital part had been designed by LAPP Annecy and was very ambitious. One could load a full sequence of calibration in FPGAs that would sequence the usual runs of loops on DAC values, patterns and number of trigger pulses.

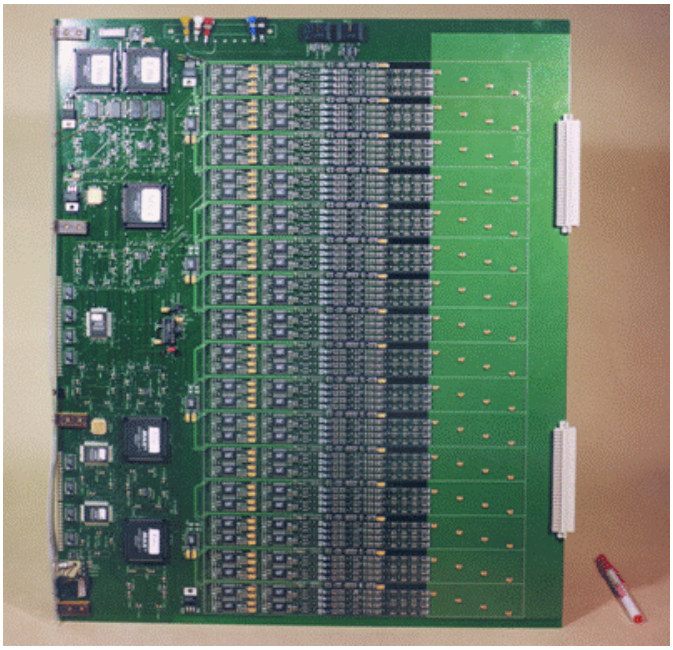


Figure 42 : module 0 Calibration boards

3.4. Performance

The performance of the system was good with a non linearity of 0.1% and an accuracy of 0.5%. Moreover, it has operated smoothly throughout the testbeam campaigns. As can be imagined, the difficulties were residing at the low end of the dynamic range : for very small DAC values, the pulse was not that small, as shown in Figure 43. There, two effects showed up :

∞ "Command Feedthru" : a positive spike appearing before the pulse and of opposite polarity. This corresponds to the command pulse that passes through the base-collector capacitance of Q2 before it turns on and that flows directly through Q1 into the load.

∞ "Parsitic Injected Charge" (PIC) due to the coupling of the emitter voltage step to the output via the base due to the base resistance and inductance in series[35]. This effect, relatively large as shown in Figure 43 will be explained in more detail in §4.2.3. , as some effort was undertaken to reduce it by one order of magnitude.

These two components, well visible without shaping are largely attenuated with the 50 ns ATLAS shaping. They partially compensate each other, although both are non linear. They corresponded *after shaping* to an injected charge of 1.8 pC, equivalent *at signal peak* to a pulse of 1 mV (0.02% of the full scale, or 4 DAC units or 1 GeV in the middle) when the DAC was set to zero.

∞

[34] Surface mount components were just coming out with and the PCB was at the limit of the fabrication standards.

[35] The base cannot be held perfectly constant at high frequency and moves during a short time

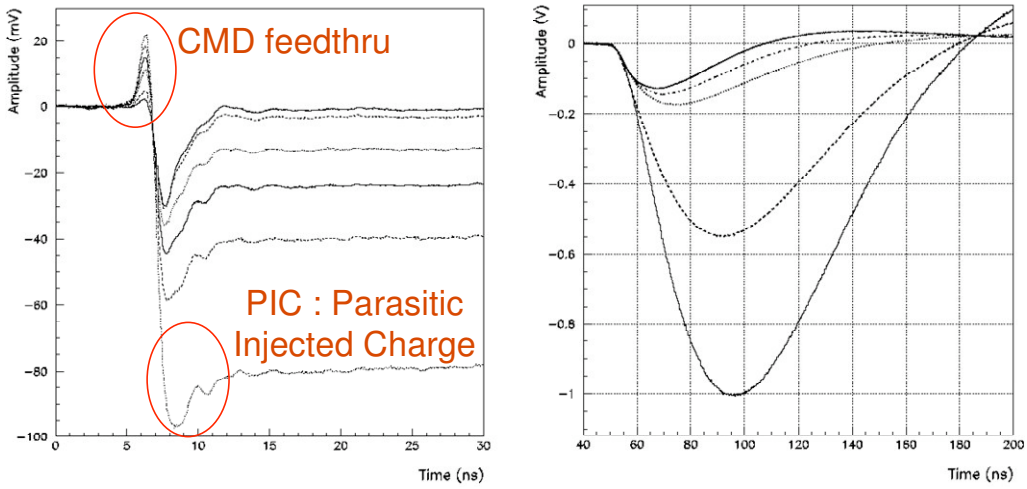


Figure 43. Left : calibration waveform at small DAC values without shaping. Right : same waveforms after shaping (right). Two parasitic effects degrade the pulse accuracy and produce a non zero signal at DAC=0.

The board uniformity was very good, at the ‰ level, as expected from the 5 resistors[36] at 0.1% level that determine the DC current. The pulse was measured on all the 128 channels of the 11 boards produced and are shown in Figure 44. It exhibited a dispersion of 0.18% *rms*, exceeding the requirement of 0.25%. It could be further improved to 0.11% when correcting for the small modulation visible in the uniformity plot and originates in the attenuation due to the difference of line length from the channel outputs to the connectors.

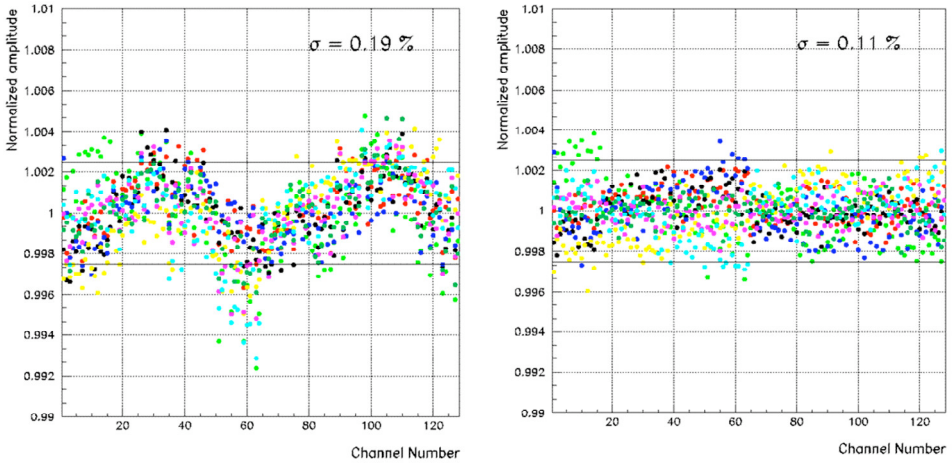


Figure 44: amplitude distribution over 128 channels of the 11 module 0 Calibration boards. The uniformity goes from 0.19% rms to 0.11% when the pulse is corrected for the output line on the PCB.

[36] The 50Ω termination, the two 10 Ω in parallel to make 5 Ω and two 1 k Ω resistors to transfer the DAC input from ground to the positive reference supply

4. ATLAS final calibration board (NIM paper [14])

From the experience of the module 0 calibration boards, designed to validate the concept, many changes have occurred in the design of the final calibration board in order to :

∞ Make the board radiation tolerant : it implied the design of radiation tolerant DAC chip, low offset Opamp chip and a digital 'universal' chip ("CALOGIC" designed by Annecy [4]) used for various functions using the DMIL technology[37]. The DMILL version of the delay chip, the TTCRx and the DMILL version of the SPAC slave have also to be implemented.

∞ Improve the parasitic injected charge by one order of magnitude whose level was about 1 GeV in the beam test calibration : The 4 PNP of the switch have been replaced by a PMOS and the parasitic inductance and capacitance on the switch have been minimized.

∞ Simplify the digital part in order to have easier debugging and external access to any action.

As shown in the simplified view of Figure 45, the overall schematic remains the same with the DC precision current source and the HF Switch. The HF switch has been moved to PMOS/NPN in order to reduce the injected charge and the use of PMOS has also simplified the schematic as it was no longer necessary to correct for the base current and only one low offset opamp was enough to make the precision current source.

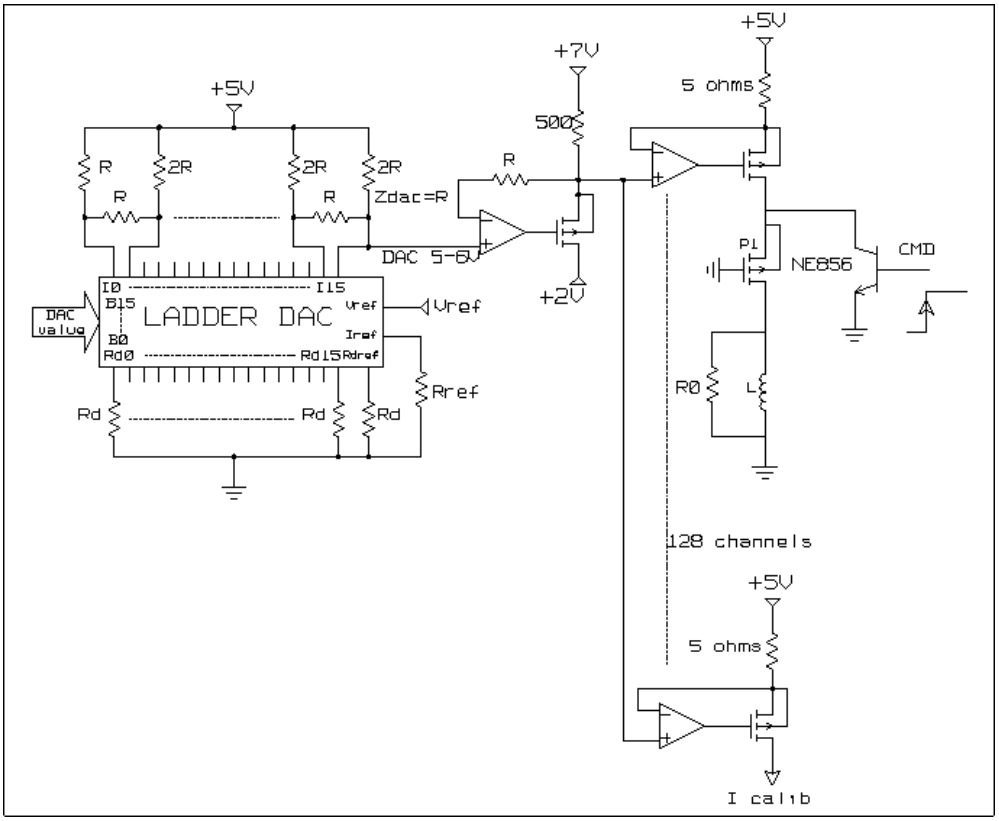


Figure 45 : overview schematic of the analog part of the final ATLAS calibration board

Sub-sections 4.1. 4.2. detail the analog ASICs realized in DMILL by Orsay. Subsection 4.3. 4.4. explains the difficulties encountered in the design and production of the 128 channels final board. Finally subsection 4.4. shows the overall performance obtained.

∞

[37] DMILL standing for "Durci Mixte sur Isolant Logico Linéaire" was a BiCMOS 0.8 µm Silicon on Insulator (SOI) semiconductor process developed for military applications by CEA and transferred to Matra for space/science applications.

4.1. DMILL DAC

The DAC was the first item that needed a custom ASIC as the commercial components failed very early under irradiation. Moreover, it had to be referred to the positive power supply of the current sources which is not standard. Finally, a full 16 bit accuracy was not really needed, but rather a 16 bit dynamic range and better than 10 bits accuracy. As there is only one DAC per board, a R-2R configuration with external 0.1% precision resistors was fine and had the advantage of good stability for the small signals, and in particular that with such configuration "zero DAC is zero voltage".

The architecture chosen (*cf* Figure 46) is an array of 16 identical switched current sources driven by a common reference source. To reduce the sensitivity to V_{BE} mismatch and variations with temperature the emitters of the current sources are strongly degenerated by 1.5 kΩ resistors (0.1% precision) which are also external. Each digital input is connected to two complementary MOS transistors (switches) which feed the collector current in the R/2R ladder. The PMOS transistor avoids that the base current of the mirror increases up to 1 mA ("floating" collector) when the NMOS is "off". The required logic levels (bits B0 → B15) must be equal to V_{DD} (+6V) and V_{SS} (+1V). In the first DMILL version, bipolar external translators have been implemented and have been integrated in the second version. The second version also improved the reference source as a current mirror was causing a slight degradation under gamma irradiation and has been replaced by a low offset opamp mounted in current source configuration. The reference 1.5 V input voltage is converted into a reference current with the same external 1.5 kΩ precision external resistor.

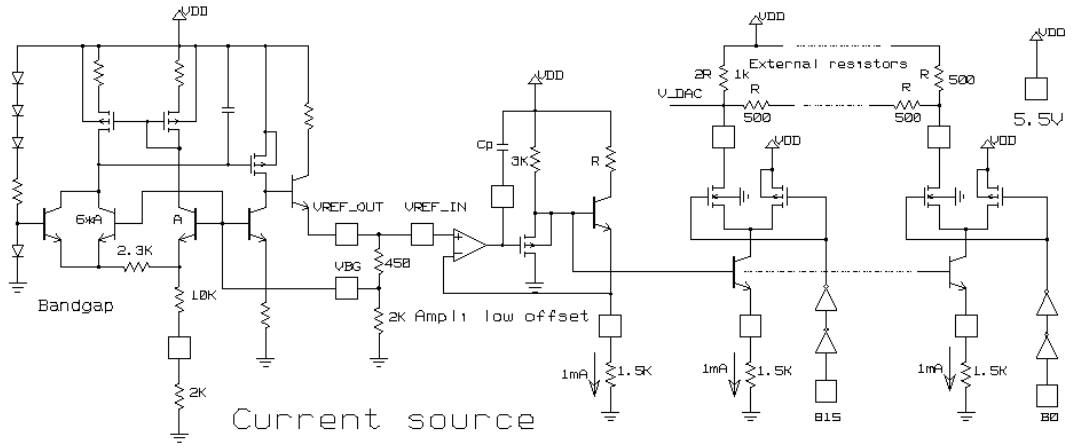


Figure 46: Schematic diagram of the 16 bit R-2R DAC

Performance : The performance of the chip has been measured in details on a dedicated testboard.

∞ Linearity : better than 0.01% on the three ranges : 0-10 mV, 0-100 mV and 0-1V corresponding to the gains 100, 10 and 1 in the readout (*cf.* Chapter 1, §3). On each individual bit, the precision is better than 0.1% or 1 LSB.

∞ Offset : < 2 μV for DAC = 0.

∞ Temperature sensitivity : - 50 ppm/K

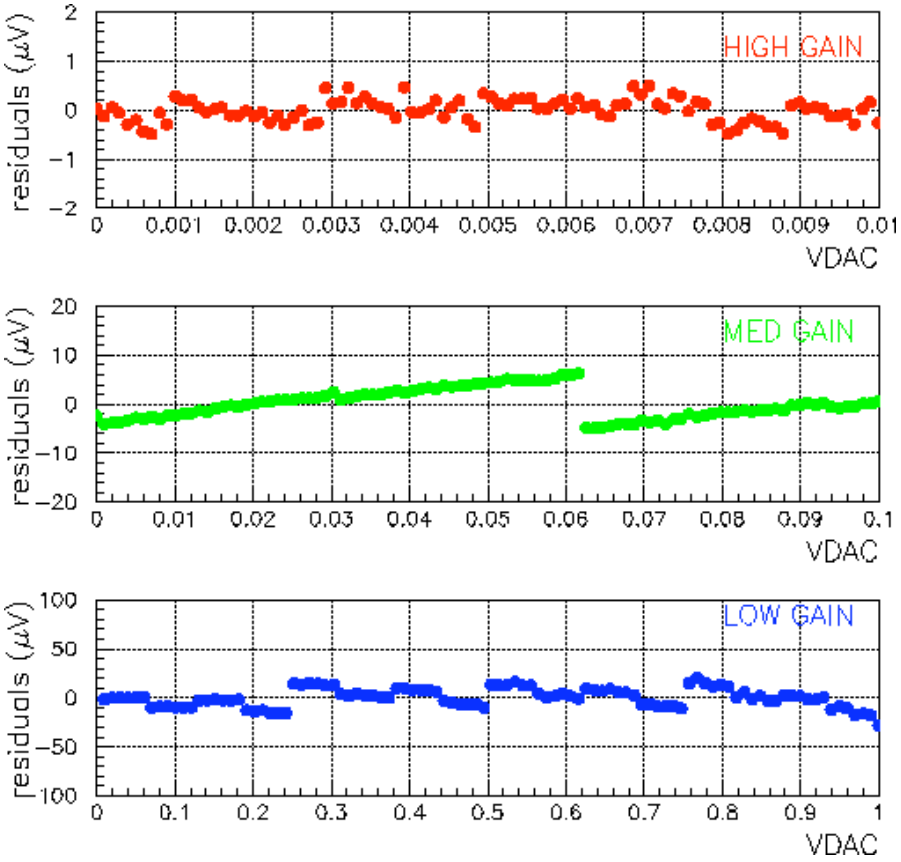


Figure 47 : DAC linearity on the three ranges 0.01, 0.1 and 1 V corresponding to the three gains 1-10-100 of the readout. In each case the non linearity is smaller than the requirement of 0.1%

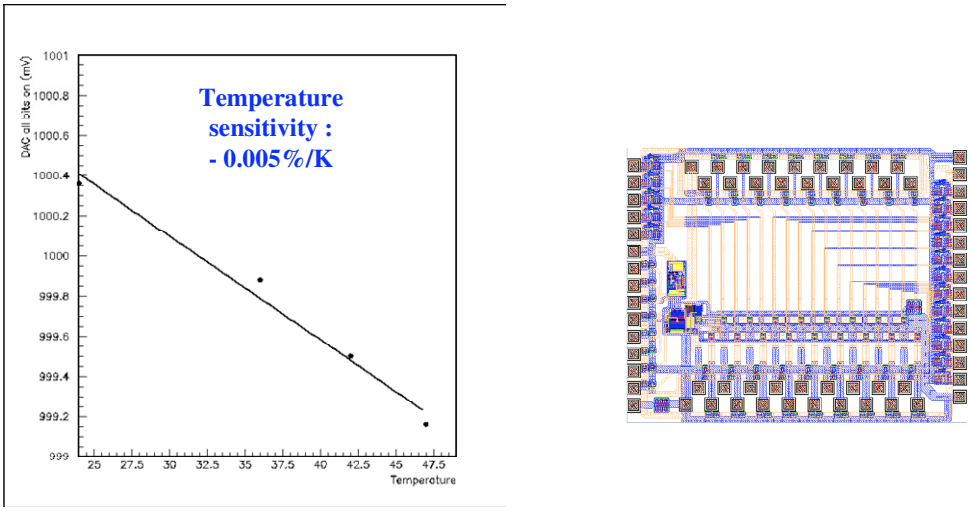
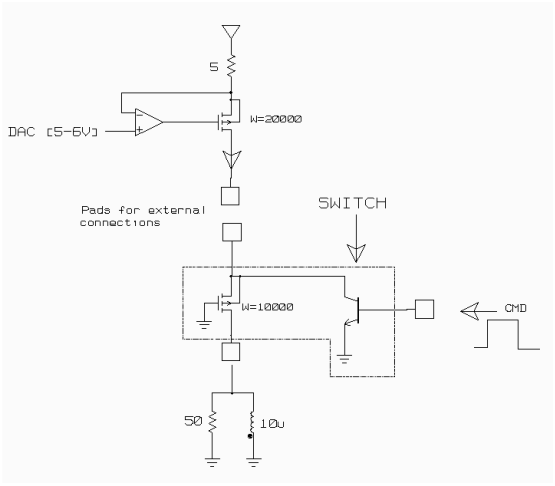


Figure 48 : temperature sensitivity measurement and chip layout

A fast characterization of the DAC sample received mid May 2002 has been done by checking that the tuning of the full dynamics range can be reached (1 V), measuring the LSB and the reference DC voltage when all bits are "off" to detect leakage current. Over the 123 chips measured, 112 were working correctly (90 % yield). Among the 11 which failed, eight showed a too large offset voltage when all bits are "off " (from 34.5 V up to 24 mV). The last three were not reaching the full dynamic range.

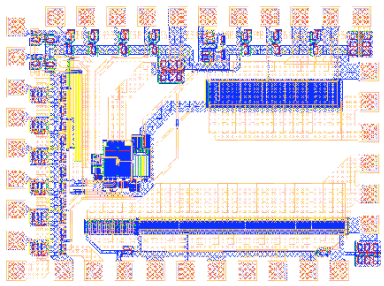
4.2. DMILL low offset opamp



The low offset operational amplifier is the key element needed to build the 128 precision DC current sources present on the calibration boards. It is also used to distribute the DAC voltage throughout the board with minimal voltage drop. The voltage to current conversion is based upon the low-offset Opamp and a 0.1% 5 Ω external resistor. The Opamp offset should be small enough compared to the signal (typically around one DAC LSB = 15.26 V) so that its contribution to the voltage output response uniformity be negligible and the full dynamic range be reachable. Moreover this offset is supposed to be stable in time and against radiation level in ATLAS. In the beam test calibration board version, OP497 were used. Many commercial low offset Opamp have been tested under neutron and gamma irradiation, but their offset voltage and their bias current showed large variations, making them inadequate for use in LHC environment.

Two different approaches were first followed : a CMOS auto-zero Opamp, and a bipolar static low offset Opamp with external precision components and bits to trim down the offset to the specified accuracy. Versions of these two chips were first submitted to AMS 0.8 µm BiCMOS to validate the concept and finally it was decided to continue only with the second option and migrate the design of the static Opamp to a DMILL ASIC, which performed as expected.

A second iteration was decided in summer 2001 to include[38] the HF switch which turns the DC current into the fast LAr-like pulse. The HF switch is a simple PMOS/NPN pair as the PMOS was shown to strongly improve the parasitic injected charge with respect to the PNP used in the beam test calibration board. This modification also reduced the cost of the calibration board.



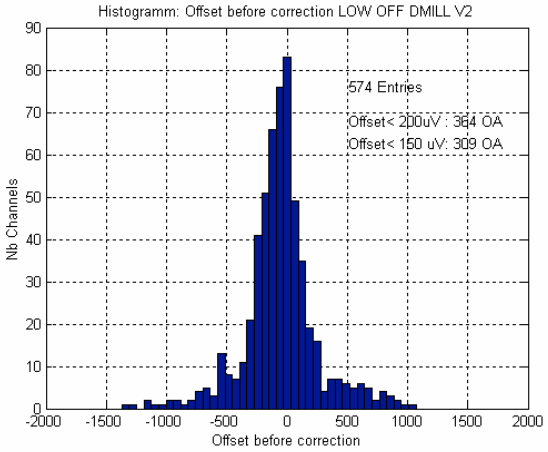


Figure 49: Low offset opamp layout in DMILL technology (left). Offset distribution before trimming (right). Only the chips within 250 µV were trimmed to15 µV, giving a yield of 60%.

[38] It has been realized lately that the dielectric isolation of the DMILL process allows to incorporate these components which operate with very different voltages than the Opamp

4.2.1. Principle/design of the low offset Opamp

As shown in Figure 50, the circuit is built around a bipolar differential pair and external precision collector resistors (165 kΩ 0.1%). The transistors are 10*1.2 NPN, mounted in centroid configuration[39]. This input stage provides a gain of 127, large enough to disregard the second stage offset. The chips are sorted to be within ± 150 V from the original distribution shown in Figure 49

The second stage is built around a cascoded PMOS (1000/0.8 μm) differential pair, again in a centroid configuration. A bank of 5 binary scaled current sources allows to add or remove up to 20% of the static current[40] and allow further trimming down to ±10 V over a ±250 V range. The total open loop gain is 80 000, in good agreement between measurements and simulation.

The output stage is a large (20,000/0.8) PMOS in order to drive the large maximum output current (200 mA). An enable input allows to turn off the current when the channel is disabled with an internal PMOS which connects the gate to +5 V. The gate is also brought out to connect a compensating capacitor in order to ensure good stability.

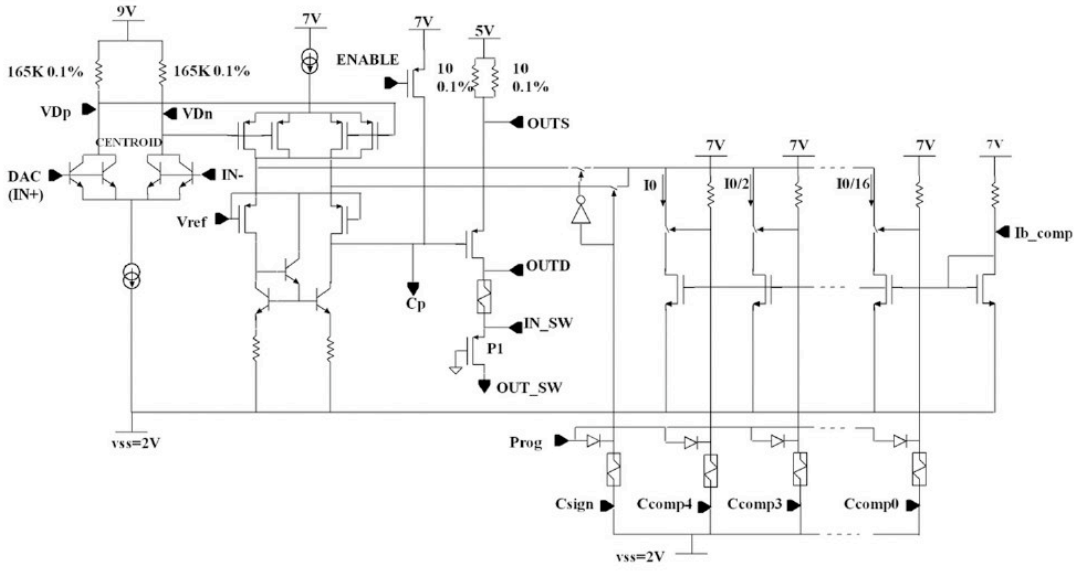


Figure 50: schematic diagram of the DMILL low offset opamp used to generate the precise DC calibration current I_{DAC}. The HF frequency switch also integrated in the chip is not shown on this schematic

4.2.2. Performance of the low offset Opamp

More than 32,000 circuits have been produced for ATLAS and packaged in PQFP44 plastic package. They were tested with the robot described in Chapter 1 §3. The offset was the main selection criterium and around 60% of the chips had it within a ±300 V window, slightly worse than the first iteration and the AMS version. They have then been trimmed down to 15 μV by burning the fuses.

The sensitivity of the offset to the temperature has been measured on ten chips before trimming and the largest variation, < 2 V per degree is observed for the Opamps with the largest offsets, which do not satisfy anyway the selection criteria. The offset of these chips has been trimmed down to their minimal value with the fuses. These chips have been kept at 87 degrees during 4 days in an oven and one chip has

∞

[39] a larger transistor size would in principle further reduce the offset, but would decrease the radiation hardness due to too low a current density

[40] This fraction is determined by an external resistor

been measured regularly. The offset stability has been found smaller than 2 V over this time period and this measurement shows also the fuses robustness.

The first version of the chip (which included only the low offset Opamp, not the HF switch) was tested under irradiation first to gammas (^{60}Co at Pagure, Saclay), then to 10 MeV neutrons at CERI (Orléans). The output current of ten chips was monitored during the irradiation. The results are presented in Figure 51 and have shown stable operation up to the Radiation Tolerance Criteria[41] (RTC) for DMILL chips in the Front-End crate of 52 kRad.. The test to neutrons was performed far in excess of the RTC_{NIEL} (up to 9.10^{13} Neutrons/cm^2 instead of $1.6\ 10^{13}$ Neutrons/cm^2). After $2.5\ 10^{13}$ the circuits could not longer be measured on line because of the failure of a discrete NPN transistor commanding the multiplexing relays. Notwithstanding, the offsets of the circuits were measured again after the irradiation and the maximum change was found to be 50 V for a chip exposed to the maximum flux.

In ATLAS, the stability of the offset of the Opamps (and the amplitude of the parasitic injected charge) could be monitored by studying the time variation of the constant term of the fit of the response of the electronics channels in the high gain connected to a given calibration channel [3].

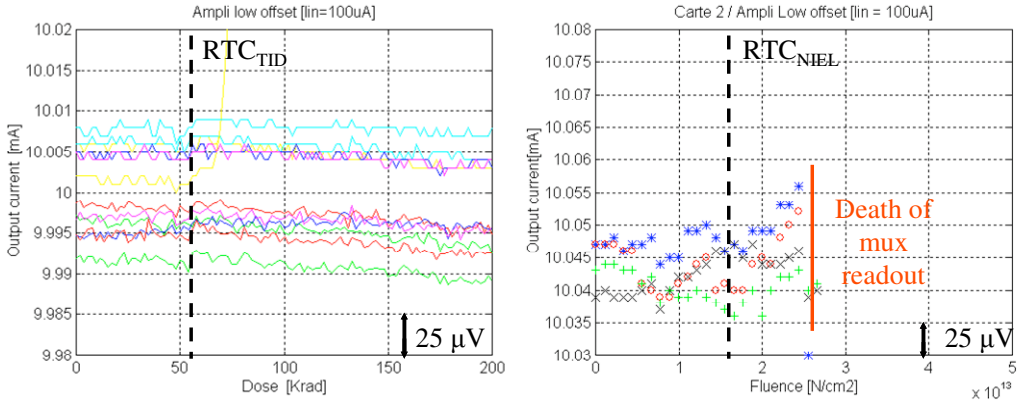


Figure 51: output current as a function of gamma dose (left) and neutron fluence (right). The opamp is stable within 25µV in excess of the radiation dose requested for ATLAS LAr.

4.2.3. Performances of the HF switch

The small signal obtained when setting DAC = 0 (or close to zero) is referred to as "parasitic injected charge" (cf §3.4). It can be quantified after shaping in DAC units at its peak or at the signal peak. In the testbeam module 0 boards, it amounted to an impulse of 1 pC, equivalent to 0.3 mV DAC (200 UDAC) or 1.2 GeV in the e.m. middle section.

This parasitic charge injection is due to the parasitic inductance between the PMOS and the NE856, which makes a resonant circuit with the gate-source capacitance (C_{GS} ~20 pF). By adding external inductors, it is possible to extract the residual inductance via the resonant frequency of the wriggles and a value of 3 nH is found (*cf.* Figure 52). Attempts to bring this value further down by integrating the NPN transistor have been jeopardized by other parasitic effects which led to worse performance.

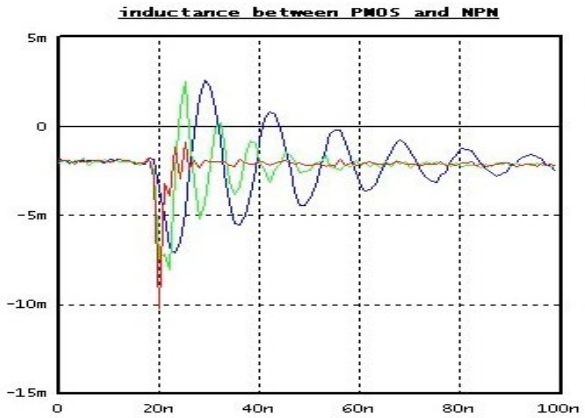


Figure 52 : calibration waveform at DAC=0 for various gate inductors (0-30 nH)

∞

[41] The RTC was defined as the simulated dose in 10 years multiply by several safety factors (5 for simulation accuracy) and 1.5 in DMIL for lot variation

In principle, the parasitic injected charge can also be decreased by decreasing the gate voltage. Indeed, it is observed that it scales linearly with V_{GS}. However, some channels could no longer be switched completely off when V_{GS} was below –0.4 V. Furthermore, the gate connection to ground must be as low inductance as possible and the parasitic inductance of a decoupling capacitor adds visible ringings. It has thus been decided to connect the gate firmly to ground.

However, some improvement could be obtained in lowering V_{GS} at a given current by reducing the effective threshold voltage V_T through the N-well voltage biasing scheme. It was previously tied to +6V to minimize body effects and tying it (in DC) to the source reduces V_{GS} from 1.2 V to 0.6 V typically, bringing a factor of two improvement to the PIC. It also reduces the source voltage at large current, allowing to lower the power supplies by 0.5 V and thus the power dissipation.

After these modifications, the PIC amounts typically at its peak to 100 µV after shaping, corresponding to the 50 MeV noise level.

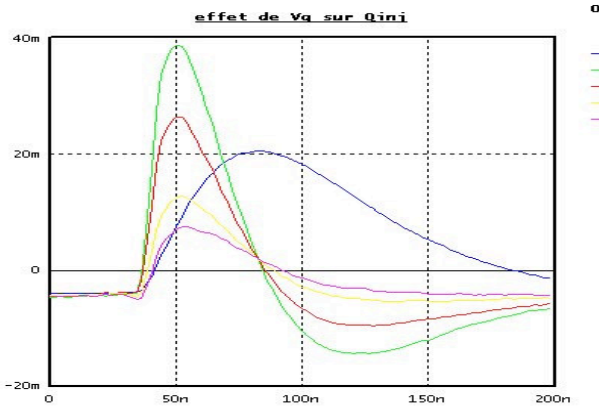


Figure 53: parasitic injection charge after shaping for various Nwell voltages V_B. Green curve : V_B=5V, yellow curve V_B=V_{DS}=1V

4.3. 8channel board design

The 8 channels board (Figure 54) was designed to be 1/16th of the final board. Due to the size of the Opamps Package, the board layout is very different from the radiation soft board used in module 0 tests. In particular, on the previous board, all the outputs were aligned in a single row, on both sides of the board, with a pitch of 6 mm. The new Opamp PQFP44 package exhibits a foot print of 14x14 mm which forces the channels to be staged in the board depth. Consequently, the large command signal (CMD) which fires the pulses could no longer be well separated from the sensitive output signals. Most of the problems experienced on the new prototype stem from this new layout and were not seen on the single channel test boards.

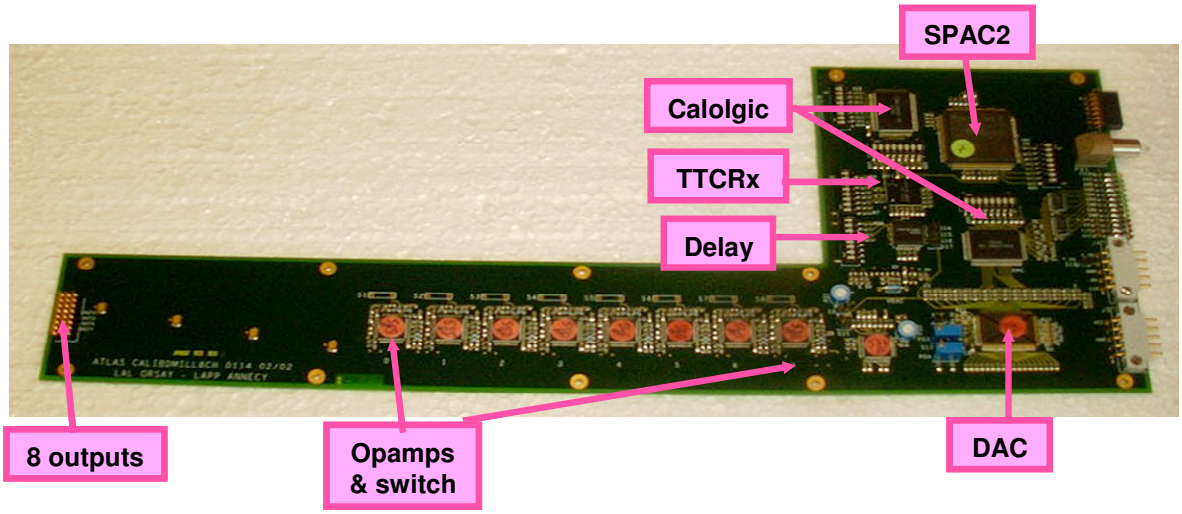


Figure 54 : Picture of the 8 channels board. The size of the board is ATLAS –like from the front panel to the output connectors. All chips are located on the same side of the board on contrary to the beam test board. Only passive components and transistors are located of the other side. The board is a 8 layers PCB.

Many unexpected problems appeared on this new layout, due to the new disposition of the components and coupling between digital and small analog signals. A short summary is given below :

∞ the DAC gave a much worse linearity in the low gain, which was traced to the large current drawn on the +5V which was affecting the external voltage reference value taken from this supply. It has been fixed by taking the reference from a different supply and the results are now in agreement with the measurements done on dedicated board. Also care must be taken to have a true star configuration for the reference voltage and ground so that no common mode current can create an unwanted voltage drop on the reference resistors.

∞ The output current deviated from linearity by 0.5% in the large 200 mA output range due to the poor temperature coefficient of the 5 Ω surface mount resistor.

∞ The pulse was not uniform to 0.2%. It had been scaled across the board in order to compensate the attenuation due to the output lines. The difference in length between CH0 and CH7 is around 17 cm which gives a difference of resistance[42] of 0.4 Ω for a 200 µm wide 50 Ω stripline. Uncorrected for, it would lead to a difference of 0.8% on pulse amplitude. Therefore, the lines bringing the +5V have been designed with variable lengths to compensate this effect with a width of 2 mm giving a resistance variation of 40 mΩ. The measured resistance turned out to be more around 60 mΩ, resulting in an overcompensated pulse.

∞ "Ground bounce" : a 1 mV, 100 ns wriggle is superposed to the pulse. It is even present when there is no pulse or when the channel is OFF. This wriggle is particularly annoying as it sits in the middle of the shaper bandpass. It is also more pronounced in the channels far away from the output and disappears when the R0 termination resistor is removed. It can be explained by the large (200 mA) current flowing in the ground from the CMD pulse and the non zero impedance of the ground plane. Small ground voltage differences appear across the board and are coupled to the outputs by the resistors R_0.

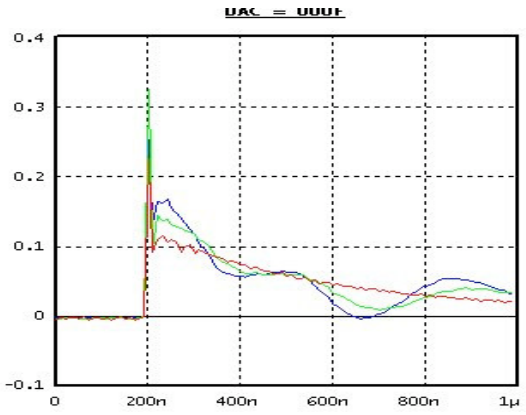


Figure 55: ground bounce due to digital signal coupling

∞ It has therefore been decided to move R0 close to the inductors to leave the current source high impedance and avoid to couple ground noise. However, it produces a visible overshoot as shown in Figure 56: the line from the switch to the resistor was 50 Ω and is now terminated by 25 Ω. This produces an overshoot well visible on the waveforms and well predicted by the simulation. It can be removed totally by redrawing the line to be 25 Ω. In order to further minimize the impact of an impedance mismatch for the line, all channels have been equalized in length for the output lines.

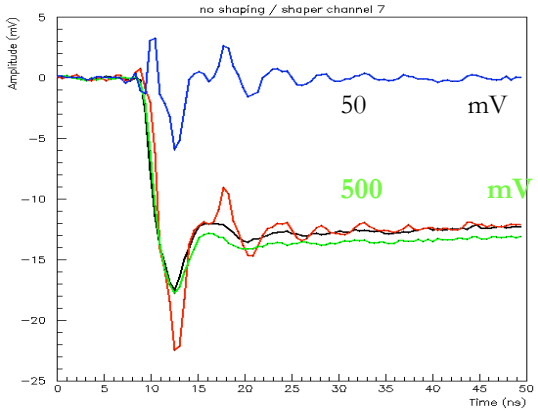


Figure 56: effect of termination resistor location

∞ Robustness : This issue had been completely overlooked and it was realized by chance that some faulty conditions had a large impact that could be easily prevented. The effect of missing power supplies has been studied as it sometimes led to having the maximum current (300 mA) flowing continuously in the opamp. A few additional external components allowed to shut down the amplifier when power supplies were missing. Individual 100 Ω series protection resistors have also been included in all the input and reference voltage busses (Vref, DAC, Vdd).

∞

[42] For 35 µm thickness copper, the resistance is 0.5 mΩ/ at room temperature.

4.4. 128 Channel Final calibration board

4.4.1. Board design

The 128 channel final calibration board is not only a 16 times replication of the 8 channel board presented above : more than 100 modifications had been necessary after the measurements of the 8 channel board and were presented to the Final Design Review in june 2002. The digital part, common to the whole board is routed on the right side of the board and the DAC is in the middle in order to minimize the effects of DAC distribution already noticeable on the 8-channel board. In particular, the VP5 "star" reference point for the DAC has received a lot of attention in the routing and all the channels are individually routed to this point, with lines equalized in length, with minimal resistance (<50 mΩ) to avoid dispersion. The lines were 400 mm long and 4 mm wide with special 70 µm copper thickness, 6 layers were necessary to route these lines.

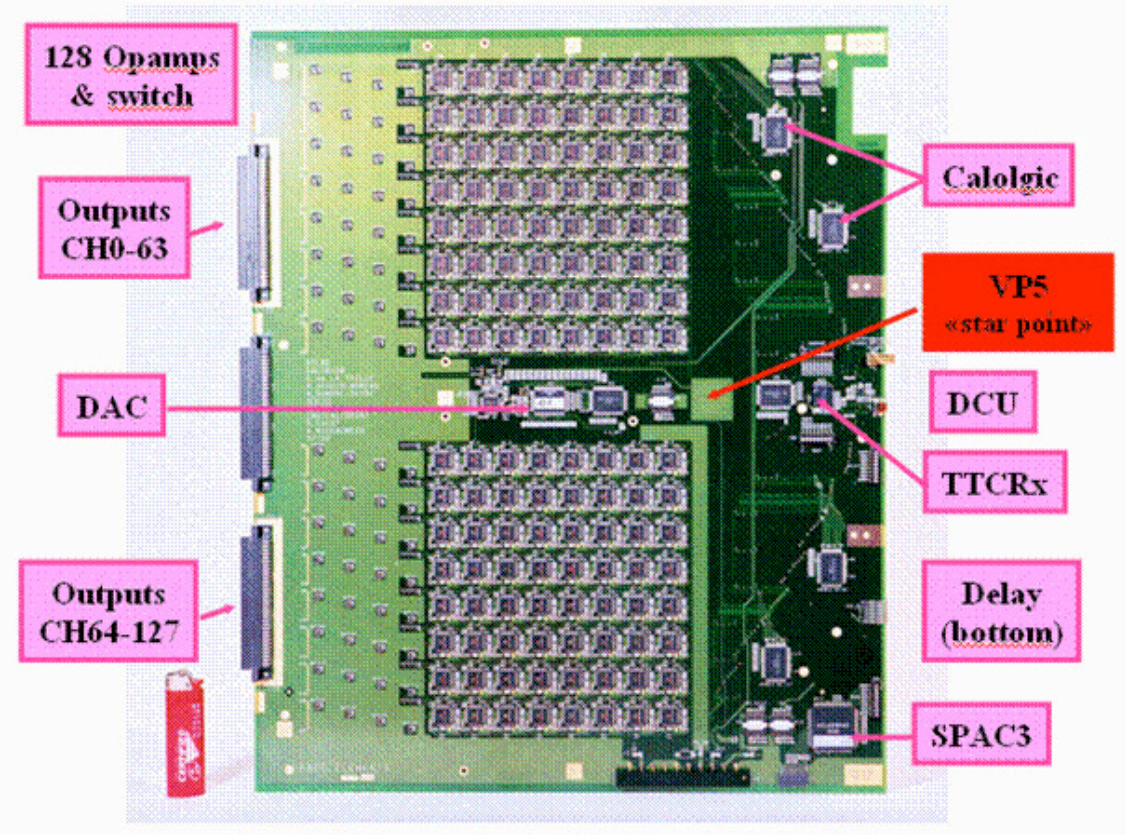


Figure 57: view of the top side of the final calibration board displaying the 128 pulsing units and common control chips.

The routing of the PCB had been very tricky to minimize the interference of the digital signal on the low amplitude analog ones. The cross section of the board is shown in Figure 58.

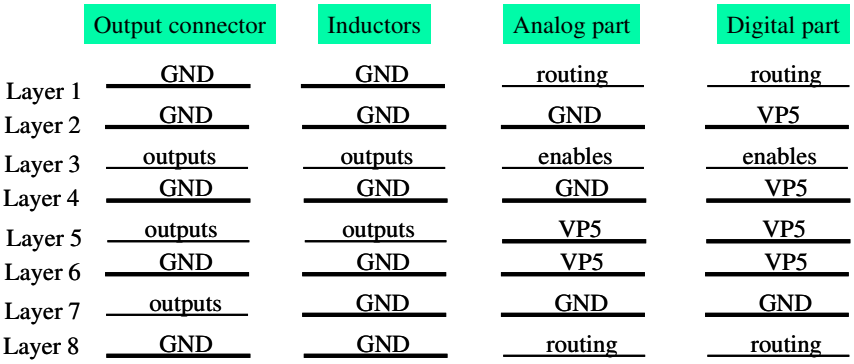


Figure 58 : cross section of the printed circuit board showing the layer assignment on the various areas

4.4.2. Board performance

∞ DC linearity:

The measurement of the DC current I_{CAL} has been performed on the 3 scales of the ATLAS readout shaper (High gain G=100, Medium gain G=10, Low gain G=1) as a function of the DAC set (in DAC units from 0 to 65535). This corresponds to DAC ranges of 0-10 mV, 0-100 mV 0-1 V and output DC currents of 0-2 mA, 0-20 mA and 0-200 mA. The DAC full scale is 1 V and one LSB corresponds to 15 µV.

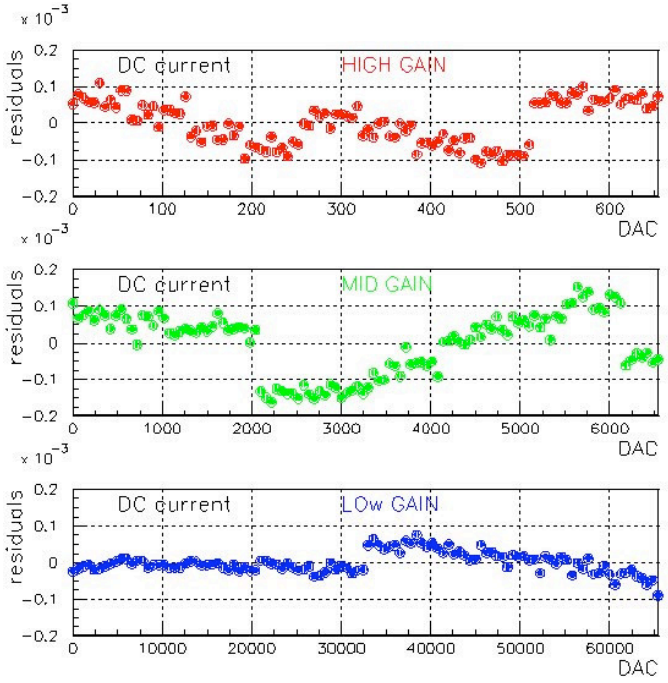


Figure 59: DC linearity of the DC current on the 3 scales (in ‰)

The results are summarized in Table 1 and in Figure 59. The residuals (data-fit)/data are plotted normalized to *each* full scale. They do not exceed 10^{-4}, corresponding to DAC = 1 µV (0.07 DAC LSB) in the high gain, 10 µV (0.7 LSB) in the medium gain and 50 µV (6.7 LSB) in the low gain and show a similar pattern as the DAC residuals. The small variation of slope in the three gains (3.008, 3.0056 and 3.0056) can be due to the change of full range on the amp-meter or a small bias of the linear fit.

IDC/DAC	P0	P1	RMS
High Gain	2.5 µA	3.0080 µA/DAC	58 ppm
Mid Gain	7.1 µA	3.0056 µA/DAC	85 ppm
Low Gain	6.7 µA	3.0056 µA/DAC	28 ppm

Table 1. Pedestal, slope and rms of the residuals of the linear fit of the calibration DC current I_{CAL} over the three shaper gains.

∞ DC uniformity :

The DC current uniformity has been measured for the 128 channels at the full scale of the High gain and Medium gain and is presented in Figure 60. The average and dispersion are summarized in Table 2. The non uniformity in high gain is dominated by the Opamp offsets (around 2 µA = 0.7 LSB) with a dispersion of 0.14% which is halved after correction. The average value at DAC=0 is equivalent to an average Opamp offset of 22.5 µV (mainly attributed to the DAC distribution Opamp[43]) and a dispersion of 11 µV *rms*.

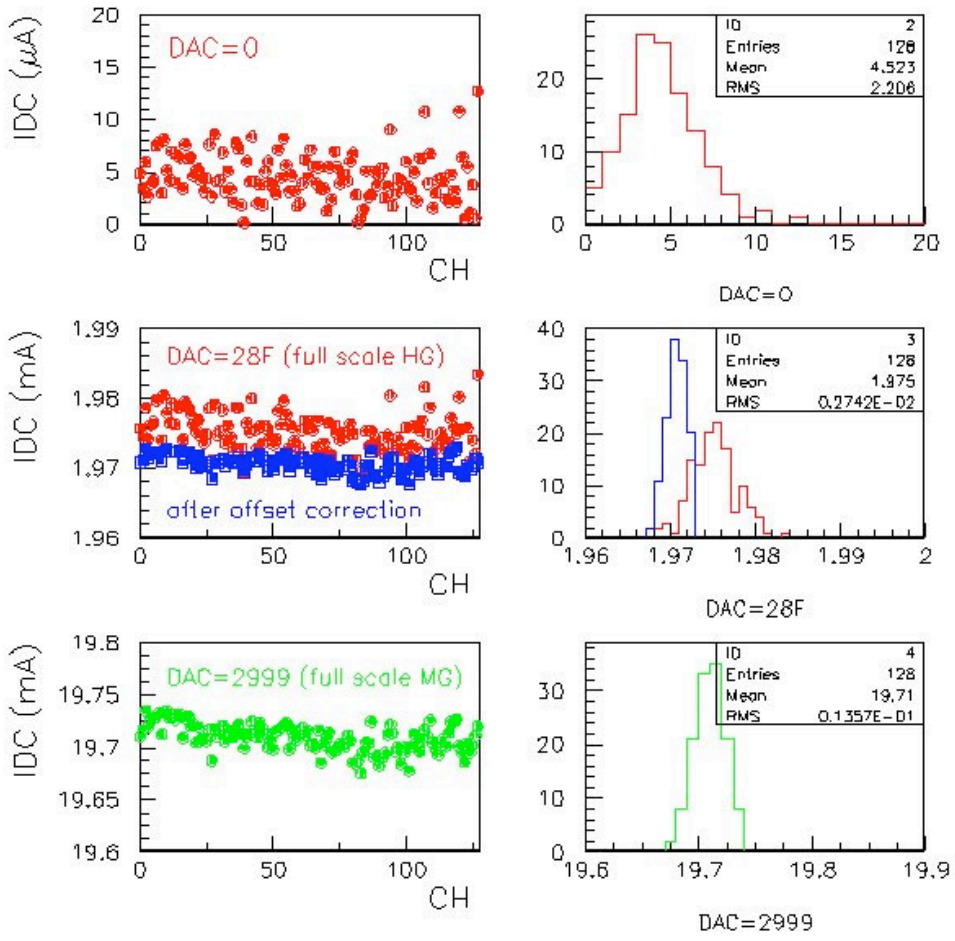


Figure 60: dispersion of the output DC current of the 128 channels for DAC=0 and for ranges 0-2 mA and 0-20 mA.

In the Medium gain, the offsets are no longer visible and the dispersion amounts to a similar value, dominated by the accuracy on the discrete components (5 Ω resistors)

	AVG	RMS	%
DAC = 0	4.52 µA	2.2 µA	
DAC=10 mV raw	1.975 mA	2.74 µA	0.14%
DAC=10 mV corr.	1.971 mA	1.5 µA	0.07%
DAC=100 mV	19.71 mA	13.3 µA	0.067%

∞

[43] A non zero-centered general offset is necessary so that all current sources be properly biased at DAC=0, otherwise a change in pulse shape is observed when the transistors reach their correct bias, resulting in non-linearity.

∞ Waveforms :

The pulse at the output is shown in Figure 61 for the 3 readout gains, corresponding to DAC = 1 V, DAC = 100 mV and DAC = 10 mV, scaled by the factors of 10 in order to be superimposed. The risetime is less than 2 ns and independent of the DAC setting and the decay time corresponds to the argon drift time of 450 ns. At small DAC (10 mV and less), wriggles become visible due to parasitic inductance in the chip package. Although carefully minimized, this signal clearly visible when setting DAC = 0 peaks at around 20 mV, but its area is very small and almost negligible after the 50 ns shaping.

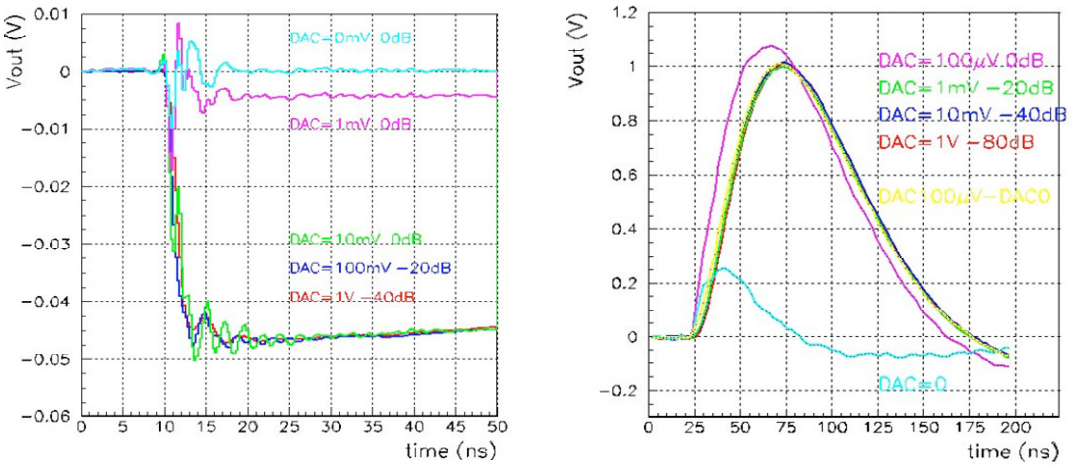


Figure 61 : calibration waveforms before (left) and after (right) shaping. The curves cover the DAC range 100 µV-1V and are rescaled to be superimposed and show the waveform.

After shaping, the pulses are shown in Figure 61. The pulses are now attenuated by factors up to 80 dB (10^4) for the full scale and the pulses are almost undistinguishable down to the DAC=1 mV pulse. A more quantitative analysis is performed in the next section with the linearity measurements. When setting DAC=100 µV (6 LSB or 10ppm of full scale) a different (faster) waveform is visible, due to the contribution of the parasitic injected charge seen as DAC = 0[44], which appears as a derivative of the normal pulse with a peak amplitude corresponding to ~15 µV. At the peak of the regular signal, the contribution of this parasitic signal is smaller than 1 LSB and when the waveform of DAC = 0 is subtracted to DAC = 100 µV waveform, the resulting pulse is again barely distinguishable from the canonical waveform.

∞ Pulse linearity

The linearity after shaping of the amplitude of one typical channel has been measured by recording the amplitude either at the peak of the signal, or at the time corresponding to the peak of the signal for DAC = 3000 (50 mV) ; the residuals are presented in Figure 62. The integral non linearity is well within ± 0.1 % on all gains. When measured at the time given by the DAC = 3000, a small non linearity is observed in the low gain which might result from a small increase of the signal rise-time due to slew rate. These results are worse by a factor about ten with respect to the DC current measurements because they are, as in ATLAS, dominated by the non linearity of the readout.

The amplitude uniformity over the 128 channels has also been measured at DAC = 5000 resulting in a 0.13 % dispersion. The larger value with respect to the DC current measurement (0.07 % for DAC = 6553) can be attributed to the inductance dispersion and a small contribution of the output lines and multiplexing test system.

∞

[44] For clarity, a channel with negligible (<1 µV) offset is shown here. On a regular channel, the waveform due to the offset (5-15 µV) has to be disentangled to see the PIC pulse shape.

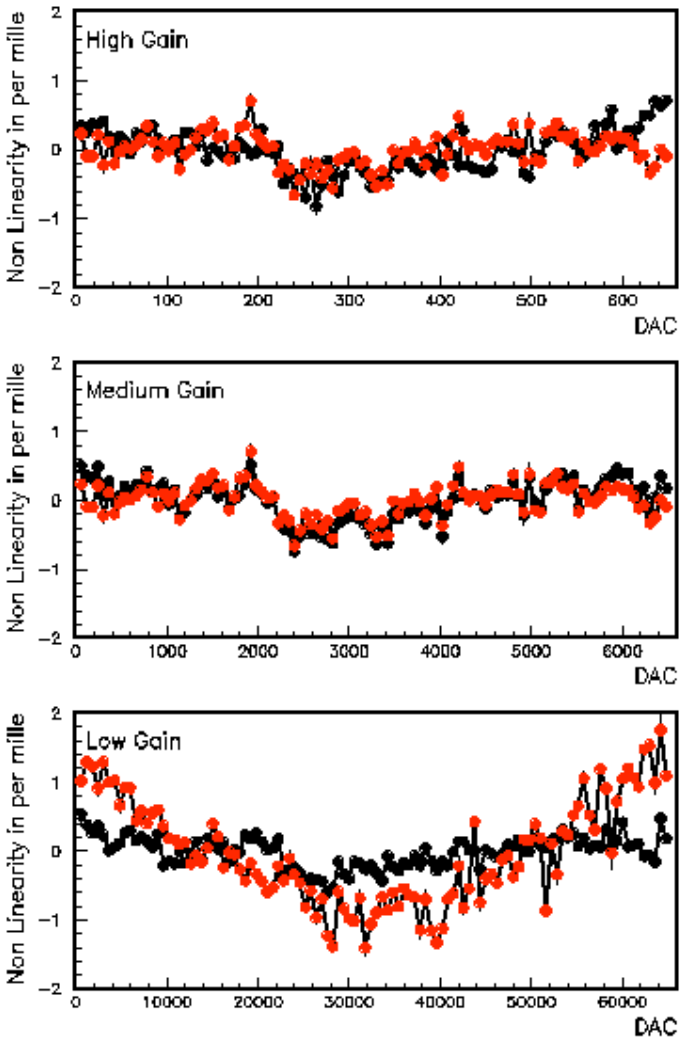


Figure 62 : linearity of the calibration pulse. Residuals in per-mil to the linear fit on the three DAC ranges 0-10 mV, 0-100 mV and 0-1 V

∞ Timing measurements

The time between the trigger and the calibration pulse can be adjusted with precision in order to compensate for cable lengths across the calorimeter (with fixed values of the PHOS4_RH delay chip). It can also be used to scan the pulse in order to reconstruct the pulse waveform. Particular attention has been taken studying the jitters introduced by the Calibration board and in particular by the delay chip and are detailed in reference [4]. The overall jitter of the board is 75 ps, dominated by the TTCRx chip.

4.4.3. production issues

∞ For ATLAS, 122 boards were necessary and around 140 were produced. They have been measured extensively both in Annecy and Orsay with an identical setup. The test bench is shown in Figure 63

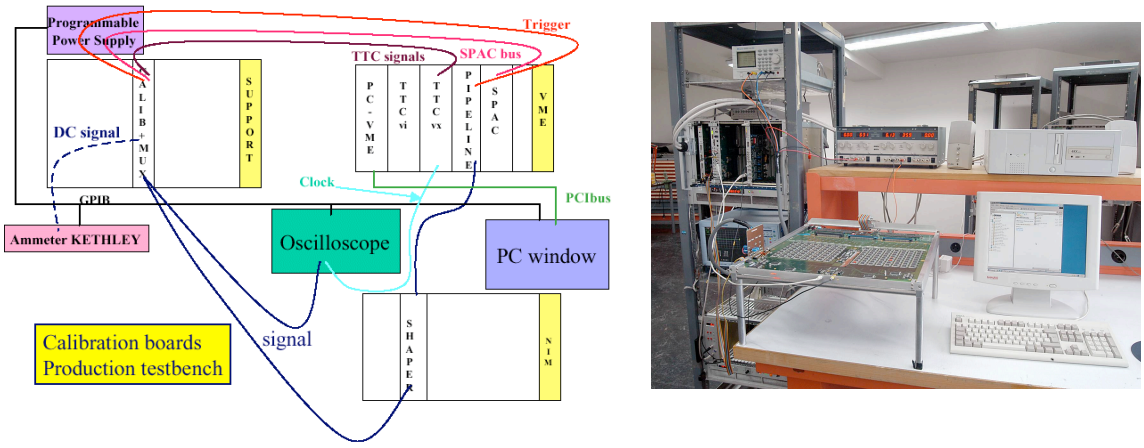


Figure 63: production test setup synoptic and picture

The test procedure consisted in :

∞ Adjusting the power supply regulators to their nominal value within 10 mV as well as the DAC full scale to 0.01% and zero to < 5 µV

∞ Checking the digital part that all channels could be turned on and off and registers read back

∞ Measuring all offset values

∞ Measuring the DAC linearity over the 16 bits

∞ Measuring the signal linearity over the 3 ranges and the 128 channels to be inside 0.1%

During the first production tests, a few channels exhibited a pulse amplitude slightly departing from their expected values. After a few thermal cycles, these channels got worse and additional channels turned out to deviate from nominal. This was traced to increased resistance of the output line (by a few 100 mΩ) which was due to cracks appearing in the PCB vias. Measurements with milli-ohmmeter and material cross-sections showed that the material was expanding too much during assembly process and two lots of PCBs had to be redone with low thermal expansion material. Afterwards, we were happy that the problem had been found thanks to the very high sensitivity of the tests, rather than after several years of ageing in ATLAS…

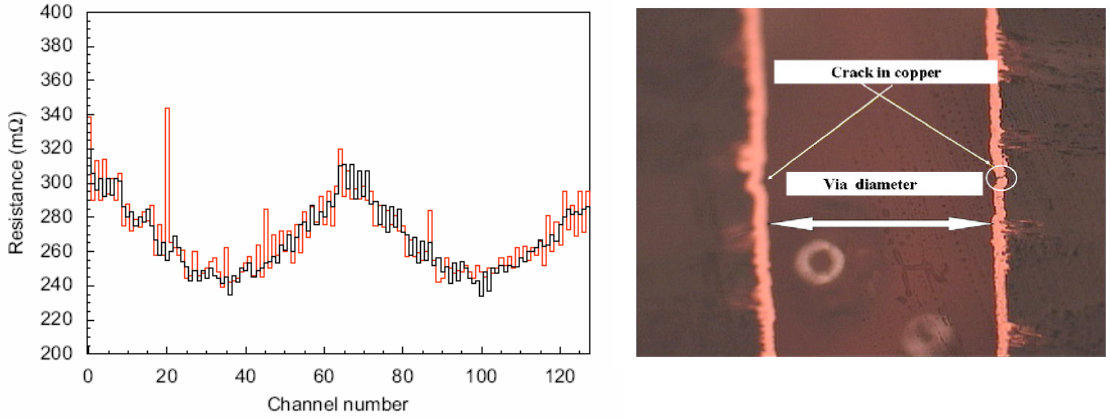


Figure 64 : output line resistance of a good (black) and faulty (red) calibration board. The larger resistance is due to crack in the PCB vias as shown in the right photograph which worsen with thermal cycles or ageing.

4.4.4. Performance in situ

The board stability and uniformity is a crucial parameter in operation. The offset stability is of course a possible concern, although it is in principle irrelevant for the calibration process[45]. The first check consists in comparing the values measured during the production testing to the pedestal obtained in the linear fit of the high gain. The correlation plot, displayed in Figure 65 shows the very good agreement obtained and establishes that the offset can be followed (and possibly corrected) with this procedure.

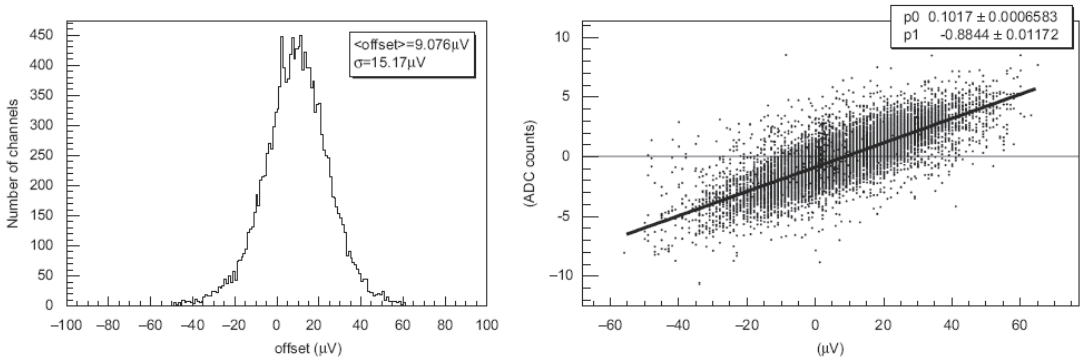


Figure 65: offset distribution on all the calibration boards and correlation with the value extracted from the linear fit on the response

5. Conclusion on the calibration

The 120 boards have been installed in summer 2006 and have been running smoothly since then. The performance in-situ is in good agreement with the specifications, allowing to reach the required accuracy.

[45] The offset gives a pedestal which is removed in the linear fit of the readout response, there is no difference between it and the one from the readout, provided it is stable.

CHAPTER 3

ATLAS DETECTOR CHARACTERIZATION

1. Introduction

With the fast shaping used for the liquid Argon calorimeter and the high precision required for energy measurement, the simplistic modelization of the detector as a pure capacitance became questionable. In particular, as shown in this chapter, the inductance between the middle electrode and the readout cable alters the signal and modifies the physics/calibration ratio with a sensitivity as high as 0.2%/nH ! Also the sensitivity of the digital filtering to the actual signal shape makes necessary to obtain an accurate physics signal, starting from the calibration pulse. This again required an accurate measurement of the detector electrical characteristics.

The first section will detail the study whether the detector needs to be considered as a transmission line or if it can be lumped as discrete elements and with what values and how they were measured

The second section will detail the parameters necessary to understand the pulse shape.

The third section will recall the effort which had been carried out by the "crosstalk task force" in order to minimize all the sources of crosstalk and examine its effects on the performance.

2. Detector modelization (unpublished LAr note)

Traditionally, the LAr calorimeter is modelized as a pure capacitor corresponding to the electrode facing the grounded absorber from which the LAr is the dielectric. With the accordion geometry and the fast shaping used, the detector can also be seen as a transmission line. Moreover, the kapton electrodes of the LAr calorimeter are etched to obtain a segmentation of three samplings in depth (Front, Middle and Back) and also to have a constant granularity along the beam axis (z or η[46]). The middle sampling has a constant depth of 21 X_0 corresponding to around 20 cm and a constant width : $\Delta\eta = 0.025$ corresponding to around 2.5 cm. This electrode is read out at the back of the calorimeter and as it is a cylinder and not a sphere, the connection to bring the signal out exhibits a large variation in length (see Figure 66).

Most of the energy is deposited in the middle compartment, where the best accuracy is required, down to a few per mil. In order to correct for the variations of all the parameters which are in the signal path (cables, preamplifiers, shapers...) a precise calibration pulse is applied as close to the signal form particles as possible. Unfortunately, it is not possible to connect the calibration pulse right in the middle of the

∞

[46] Pseudo rapidity : η = Ln tan(θ/2) in which θ is the azimuthal angle with respect to the beam line

collecting electrode and this signal is injected at the back of the calorimeter, on the motherboards where 4 electrodes are summed in parallel and connected to the readout cable.

All the elements which are between these two points have to be carefully understood and measured in order to correct for the bias they introduce.

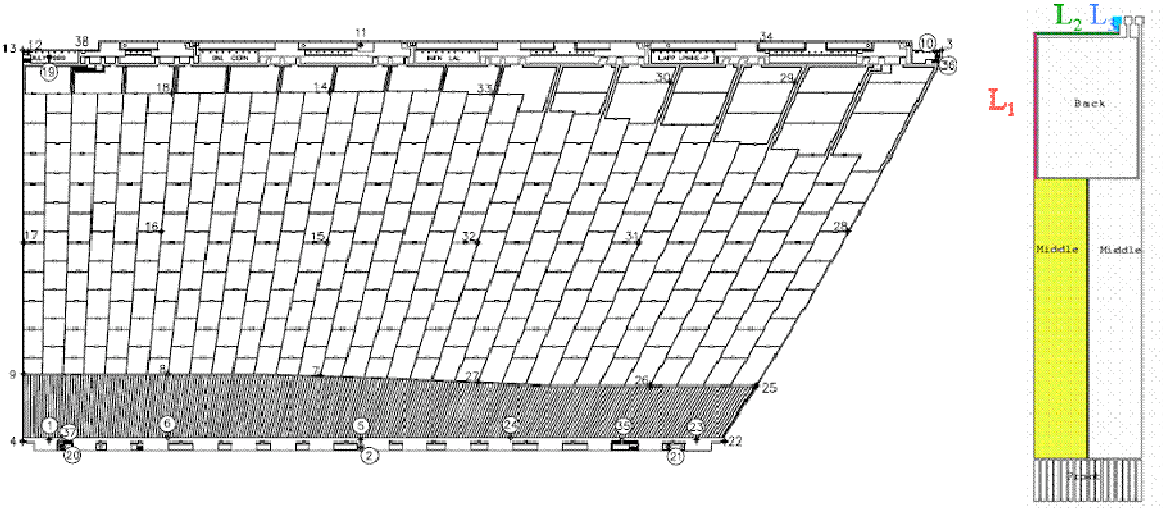


Figure 66: view of one electrode of the barrel, split in three samplings : front, middle and back.

2.1. detector geometry, line and lumped model

The most accurate modelization of one cell on the kapton electrodes is a transmission line model or stripline : the signal is the conductor on the kapton, the dielectric the liquid argon and the absorber is the return ground, as can be seen in Figure 67.

An ideal (lossless) line is characterized by two parameters[47] : either its capacitance C and inductance L, or its characteristic impedance R_C and its propagation time T_d. These quantities are related through the usual equations : $R_C = \sqrt{L/C}$; $T_d = 1/\sqrt{LC}$. The propagation velocity depends only on the dielectric medium : $v = c/\sqrt{\varepsilon_r}$ which relates the inductance and capacitance. Therefore, knowing the capacitance (and the dielectric permittivity) permits to determine all the line parameters.

So far, the model of striplines has been used as for usual printed circuit boards and the electrical characteristics can be calculated from the geometrical dimensions[48]. However, the kapton electrodes slightly differ from this model mostly because of the close presence of the neighbouring electrodes and because of the different thickness which must be used for the signal[49]. Therefore, the electrodes should be considered as *coupled transmission lines* and their electrical characteristics have been completely extracted by solving *Poissons*'equation with finite element analysis.

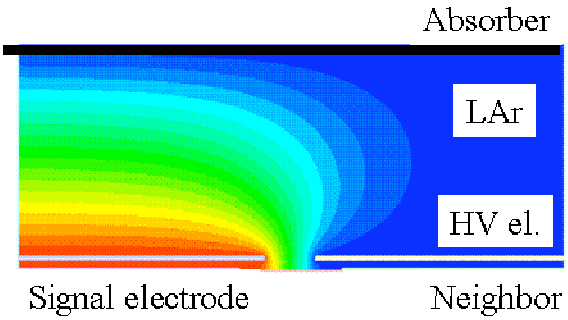


Figure 67 : equipotential lines in detector

∞

[47] This holds for an isolated line with no losses. For coupled lines, as is the case of the electrodes, four parameters are necessary : C_D, C_X, L and M, or the characteristic impedance and propagation velocities in common and differential modes. This will be detailed in the following

[48] A stripline of width W and thickness 35 µm at a distance g of two ground planes exhibits a characteristic impedance : $R_C = 377/\sqrt{\varepsilon_r}\,(1.765 + 2W/g.)$ This formula takes into account the edge effects, hence the 1.765 additional term. Neglecting this term reduces the expression to the formula of the plane capacitor.

[49] The signal conductor is in fact made of three 35 µm copper layers (2 high voltage and a signal) separated by 80 µm kapton material.

Solving *Poissons*'s equation allows to extract the capacitance to ground C_D and to the neighbouring electrodes C_X, which scales nicely with electrode thickness (large compared to the gap). The different configurations have allowed to fit these capacitances as :

- $C_D = (9.81 + 8.43*w) * \varepsilon_r * l$
- $C_X = 18.7 * \varepsilon_r * l$ in the front
- $C_X = 10.5 * \varepsilon_r * l$ in the middle and back[50]

In which w and l are the width and length of the electrode in mm, the bigap of LAr is taken for the barrel g = 2.1 mm and the permittivity of LAr is $\varepsilon_r = 1.53$.

The total capacitance, shown in Figure 68 is given by $C_T = n(C_D + 2\,C_X)$ where n = 4 for middle and back and n = 16 for the front.

The transmission time T_d is simply obtained by the permittivity or the propagation velocity ($c/\sqrt{\varepsilon_r}$ = 4.12 ns/m) and the line length.

This allows to calculate the characteristic impedance[51] obtained using

$$R_C = T_d / C_T$$

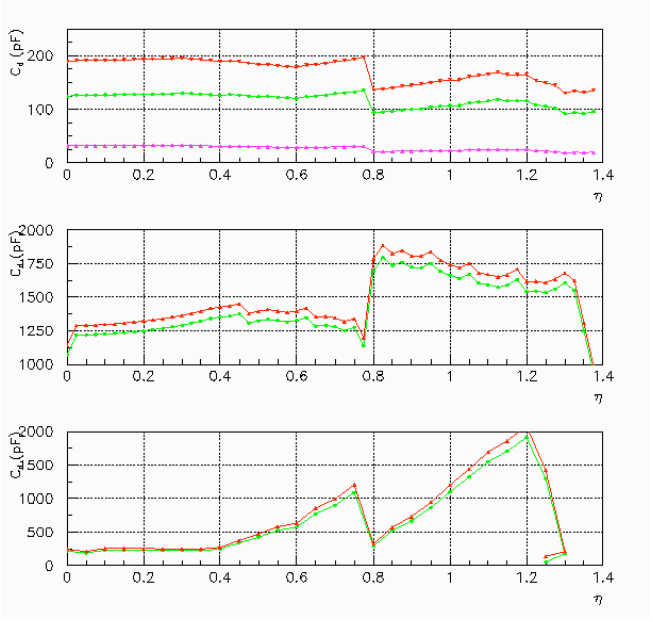


Figure 68: capacitance to ground (green) to the neighbours (blue) and total (red) for the front (top) middle and back (bottom) samplings of the barrel calorimeter

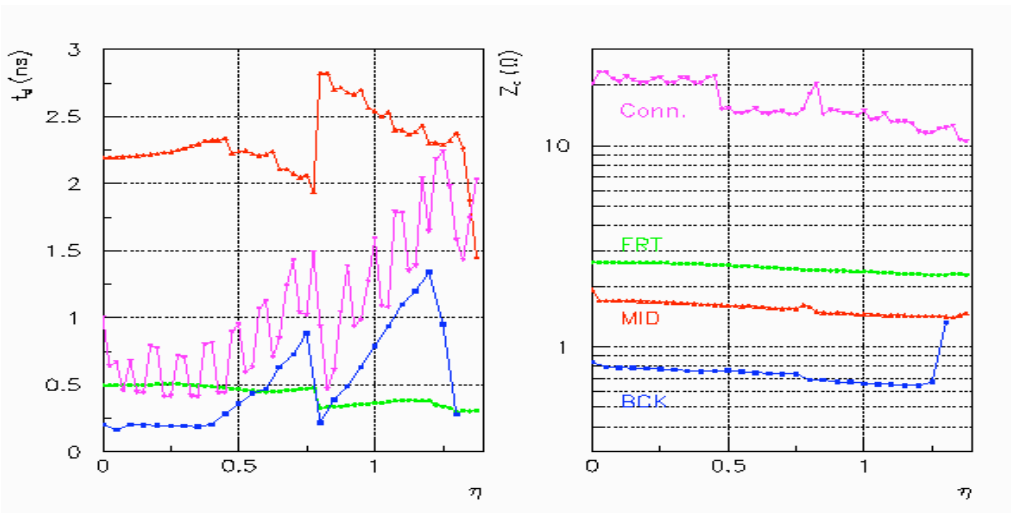


Figure 69 : propagation delay (left) and characteristic impedance (right) of the 3 samplings + connection

∞

[50] The spacing between two neighbours is taken equal to 1 mm, for the midlle and back and 0.5 mm for the front, wheras the signal electrode further recessed by 0.25 mm.

[51] With coupled transmission lines, there are two expressions for the characteristic impedance, one for the common mode and one for the differential mode $R_C(cm) = \sqrt{(L+M)/C_D}$; $R_C(dm) = \sqrt{[(L-M)/(C_D+2C_X)}$. In our case, most of the signal is deposited in one cell and only a small fraction flows in the neighbours. In that case, it is legitimate to assume that the crosstalk signal induced in the neighbours does not modify the main signal. In transmission lines theory, this hypothesis is referred to as weak coupling approximation. In that case, the transmission line equations can be simplified as $R_C = \sqrt{L/(C_D+2C_X)}$

Given the large difference in characteristic impedance of the two lines described above forming the middle cell and its connection to the back, the lower impedance one (detector middle cell) can be seen as a capacitance C_1 and the the higher one (connection) as an inductance L_2 according to the following equations :

$C_1 = T_{d1}/R_{C1}$ and $L_2 = T_{d2}*R_{C2}$

This approximation has been checked in simulation, comparing the impedance of both models as a function of frequency. First, it can be seen in Figure 70, that the general behaviour is the same up to hundred MHz. More precisely, at low frequency, the line model is equivalent[52] to a capacitance which is the sum of the two capacitances C_1 and C_2.

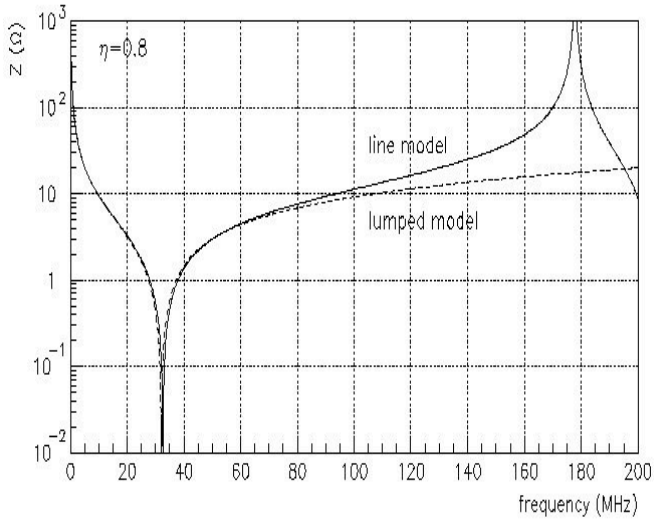


Figure 70 : impedance as a function of frequency of the line model and lumped using C1+C2 and L2

To evaluate the equivalent lumped inductance, the resonant frequency can be studied both in the line model and in the LC model, using the total capacitance C_1+C_2. The results are summarized in the table below, in which it can be seen that the best approximation is obtained by taking only L_2. The accuracy of the lumped model has been further checked by comparing the waveforms with the line model and the lumped LC model, showing an agreement within 0.1% over the L, C range shown in the next section.

eta	C_1	L_1	C_2	L_2	f_0 line	$1/\sqrt{L_2C_1}$	$1/\sqrt{L_2(C_1+C_2)}$
0.025	1105 pF	3.91nH	31 pF	13.1nH	**39.6MHz**	41.8MHz	39.9 MHz
0.425	1232pF	3.95nH	21.2pF	8.9 nH	**43.8MHz**	48 MHz	47.6MHz
0.8	1438 pF	4.17 nH	80pF	16.3nH	**31.3MHz**	32.9MHz	32.0MHz
1.125	1353pF	3.35nH	191pF	26.1nH	**25.7MHz**	26.8MHz	25.1MHz

Conclusion : these calculations and simulations have allowed to define the lumped model of the middle sampling of the electrode as a series L and C. The inductance L corresponds to the line that connects the middle sampling to the output connectors and is calculated knowing its total length (T_{d2}) on the electrode and the capacitance is the sum of the capacitance of this line (C_2) and the capacitance of the middle sampling itself (C_1).

∞

[52] Calculating the impedance of the two lines in series and looking for an equivalent in the low frequency region gives $Z = R_{C1} / j\omega T_{d1} \{1 / 1 + R_{C1} T_{d2} / R_{C2} T_{d1})$, which is a pure capacitance. Letting $C_1 = T_{d1}/R_{C1}$ gives $Z = 1 / j\omega (C_1+C_2)$

The inductance values obtained over the whole barrel[53] are summarized in Figure 71. They led to an update from the values calculated in the TDR [1] which were using only the length of the connection and were too crude. The pattern (2 high values, 2 low values) corresponds to the cells far and close to the output connector. The variation of around 15 nH will require a correction on the calibration signals of around 3%.

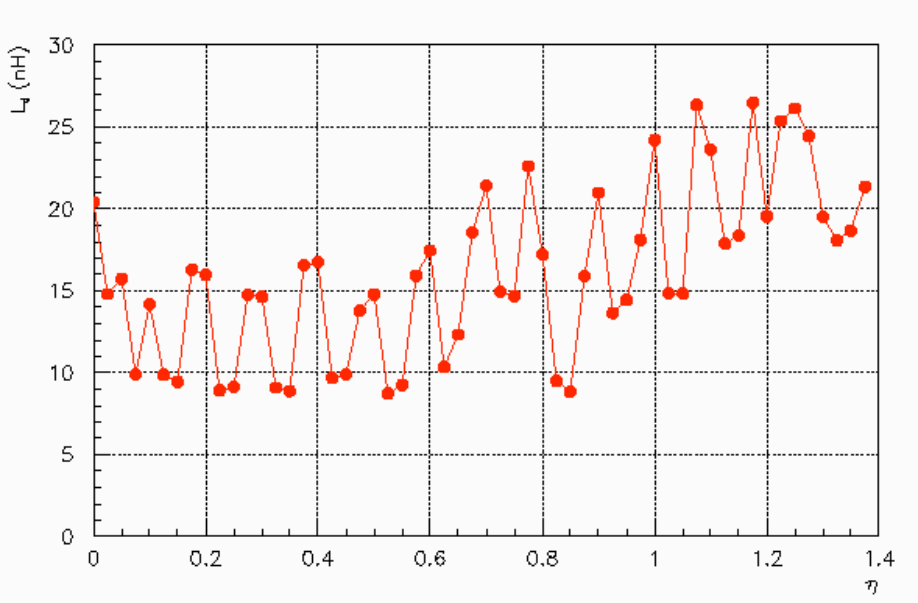


Figure 71 : calculated detector inductance for the middle section of the barrel calorimeter using the complete line model and detector geometry.

2.2. Detector measurement

As the detector inductance[54] has a crucial impact on calorimeter accuracy, a lot of efforts have then been deployed in order to measure it.

When, there was access to the summing boards, the real electrodes have been measured using an RLC impedance-meter (HP 4285A) up to 30 MHz. For this measurement, a special small PCB had been realized in order to perform a four point connection with minimal stray inductance. It plugs in the summing board in place of the motherboard and is moved around.

A typical measurement is shown in Figure 72. The fit of a pure RLC is good as can be seen from the residuals, showing again the good accuracy of the lumped model. It was also seen that the Imaginary part of the impedance was giving a more precise value of the resonant frequency than

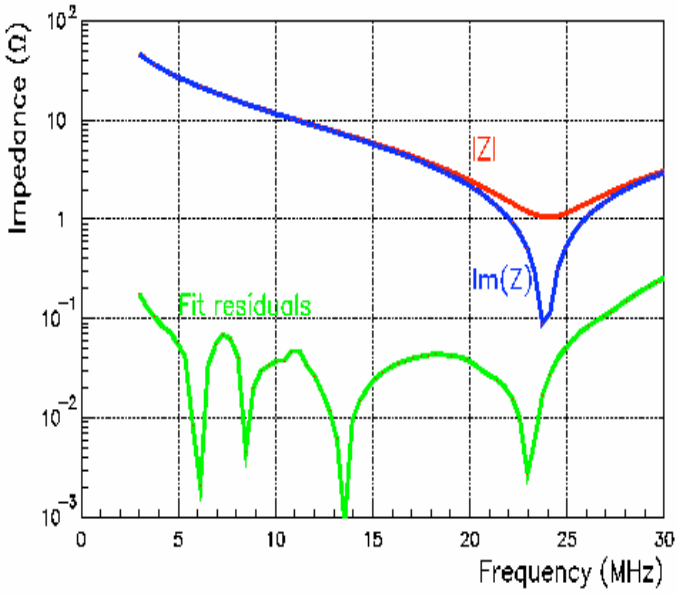


Figure 72 : measured detector impedance

∞

[53] Similar calculations were also done for the endcap. It sl
compartments as they are close to the connectors and hav

[54] In fact, it is the resonant frequency that is the important quantity to be measured, as shown in the next section.

the module and has been used in the systematic campaign of measurements that has been carried out on the whole modules in 2002-2003. The results are shown in Figure 73, showing a good agreement of the general shape, together with a large added value that puzzled us for a while. In fact, it corresponds to the summing boards shown in Figure 74 that gang 4 electrodes in parallel to form a 0.025 tower in φ and bring them to the motherboards (see also Figure 75 and Figure 76).

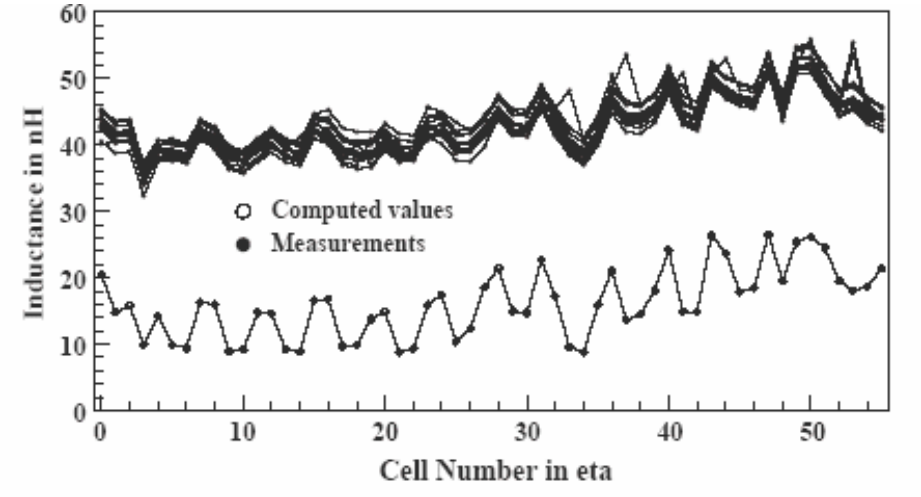


Figure 73 : measured inductance on the calorimeter barrel calorimeter compared to the calculated values. The pattern is similar and the offset is explained by the extra inductance added by the summing boards and connectors to the motherboard.

Indeed, the summing boards have also been measured separately and exhibit an inductance of 9 to 15 nH. They have been redesigned to equalize the length in phi in order no to introduce a variation with φ of the inductance pattern.

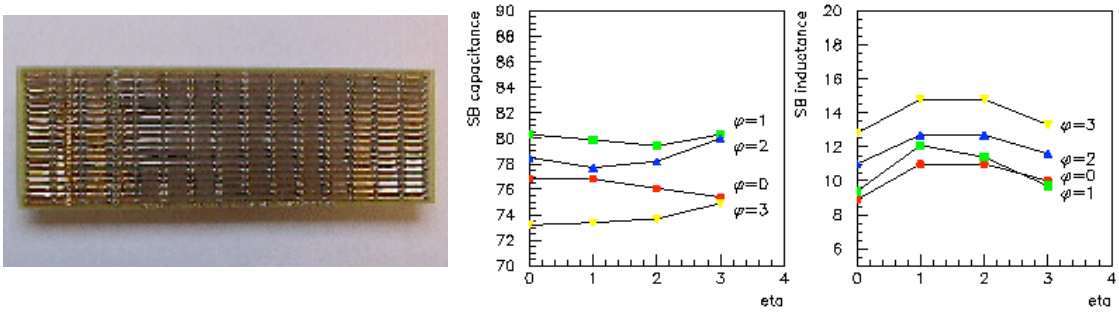


Figure 74: photograph of a summing board that gangs 4 electrodes in phi and route the signals to the motherboard. Measured capacitane and inductance.

2.3. The complete readout path

The lumped model and the measurement of capacitance and inductance of the electrode is a nice step on the path of signal reconstruction, but many more items are on the signal path between the central electrode where it is generated and the readout preamps. Summing boards were mentioned before as 4 electrodes are connected together in φ to form a $\Delta\varphi = 0.025$ tower. Then signals are routed on motherboards to output connectors and to distribute the calibration pulses. All this chain is shown in the synoptic of Figure 75 and in real on the picture of Figure 76.

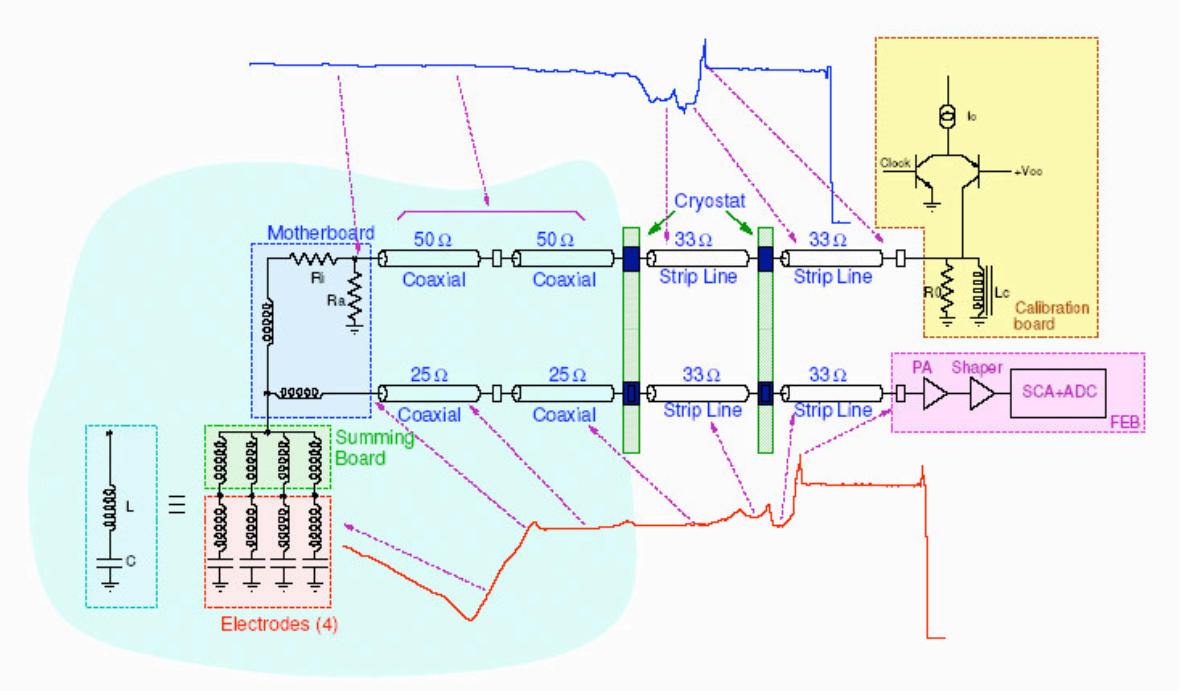


Figure 75 : calibration and readout signal path showing the different cables and connectors.

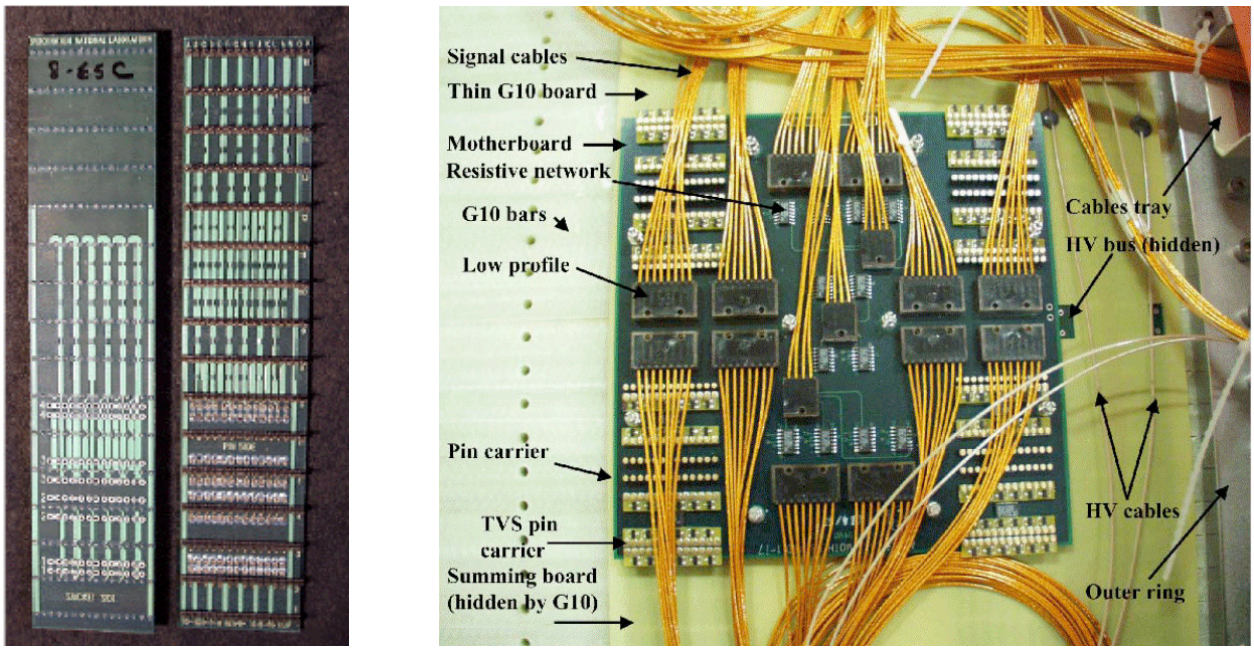


Figure 76: photograph of the summing boards (left) and motherboards (right) with low profile connectors and output cables

Once again, it was necessary to measure all the detector parameters, but with the detector in place at cold with the liquid argon. A quick simulation finished to convince us that it was hopeless to measure 20 nH and 1 nF with a few percent precision after several meters of cable whose characteristics were not known better than 5%. A four-points measurement was needed there and the calibration signal supplied a way to come close to it ! In effect, by using the calibration resistor to inject a sinusoidal wave and measuring the voltage at the detector with the readout, it was a 3 points measurement which could give

access to the resonant frequency which was the most important measurement for the waveform reconstruction. Moreover, as the inductance did not depend on the presence of LAr it would also give the capacitance.

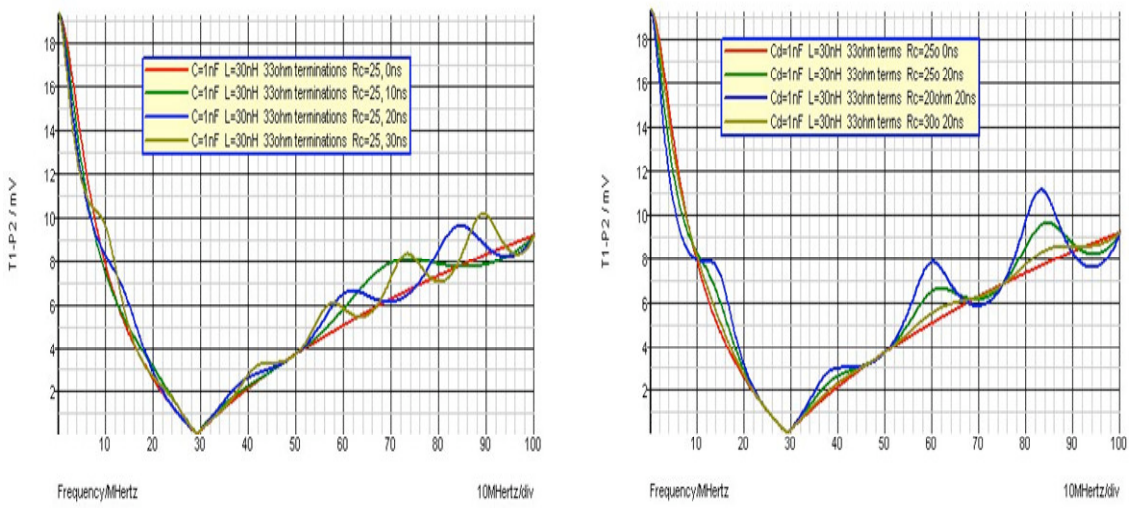


Figure 77: simulated detector impedance at the end of 5 m cable and feedthrough with various mismatches. The resonant frequency that is the quantity of interest remains unaffected.

An automated setup (Figure 78) has been designed so that this measurement could be carried out on 100% of the detector, but is still took quite some effort and shifts. Each channel was fitted (at warm and cold) to extract the resonant frequency f_0 and impedance. An example of measurement is shown in Figure 79. The extracted values are then stored in the data base to be used for the pulse reconstruction described in the next section.

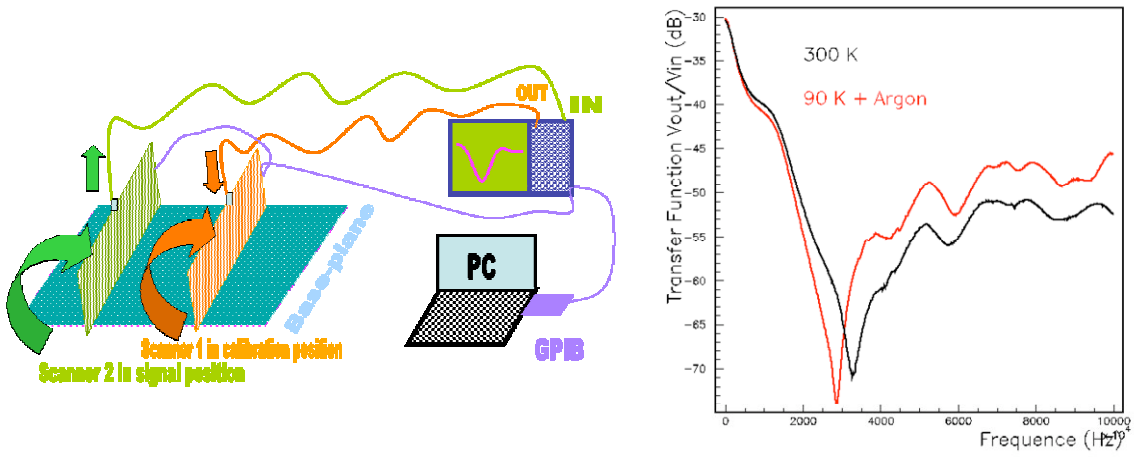


Figure 78: experimental setup to measure the resonant frequencies in the calorimeter. Example of measurement (right) both at warm and in liquid argon

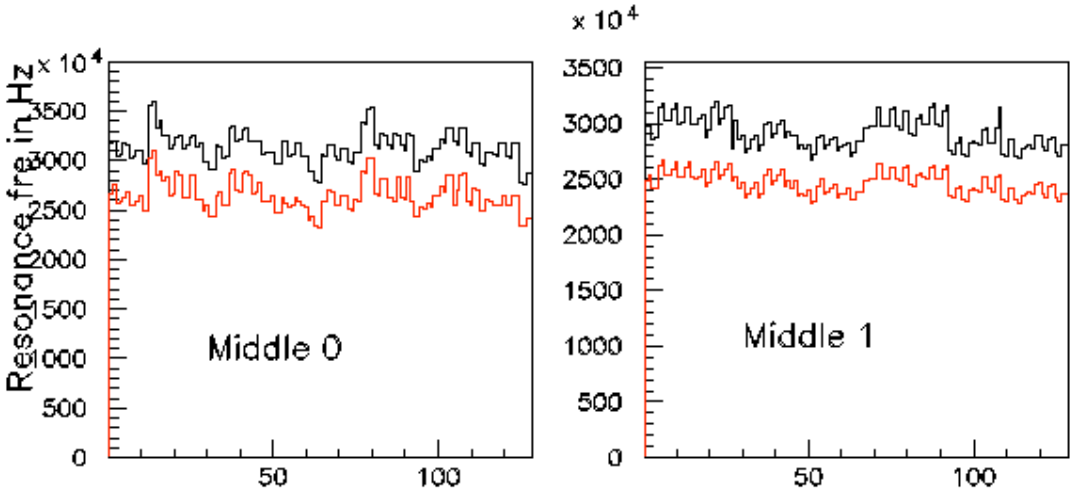


Figure 79: resonant frequency measurements in the barrel calorimter both at warm (black) and in liquid argon (red). The values obtained are used to correct for the calib/physics ratio.

3. Understanding the signal shape

As was explained in Chapter 2, the calibration and signal physics slightly differ and it is important to get the correct physics signal shape in order to calculate the optimal filtering coefficients and get a good calorimeter uniformity.

The physics signal has a triangular shape, with a decay time corresponding to the drift time T_{dr}.. It has been shown by our previous work in Ref that measuring the undershoot amplitude allows to extract precisely the drift time. It is applied across the detector capacitance C_D and flows into the readout cable through the connection inductance L_D, explained in §2 .

The calibration signal has an exponential shape initially following the decay time of the LAr pulse, as described in Chapter 2. It is applied on the motherboard thanks to the injection resistor R_{CAL} and splits between the output cable and the series combination of detector capacitance and inductance.

The signal and calibration paths are summarized in Figure 80. It is clear that the detector inductance affects differently the physics and calibration pulses[55], leading to a different pulse shape and amplitude, all the more since the shaping time is fast[56] and the inductance effect becomes more important.

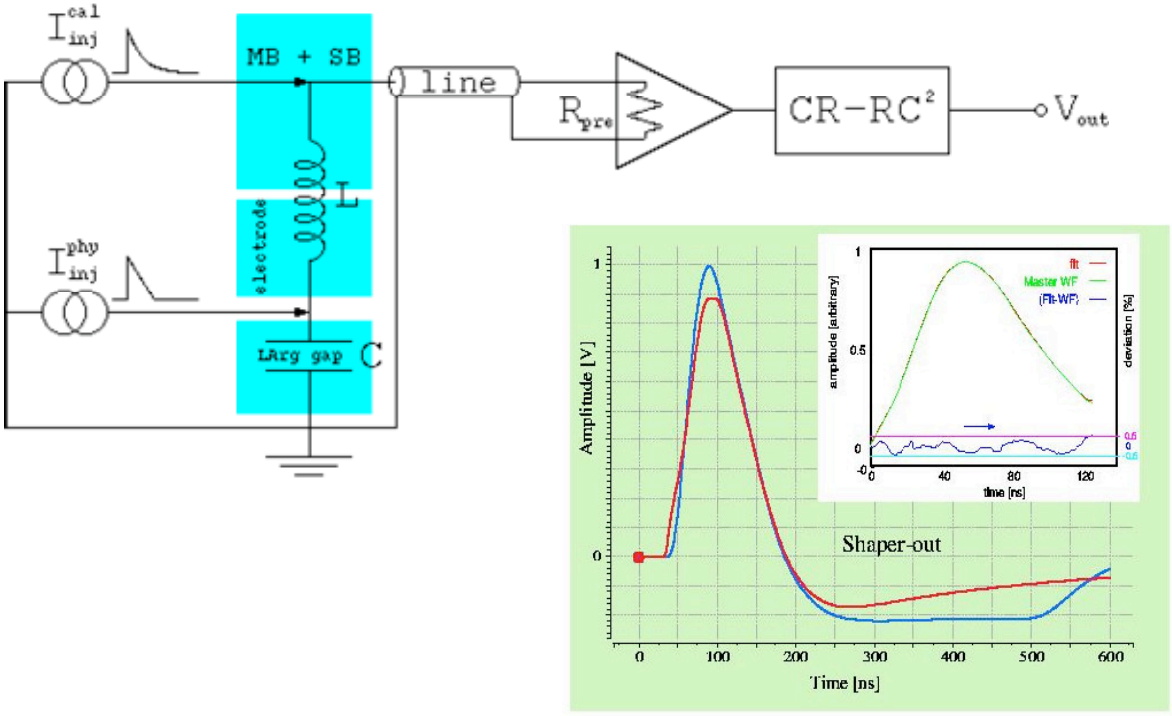


Figure 80: physics and calibration signal paths and waveforms

A first order analytical calculation can be performed to evaluate the difference in the calibration and physics pulse amplitude[57]. As usual, the signals are calculated in the frequency domain and brought back in the time domain by inverse *Laplace* transform in order to calculate the signal peak amplitude.

∞

[55] For the physics signal, the inductor in series gives a slightly resonant RLC circuit, with a quality factor (Q~0.2 with C~1 nF, L~30 nH and Rc=25 Ω). For the calibration signal, the inductance "shields" the capacitance and the fast edge flows in the preamp, creating an early "shoulder" on the calibration pulse.

[56] The effect will worsen at high luminosity with digital filtering as shown in Chapter 1.

[57] The second order calculation is necessary to get the. waveforms correct, in particular on the trailing edge, where the various impedance mismatches in cables and feedthroughs produce visible distortions that affect the digital filtering, as shown in []

Starting from the physics and calibration currents expressions in the frequency domain :

$I_{PHY}(s) = I_O\,(1/s - 1/s^2T_{dr} + \exp(-sT_{dr})/s^2T_{dr})$ and $I_{CAL}(s) = I_O\,(1+ s\tau_{cal})/(sf_{step}+s^2\tau_{cal})$

In which s is the frequency *Laplace* variable, T_{dr} is the drift time in liquid argon (~450 ns), τ_{cal} the exponential decay time of the calibration pulse and f_{step} the initial value of the calibration pulse (cf Chapter 2 § 3.1).

The fractions of these currents that flow in the cable are then respectively :

$I_1(s) = I_{PHY}(s) / sC_D(R + sL_D + 1/sC_D)$ and $I_2(s) = I_{CAL}(s)\ (sL_D + 1/sC_D) / (R + sL_D + 1/sC_D)$

Assuming that the cable is perfectly terminated in its characteristic impedance and that the preamplifier of transimpedance R_F is followed by the CRRC² shaper, the voltage at the output of the shaper for both cases are respectively :

$$V_{PHY}(s) = I_0 \frac{sTd - 1 + \exp(-sTd)}{s^2 Td} \frac{1/s.C_D}{R + sL_D + 1/s.C_D} R_F \frac{\tau.s}{(1+\tau.s)^3}$$

$$V_{CAL}(s) = I_0 \frac{1 + s.\tau_{CAL}}{sf_{step} + s^2\tau_{CAL}} \frac{sL_D + 1/s.C_D}{R + sL_D + 1/s.C_D} R_F \frac{\tau.s}{(1+\tau.s)^3}$$

From which the ratio can be easily calculated :

$$\frac{V_{PHY}(s)}{V_{CAL}(s)} = \left(\frac{1}{1 + s^2 L_D C_D}\right)\left(\frac{sTd - 1 + \exp(-sTd)}{s.Td} \frac{1 + s.\tau_{CAL}}{f_{step} + s.\tau_{CAL}}\right)$$

The first term happens to be completely dominant and requires the knowledge of the resonant frequency to a few percent. The second term only reflects the slight difference in physics and calibration pulse shapes (exponential vs triangular) and is negligible at fast shaping.

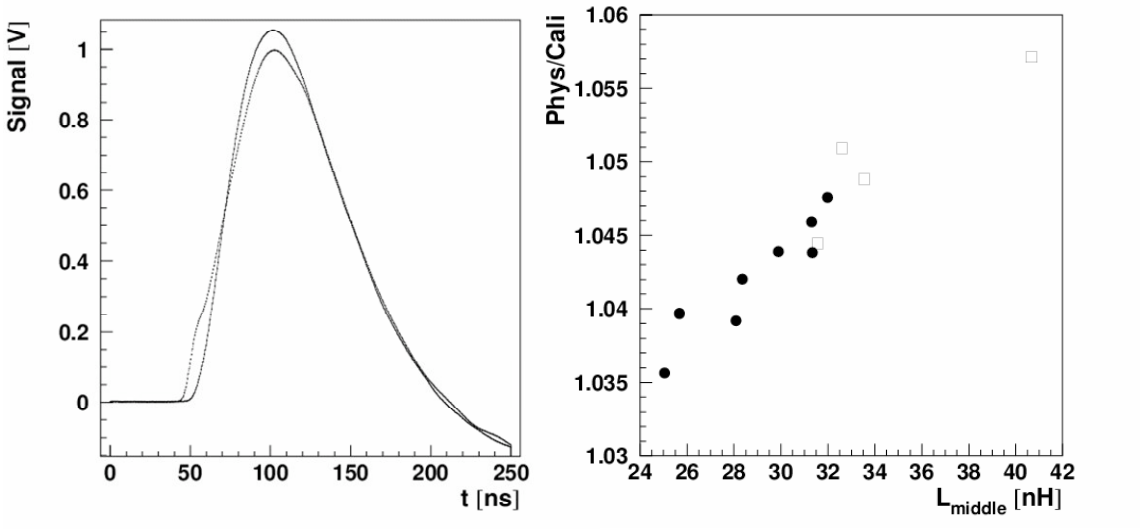


Figure 81. Left : calibration and physics waveforms. The calibration waveform exhibits a "shoulder" due do the detector inductance L_D and a smaller amplitude leading to a ratio Phys/Calib which is a function of the detector inductance (and also of detector capacitance). This effect needs to be corrected and requires the capacitance and inductance measured to ~10% accuracy over the whole calorimeter.

4. Crosstalk (2 LAr notes [15][17])

Two unusual features have motivated a particular study of the crosstalk and even the creation of the cross talk task force" to tackle the issue :

In the Front section, as the strips are 5 mm wide, 2 mm to ground and separated by 500 μm from their neighbours, the capacitance to the neighbouring cells (noted C_X) is similar to the capacitance to ground (noted C_D). Thus, the usual approximation of C_X « C_D is no longer valid for the crosstalk calculations. Moreover, the fast shaping and non negligible preamp rise time make the crosstalk shape not a pure derivative and the contribution at the peak is not negligible. The effect on π^0 rejection, which is one of the main objectives of the front fine segmentation could be jeopardized and this led to a dedicated note (LArG 39) [17].

In the middle section, where the capacitance to neighbours is small, some channels had an un-expected high value of crosstalk (several %) which was an important worry for the calorimeter uniformity

Finally, some channels had long distance crosstalk which was traced to the feedthrough ground return resistance. This effect of up to several % led to the gold plating of all the calorimeter and systematic measurement on the whole calorimeter

4.1. Capacitive crosstalk in the front strips

The crosstalk capacitance C_X between two channels is calculated as shown on the schematic in Figure 83. An important parameter on the crosstalk amplitude is the preamplifier input impedance R_{in}, the lower its value, the lower the crosstalk. More precisely, the most important parameter is the time constant $\tau_{pa} = R_{in} C_D$ compared to the shaping time τ_{sh}.

In the case of ATLAS, the use of ØT readout is forcing us in the region where $R_{in}C_D \sim \tau_{sh}$, which has a penalizing effect on crosstalk as the crosstalk signal is no longer a pure derivative of the signal.

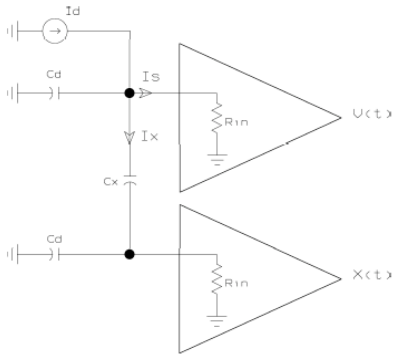


Figure 82 : capacitive crosstalk schematic

The calculations have been detailed in [17]. They give in the frequency domain :

$V(s) = R_F I_0 \, s\tau_{sh} / (1+s\tau_{pa})(1+s\tau_{sh})^3$

$X(s) = R_F I_0 \, s\tau_{sh}\tau_{pa} \, C_X / C_D (1+s\tau_{pa})^2(1+s\tau_{sh})^3$

In which V(s) is the signal waveform at shaper output and X(s) the crosstalk.

This gives in the time domain :

$$V(x) = R_f I_o \left[\frac{\lambda^2 e^{-x/\lambda}}{(\lambda-1)^3} - \left(\frac{x^2}{2} + \frac{\lambda x}{\lambda-1} + \frac{\lambda^2}{(\lambda-1)^2} \right) \frac{e^{-x}}{\lambda-1} \right]$$

$$X(x) = -R_f I_o \frac{\lambda C_x}{C_t} \left[\left(x - \frac{\lambda^2+2\lambda}{\lambda-1} \right) \frac{e^{-x/\lambda}}{(\lambda-1)^3} + \left(\frac{x^2}{2} + \frac{\lambda+1}{\lambda-1} x + \frac{\lambda^2+2\lambda}{(\lambda-1)^2} \right) \frac{e^{-x}}{(\lambda-1)^2} \right]$$

In which $x = t/\tau_{sh}$ and $\lambda = \tau_{pa}/\tau_{sh}$ characterizes the preamplifier rise time with respect to the shaping time.

The crosstalk can then be specified in two manners :

∞ Peak of crosstalk : X_{max} is the maximum amplitude of the crosstalk signal normalized to the maximum amplitude of the direct signal : $X_{max} = \max\{X(x)\} / \max\{V(x)\}$

∞ Crosstalk at peak : $X(t_{max})$ is the crosstalk amplitude at the signal peak t_{max}, normalized to V_{max}

It is interesting to notice that the crosstalk amplitude scales directly with C_X/C_D and that the crosstalk signal "sees" one more pole ($1+s\,\tau_{pa}$ is to the square), slowing down the crosstalk signal. The effect is plotted in Figure 83. It can be seen for two very different preamp risetimes that in one case, the crosstalk is a clean derivative, whereas in the case of $\tau_{pa} = \tau_{sh}$, it amounts to half of the crosstalk peak.

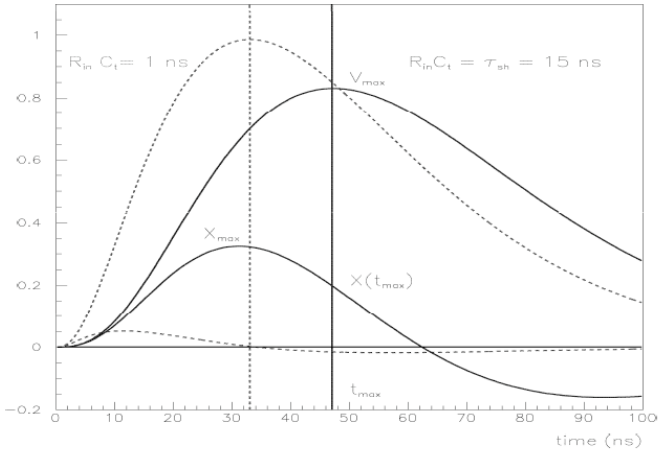


Figure 83 : signal and crosstalk waveforms are shown for two different preamp impedances and 15 ns CRRC2 shaping. In red, a small impedance such as RinCd=1 ns corresponding to an almost ideal preamp and in blue a preamp corresponding to the 0T ATLAS case in which RinCd=tau=15ns. The coupling capacitance is taken such as Cx=Cd for normalization.

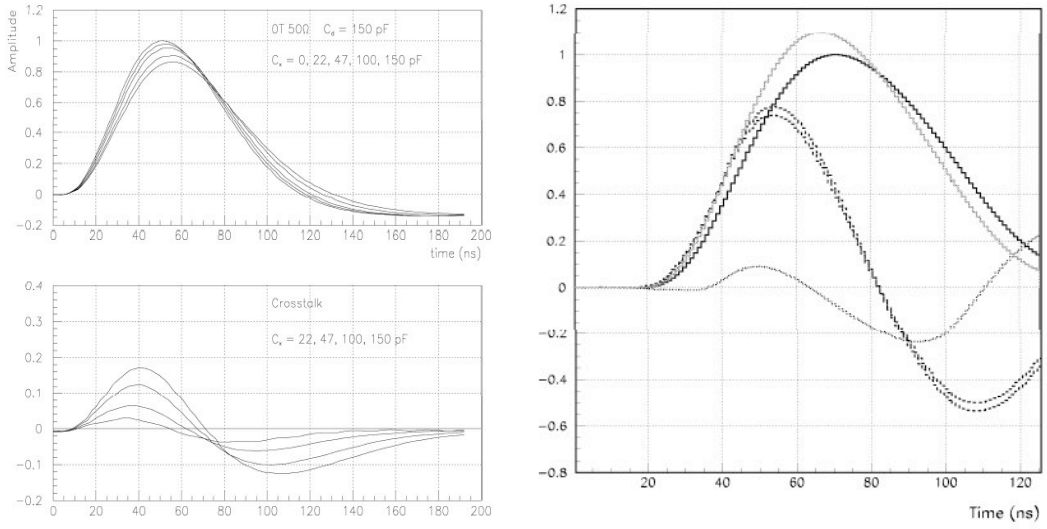


Figure 84 <u>Left</u> : measured waveforms with the effect of various crosstalk capacitances between one channel and its neighbours. On the top left plot, the effect on the signal which decreases and slows down and on the bottom left, the crosstalk signal. <u>Right</u> : measured crosstalk on both sides in the calorimeter strips (multiplied by 10) compared to the main signal (solid line). In the calorimeter, the crosstalk capacitance is 40 pF to both sides, giving a crosstalk of 7-8%, with an amplitude and shape in good agreement with simulations and testbench measurements.

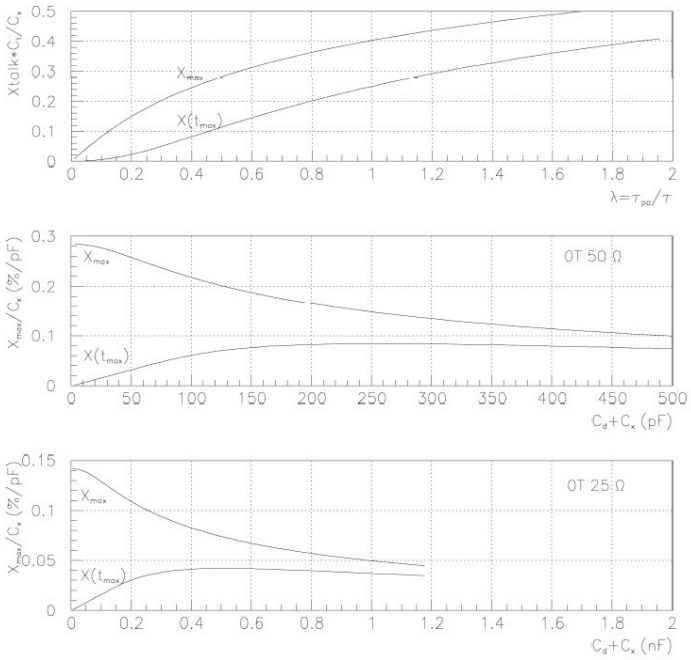


Figure 85 : theoretical crosstalk amplitudes as a function of λ and normalized to C_X/C_D = 1. Bottom curves : Xmax and X(tmax) as a function of $C_D + C_X$ for 25Ω and 50Ω preamplifiers, τ = 15ns CRRC² shaper, normalized to C_X =1. Knowing $C_D + C_X$, the crosstalk in % is obtained by multiplying the value on the plot by C_X. For example in the strips, C_D=150 pF and C_X =50 pF, the top curve in the middle plot gives 0.16%/leading to Xmax=0.16 C_X = 8%.*

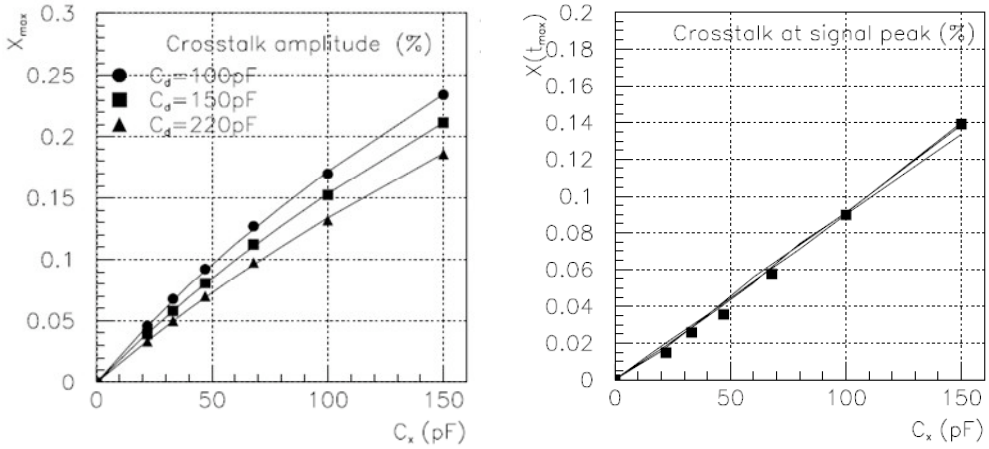


Figure 86: measured Peak of crosstalk and Crosstalk peak (in %) as a function of crosstalk capacitance in the 50Ω 0T preamplifiers

As was shown in §2.1. , the capacitance to the neighbours has also been calculated with Poisson equation and is shown in Figure 87, giving for the front strips in the barrel typical values of 40 pF (to each neighbour) whereas the capacitance to ground is 120 pF. This leads to a crosstalk at signal peak of around 8% as shown in the theoretical expressions of Figure 85 and the testbench measurements of Figure 86.

Finally, the crosstalk in the strips has also been measured in the calorimeter itself using calibration runs (and also physics data) and have again given a value around 8% with a good agreement for both shape and amplitude with the calculations and testbench measurements as displayed in Figure 88.

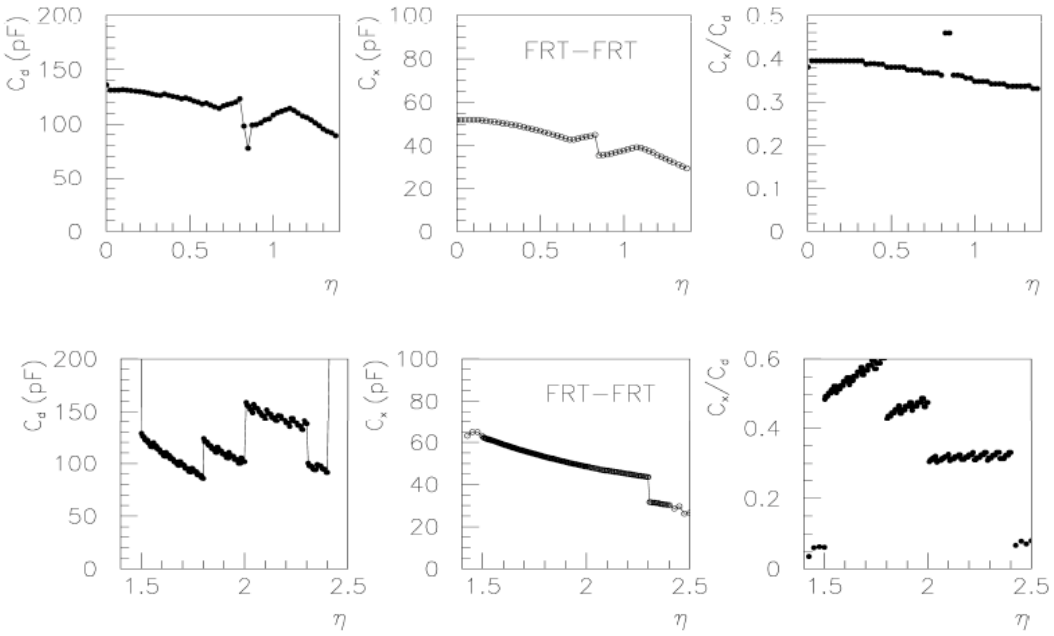


Figure 87 : detector (C_D) and crosstalk (C_X) capacitance in barrel and end-cap strips as a function of pseudo-rapidity

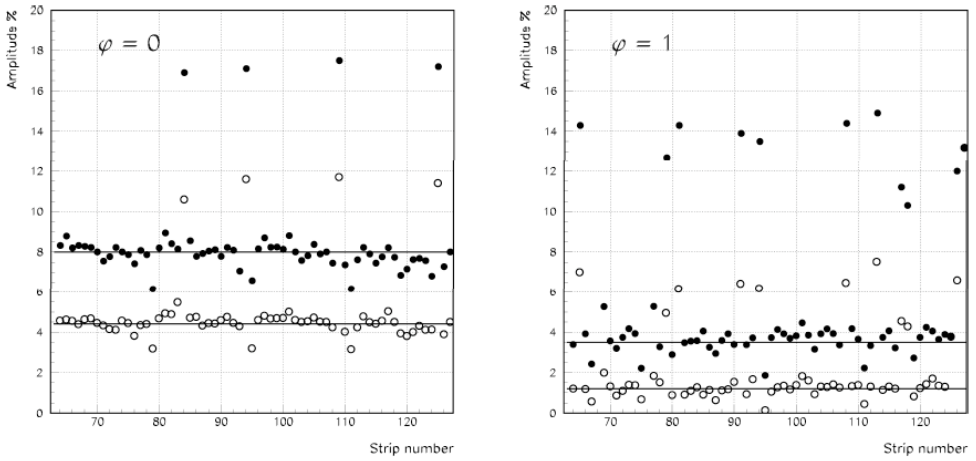


Figure 88: crosstalk over a complete barrel electrode. The high points correspond to a short in a high voltage electrode..

4.2. Noise crosstalk in the front (or noise correlation) and effect on γ/π^0 rejection (PhD Jacquier)

The relatively large crosstalk in the front section has two effects :
Broadening of the signal in adjacent strips
Noise coupling between preamps.

Both effects can affect the γ/π^0 rejection ratio, which relies on the shower width in the front section of the calorimeter. The relatively large crosstalk (8%) can thus degrade the typical ration of 3 that is critical in the H-> $\gamma\ \gamma$ process. Moreover, the large coupling capacitance (C_X = 40pF) can inject the noise of one preamp into its neighbour, leading to correlated noise, which had already had a sizeable influence on the rejection factor. Thus, the crosstalk waveforms and also noise correlation have been calculated and introduced in the reconstruction program in order to evaluate the impact on the performance. The crosstalk waveforms were given in § . For the noise, the modelization displayed in Figure 89 has been used. The series and parallel noise generators (e_n and i_n) are inserted at preamp input, at the end of the readout cable of length t_d. Part of the noise flows in the cable and couples to the neighbours through the crosstalk capacitance C_X. Thus the phase of the noise between the two channels is closely dependent on the cable length, leading to different results between cold and warm preamplifiers [17].

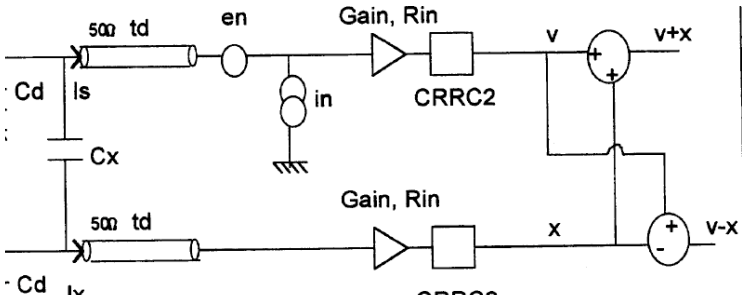


Figure 89 : correlated noise modelization

It can be seen in Figure 90 that the correlation factor is opposite between series and parallel noise and washes out when the line gets long enough compared to the shaping time. In the case of ATLAS, the line length is 25 ns, leading to a negligible correlation, which would not be the case with cold preamplifiers.

Finally, the effect of crosstalk and noise correlation has been added in the Geant3 simulation of the calorimeter to evaluate its effect on the γ/π^0 rejection factor and the effect has (fortunately) been negligible, as shown in Figure 91 [17].

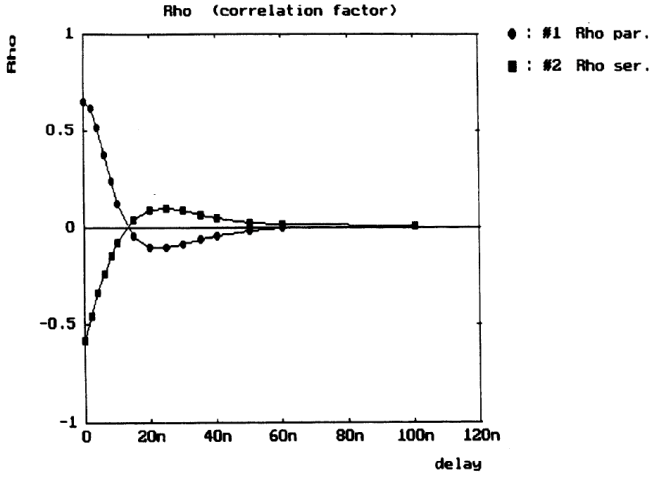


Figure 90 : noise correlation between two front neighbouring channels

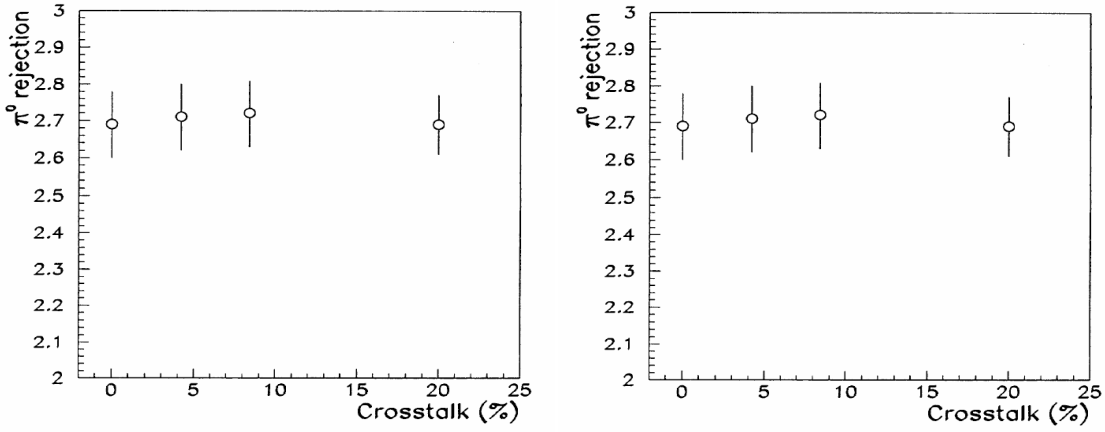


Figure 91: π^0 rejection factor as a function of crosstalk level. The left plot shows the impact of signal crosstalk and the right plot shows the effect of noise correlation. In ATLAS strips, crosstalk is 8%, leading to a negligible degradation

4.3. Resistive crosstalk and feedthrouhgs crosstalk

Any resistance between channels can couple crosstalk signals, with the same shape as the regular signals, although possibly inverted when the resistance is in the ground return connection. In ATLAS both versions were observed although rather unexpectedly.

The first type (non inverted) has been seen between Front and Middle electrodes, due to the large inked resistors that connect the high voltage to the front strips. Although of very high value (hundred of kΩ), many are in parallel which makes them not negligible compared to the preamplifier impedance.

The second type (inverted) was found in the first version of feedthroughs, were the ground connection is made through the flange with metal springs on the connectors. In the feedthroughs, there are so many pins that there was no way to have as many ground pins as signal pins (or even one for two) and it was chosen to use the bulk of the flange as ground return. Special connectors were designed by ATI company to have a low inductance connection to the flange of the pin carriers. Indeed, depending on the surface quality of the flange and on the spring pressure, a resistance of a few hundred mΩ could be (indirectly) measured[58], inducing long distance crosstalk.

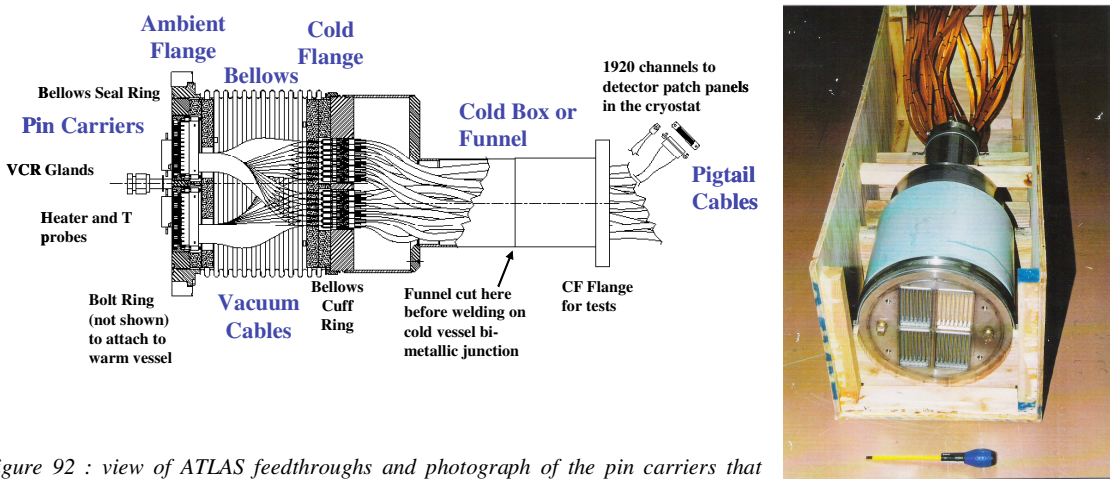


Figure 92 : view of ATLAS feedthroughs and photograph of the pin carriers that transmit signals while the ground return is taken on the walls of the flange.

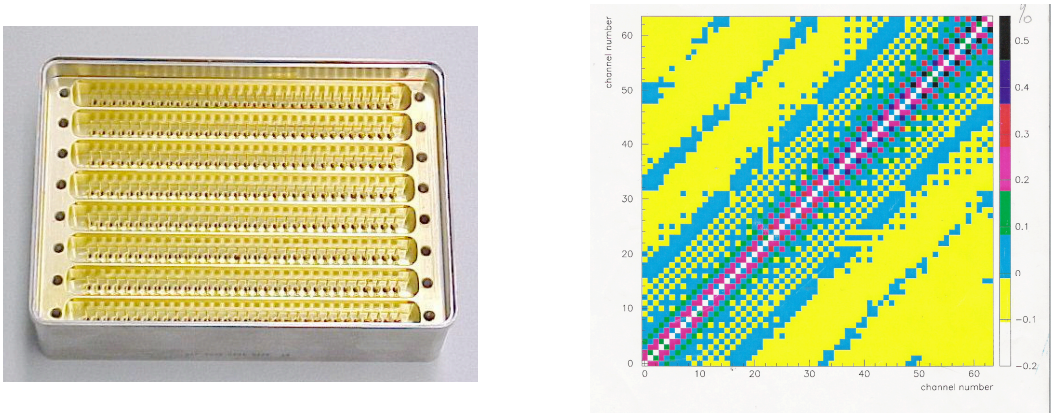


Figure 93 : pin carriers used on the feedthroughs to pass the signals.

∞

[58] The ground resistance is also affecting the calibration pulse amplitude depending on the number of pulsed channels. By measuring the amplitude as a function of the number of pulsed channels, the ground resistance could be computed with respect to the 50 Ω termination.

As a correcting action, all the pin-carriers and springs were gold-plated and the ground-resistance has been systematically measured on all feedthroughs with a similar setup as the detector impedance measurements.

4.4. Inductive crosstalk

The large and non uniform crosstalk in the middle section of the calorimeter came as a surprise, some channels were as high as 5% when 1% was the value commonly anticipated and was seen in several places. Also the crosstalk signal was much faster than the usual crosstalk signals which was intriguing. The puzzle is summarized in Figure 94.

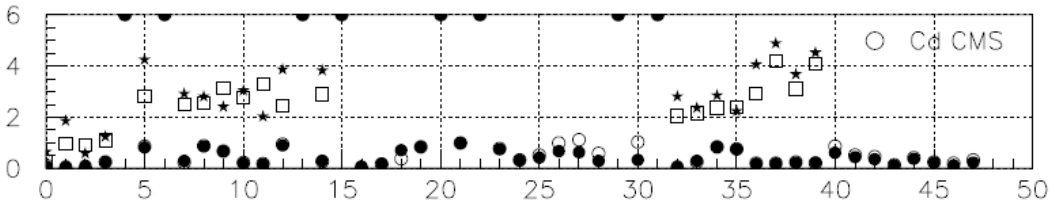


Figure 94 : Crosstalk (in %) as a function of channel number. The channels 4, 6, 13, 15, 20, 22 29 and 31 receive the calibration pulse. The stars are the testbeam data, the squares the testbench measurements and the circles are the same data with all cables and detector capacitors soldered on the motherboard, almost removing all crosstalk.

The measurements on testbench with soldered surface mount capacitors hinted at inductive effects and coupling by mutual inductance. This is very unusual in particle physics as the detector currents are very small and detector impedances very large. Here in ATLAS, the large detector capacitance and the short shaping time made it noticeable.

Three main contributors were found :

∞ Ground inductance. This was the main contributor, mainly due to an insufficient number of ground pins between summing boards and motherboards (one for 6 channels). The relative length of the connecting pins (5 mm) and their wide arrangement (over 3 cm) made a nice transformer ! (see Figure 95) The calculation showed that a few nH were giving % levels, in particular for the calibration pulse as two channels are pulsed simultaneously. The summing boards and motherboards were all redone such that each signal pin had its ground pin nearby.

∞ Ground apertures. A less obvious source of inductance in the ground return is the slits which are cut in the ground planes or the motherboards in order to leave the clearance around the low profile connectors. The effect can be seen in Figure 96 and explained why some channels remained high with surface mount capacitors soldered on the motherboard.

Mutual inductance coupling in connectors, in particular on the "low profile" connectors. This is illustrated in Figure 97. The negative polarity of the crosstalk signal is in good agreement with Lenz law and this kind of crosstalk couples further away than the first neighbour as it decreases very slowly with the distance, which is very annoying for making offline corrections. The only possible mitigation is by reducing the loop area, which has been done in ATLAS by designing special, smaller, "low profile" connectors. One particularly unfortunate bad configuration was observed when one calibration connector was nearby an output connector[59].

After these modifications, the crosstalk was everywhere below 1%.

∞

[59] In that case, the current in the « emitting » loop is much larger as the calibration drives a 50 Ω termination.

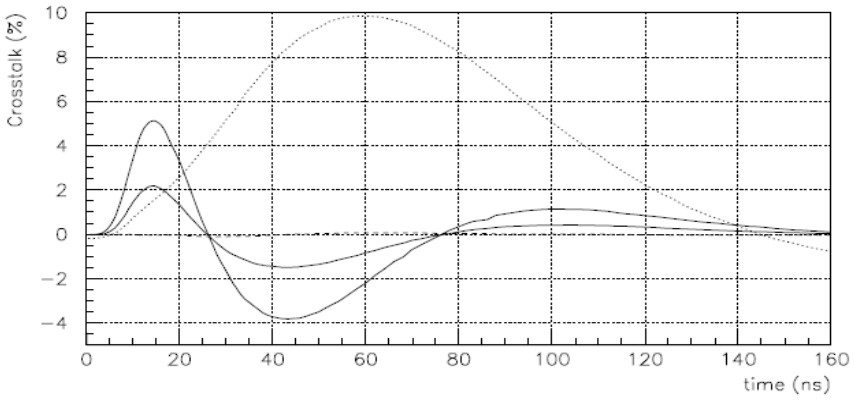


Figure 95 : crosstalk signals due to the inductive ground return between summing boards and motherboards shared by several signal lines.The two curves corresmond to channels closest and furthest away of the ground return. The dashed curve, almost invisible on zero shows the crosstalk signal when the detector capacitance is soldered directly on the motherboard.

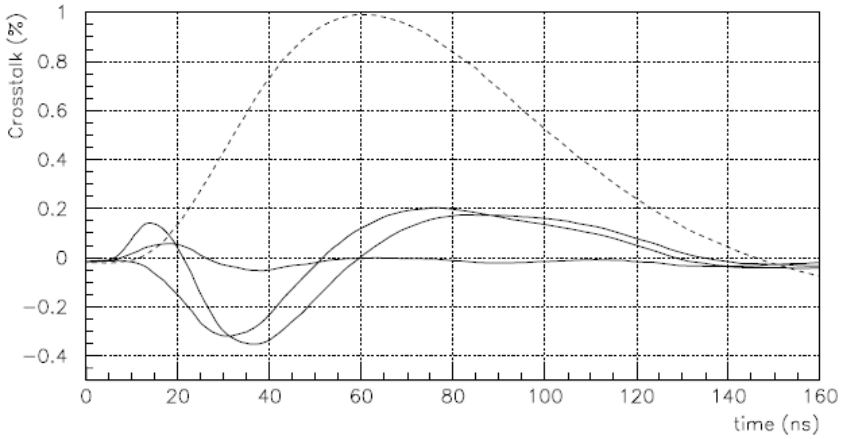


Figure 96: crosstalk due to ground apertures on the motherboard

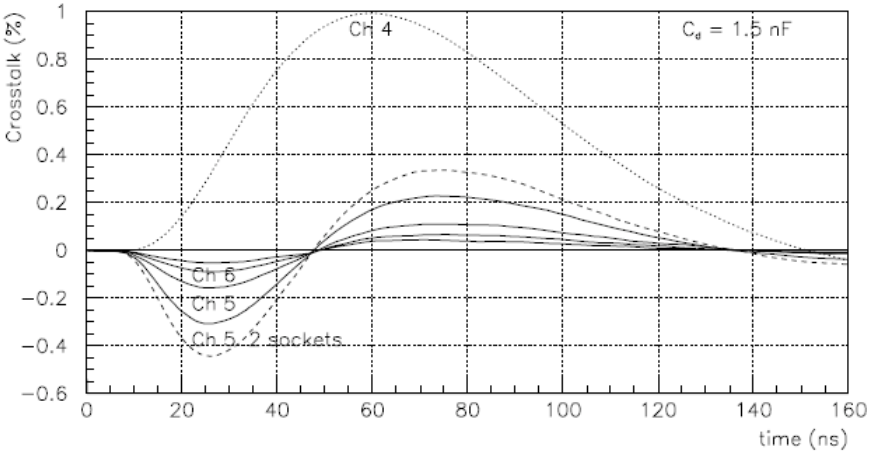


Figure 97 : crosstalk due to mutual inductance in the low profile output connector.

4.5. Summary on crosstalk

All these various sources have allowed to make a detailed cartography of crosstalk values all over the calorimeter, as displayed in Figure 98. Except in the front strips where its amount of 5-8% has been carefully analysed, it is everywhere below 1-2%. To achieve this small value regarding the fast shaping used, several sources have been found, analysed and corrected, often by redesigning boards or connectors.

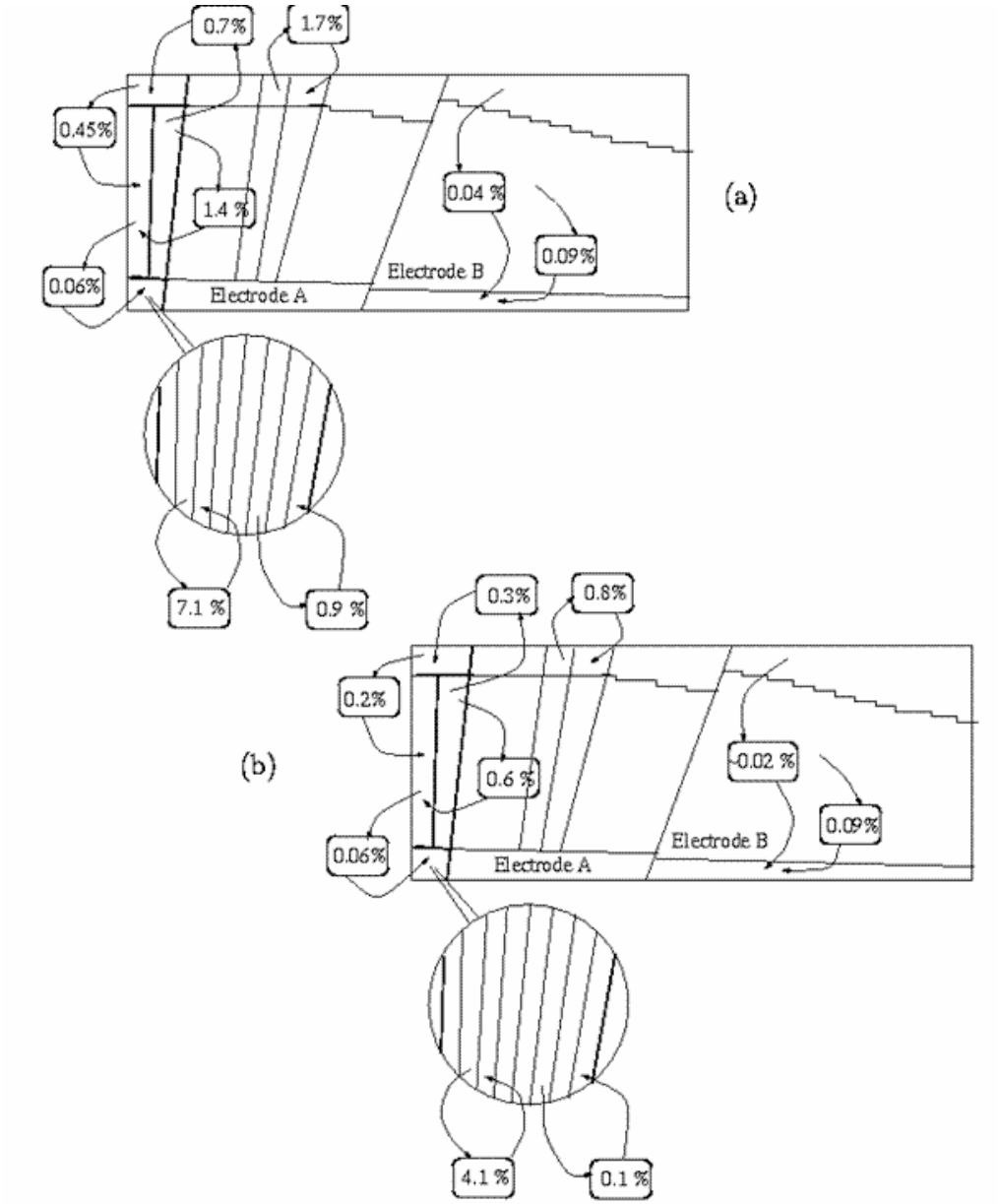


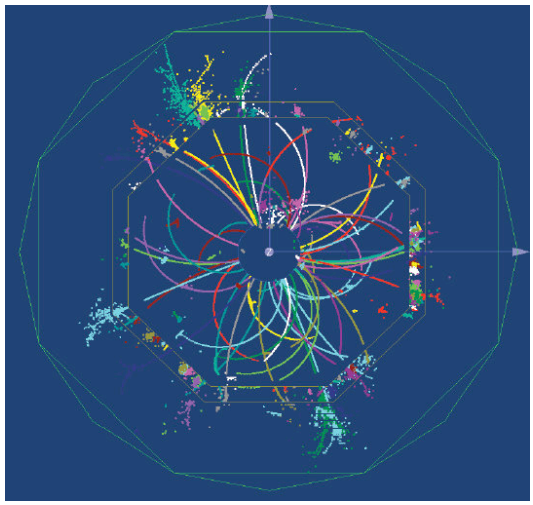
Figure 98: Crosstalk summary on Barrel and End-cap electrodes

CHAPTER 4

IMAGING CALORIMETRY AT THE ILC

1. Introduction (TDR ILC [18])

The next generation of colliders after the LHC is likely to be an International Linear Collider (ILC) with electrons that will be a worldwide experiment. The location between the 3 regions (America, Europe and Asia) is bitterly disputed among the nations, the budget is a hotly debated subject and the schedule varies between 2015 and 2025. However, the physics requirements are clear and the detector design are well defined and challenging enough to start the R&D work.



The calorimeter plays a central role in the detector for a linear collider. The proposed designs feature unprecedented detector granularities which require the exploration of novel technologies (e.g. for photo-sensors) and the collection of large test beam data samples to validate the simulations. Significant developments are ongoing in the world to develop these technologies. In particular the CALICE collaboration has formed over the past few years, with the goals of building and testing a first version of a "particle flow" calorimeter[60].

A comprehensive optimization of the calorimeter for the ILC depends on a number of factors. The ansatz of a "particle flow" calorimeter first proposed

∞

[60] The particle flow technique, proposed by *JC Brient* and *H. Videau* in 1990? proposes to optimize the jet resolution by cleanly separating and identifying the different constituents of the jet (charged, photons and neutrals) and measuring them with the detector that gives the best resolution (tracker for charged, ECAL for photons and hadron calorimeter for neutrals). The goal is to obtain a resolution down to 30%/√E

for the ILC by a European group requires to obtain the best possible separation between photons, neutral and charged hadrons. For the first about 20 radiation lengths of calorimeter a baseline solution exists based on the use of tungsten as absorber and Si-sensors for the readout. For the largest part of the calorimeter however many different options exist, with very different trade-offs between performance and cost. Progress in the field of large area readout systems, either through gaseous systems like resistive plate chambers (RPC) or through scintillator based systems, is extremely rapid.

In order to address efficiently and fairly the R&D on calorimeters for particle flow implementation, the worldwide efforts have been coordinated by the CALICE collaboration, chaired by *F. Sefkow* [19]. This collaboration which gathers 280 scientists in 42 laboratories and 11 countries allows to develop and compare in fair conditions the different options of calorimeters that are considered for the ILC.

To progress rapidly on the validation of the concept, CALICE has chosen to separate very early two paths of R&D

∞ Physics prototype to validate simulation models and check the performance of the various detectors in testbeam. This prototype was designed to check the physics and not the technology and not mingle technological studies with physics studies. Thus it is of reduced size (0.2 m cube for the ECAL, cubic meter for the DHCAL) conservative options have been taken for the readout, with electronics outside the detector.

∞ Technological prototype to study the feasibility of large scale, industrializable, affordable modules. This axis has received the support of a FP6 European Infrastructure program called EUDET [20]

The physics prototypes have been designed in 2003-2005 and have been in test beam since then at DESY, CERN and FNAL as shown in Figure 99 producing heaps of good data for physics analysis.

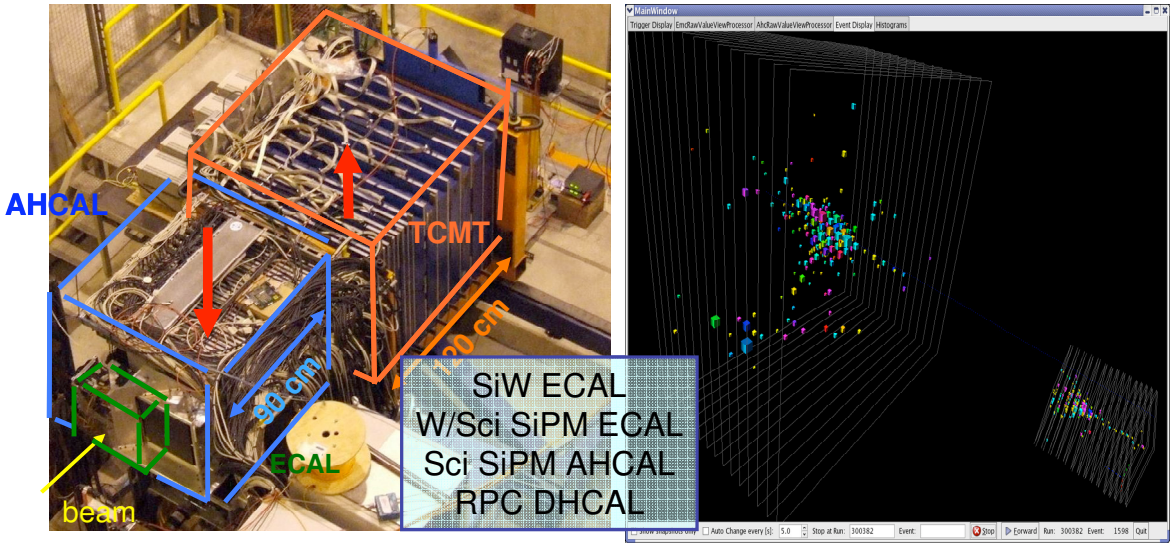


Figure 99: view of CALICE physics prototypes in testbeam at CERN in 2004

The technological prototype addresses the integration issues, which are extremely challenging for the electronics : how to read hundred millions of channels, inside the detector, with calorimetric performance i.e. high precision, large dynamic range. Compared to LHC readout, space and power dissipation need to be brought down by 4 orders of magnitude ! For space, this can be achieved through microelectronics

integration and for the power it exploits the duty cycle of the beam shown in Figure 100, together with on-detector zero suppression[61].

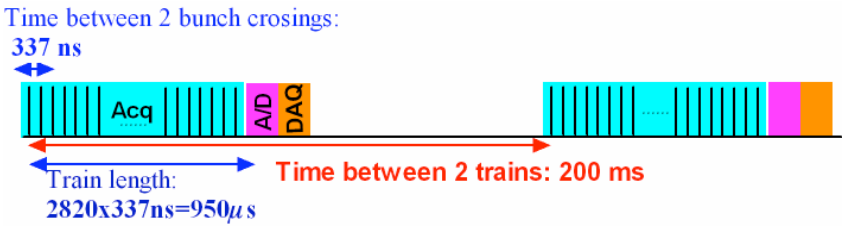


Figure 100 : ILC bunch structure. The collisions take place during trains of 1 ms separated by a 200 ms inter-train during which the readout is performed and the electronics switched off.

All these features now need to be demonstrated ! Comparing with the ATLAS readout electronics shows the size of space and power reduction (Figure 101), while maintaining similar calorimetric performance[62].

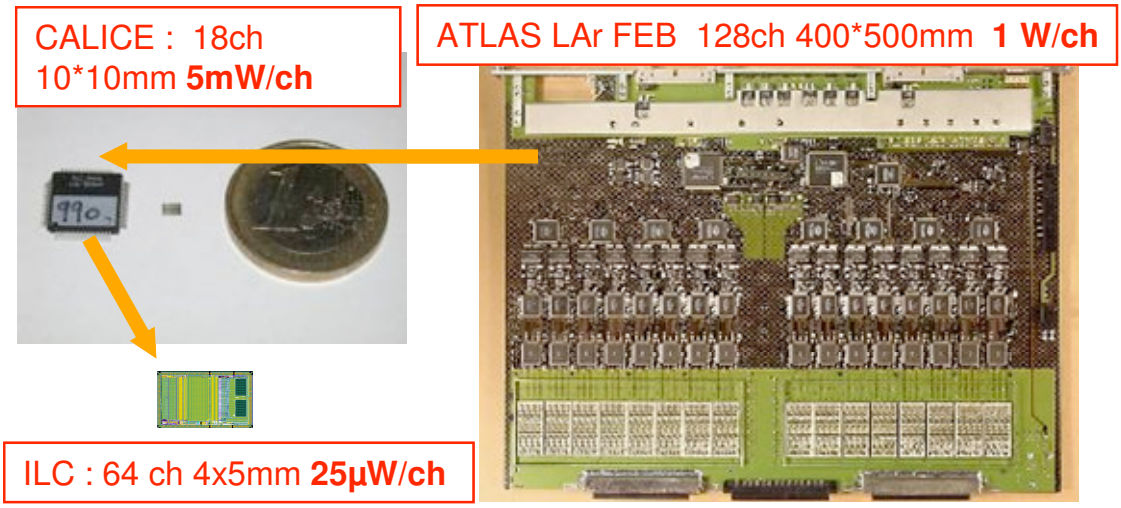


Figure 101 : Sketch comparing the 128 channels ATLAS LA front-end board, to the chips used in CALICE and the ultimate version for ILC. Four orders of magnitude need to be gained both in area and in power dissipation, which should be achieved thanks to the low duty cycle and low occupancy of the ILC collider compared to the LHC.

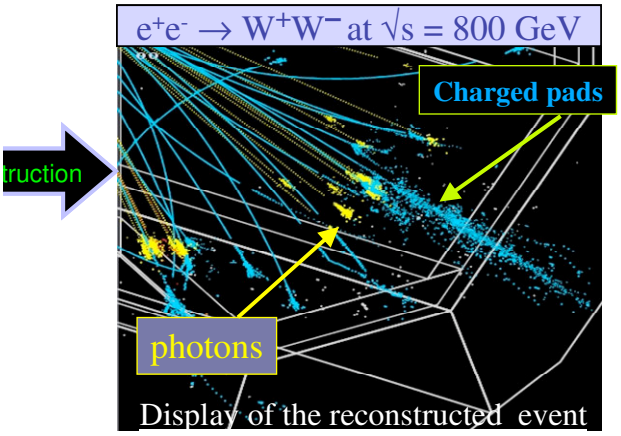
∞

[61] With a bunch duration of 1 ms every 200 ms, a factor 200 can be obtained by shutting off the electronics during inter-bunch (provided it can be tuned on fast enough). The other factor 100 (as compared to LHC) comes from digitizing and sending-out only data above ½ MIP and takes advantage of the low occupancy of leptonic collisions.

[62] Similar in terms of dynamic range and accuracy. A large difference comes however from the collider structure which is almost continuous at LHC while it exhibits a 0.5% duty cycle at ILC allowing a factor 200 power reduction. The other main difference comes from the occupancy as cross sections are order of magnitudes lower in leptonic collisions compared to hadronic ones. This low rate of events allows to to perform on-detector zero-suppression and reduces the bandwidth of the DAQ and hence the power necessary to readout the data.

2. Electromagnetic calorimetry

A prime candidate for the electromagnetic calorimeter technology is Silicon Tungsten as it combines good resolution with very small *Moliere* radius[63] (1 cm) which is essential to obtain a clean separation of electromagnetic showers. As the good *Moliere* radius of Tungsten is quickly deteriorated when the sampling material gets thicker, all the silicon and readout electronics need to fit in a thickness around 1 mm. Besides, detailed simulations have shown that to have good performance of the PFA, the cell size should be smaller than 1 cm², with a sampling in depth around 30-40 layers, hence the name of *"imaging calorimetry"*.



The physics prototype has been built in 2003-2004 by LLR. The technological prototype, called EUDET module as it was funded by the European FP6 program EUDET , addresses the issues of large scale realization. It has been started in 2006 and should be completed in 2009 and is essential to assess the feasibility of the electronics

2.1. Physics prototype and FLC_PHY3 ASIC

The physics prototype built to validate the particle flow concept is a 18x18x20 cm³ Silicon-Tungsten calorimeter, shown in Figure 102. It is built with 30 layers of front-end boards called slabs which realize a $20X_0$ calorimeter with fine sampling in depth and granularity totalizing 9600 readout channels. The detector is described in more details in [21]

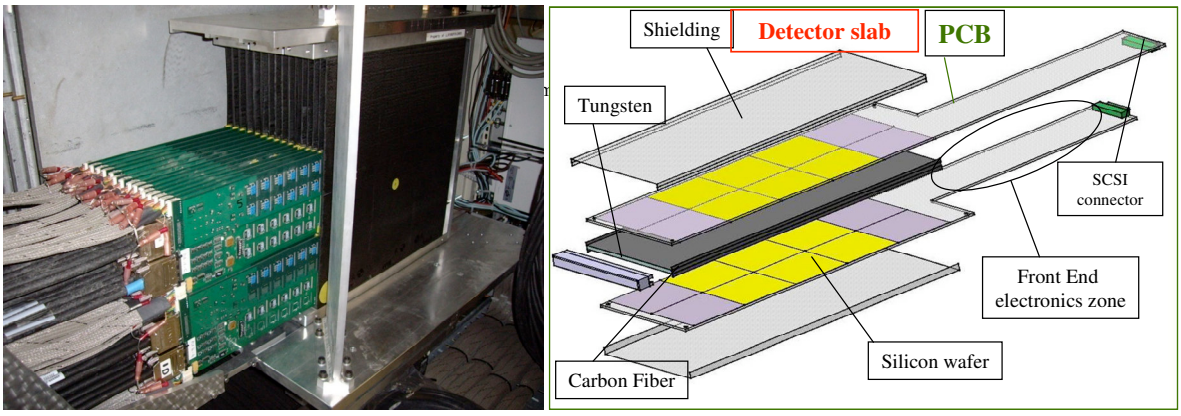


Figure 102 : view of the complete ECAL physics prototype (left) and split view of one detector slab (right)

One slab houses 6 wafers of 36 Silicon diodes of 1 cm² and 525 µm thickness, giving a MIP signal of 40 000 e- (6.4 fC). They have been produced by Russian and Tcheque producers and tested at LLR before being glued on the PCB. The PCBs that support 6 wafers and readout electronics have been designed at LAL, they are 14 layers to minimize crosstalk and have been produced by our Korean collaborators.

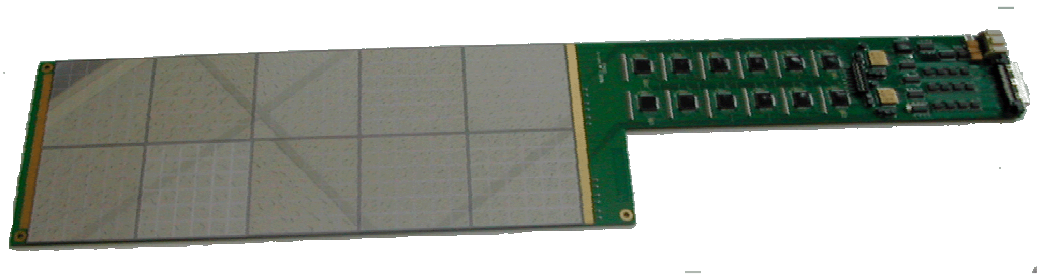


Figure 103: front-end board of the CALICE SiW physics prototype.

The Silicon pads are read by an 18 channel dedicated ASIC called FLC_PHY3, developed at Orsay in 2002-2003 that performs low noise charge amplification, shaping, track and hold and multiplexed output. The multiplexed signals are digitized in the DAQ by 16 bits ADCs developed by *P. Dauncey* et al. (Imperial College London).

2.1.1. FLC_PHY3 Chip architecture

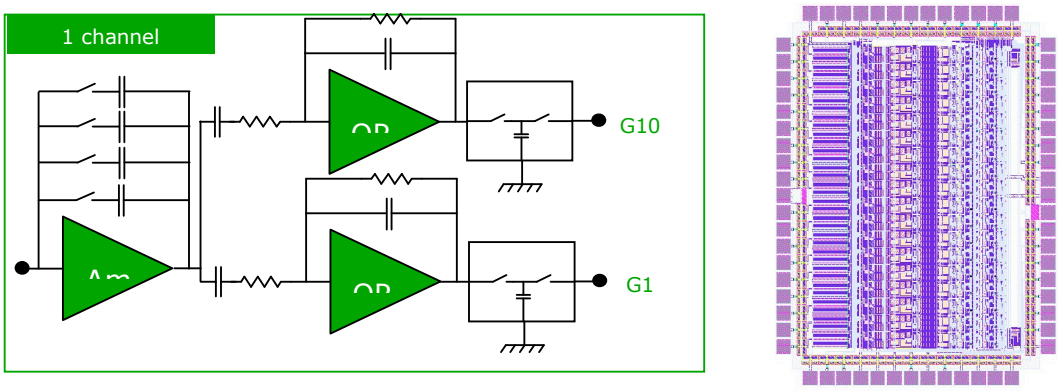


Figure 104: synoptic of FLC_PHY3 and layout in BiCMOS 0.8 µm (2003)

The chip architecture is built around a low noise variable gain charge preamplifier followed by a by-gain CRRC² shaper, a Track and Hold and an output multiplexer. The chip houses 18 channels, matched to a half detector wafer and is realized in 0.8 µm AMS BiCMOS technology. 1000 circuits have been produced at the end of 2003 and are packaged in TQFP64.

The charge preamplifier is a classical folded cascode architecture with a 3000/0.8 input PMOS which exhibits a transconductance of 8 mA/V and a noise spectral density of 1.6 nV/√Hz at I_D = 0.9 mA drain current. The DC feedback is realized with a 36 kΩ resistor multiplied by 625 by a set of current mirrors, achieving an effective feedback resistance of 22 MΩ, while keeping good linearity. The "gain" (feedback capacitance) can be varied from 0.2 pF to 3 pF in 4 bits, the rise time can also be tuned by changing the

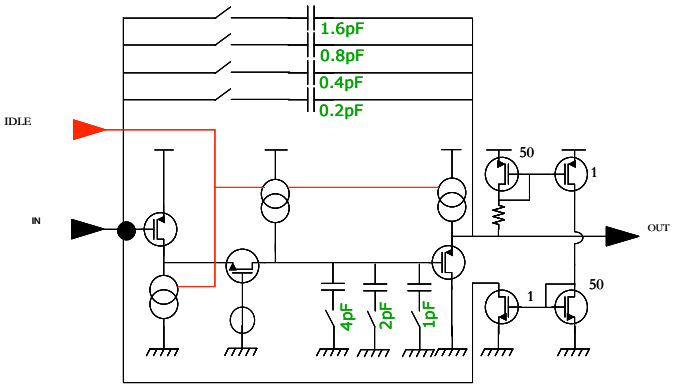


Figure 105: schematic diagram of FLC_PHY3 preamplifier

dominant pole capacitance by a similar ratio.

The following stages are taken from the previous ASIC OPERA_ROC (*cf* Chapter 5, § 3) developed for multi-anode photomultiplier readout of the OPERA neutrino experiment. The shaper uses a differential configuration in order to reduce the pedestal dispersion at the output and is built around a *Sallen-Key* architecture with a peaking time of 180 ns. The track and hold is also similar to OPERA_ROC with a 1 pF storage capacitor and a CMOS switch followed by a *Widlar* differential buffer for low offset ; it is read-out sequentially by an OTA in follower configuration.

2.1.2. FLC_PHY3 measured performance

The output waveforms for the various gain settings are shown in Figure 106. The gain can be varied with 4 bits on a range of 16, while keeping the signal shape very constant. The linearity of the gain adjustment is better than 1%, with a "slope" of 1.65 V/pC and an "offset" of 25 fF.

The noise of the preamplifier alone has been measured via a dedicated "test output" followed by a variable CRRC^2 shaper []. It follows nicely the fitted curve with series noise and 1/f noise. By varying the detector capacitance, one can extract the noise spectral density and the input capacitance, yielding : e_n=1.6 nV/√Hz and C_{PA}=25 pF from which the test board accounts for 15 pF.

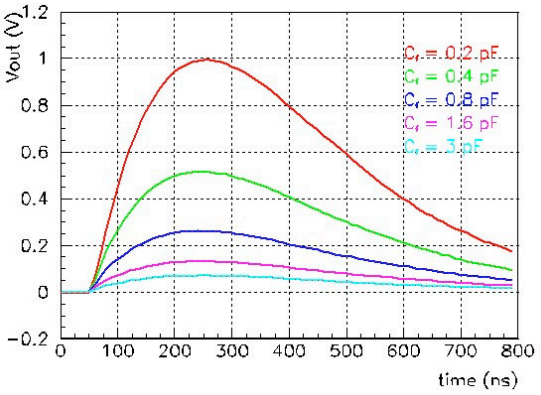


Figure 106: shaper output waveforms for various preamp gains

At tp=150 ns, the equivalent noise charge is measured as ENC = 1000 + 30 e-/pF. Thus with a detector capacitance of 70 pF (25 pF for the Si diode and 20-50 pF for the PCB line) the total noise is expected to be around 3500e- < 1/10 MIP. The preamplifier maximum output voltage is 3 V, corresponding to 600 MIPS with a feedback capacitance of 1.6 pF. All further plots below are shown with C_F = 1.6 pF.

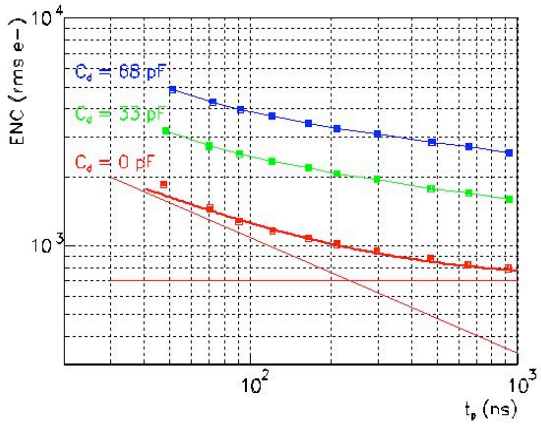


Figure 107: Preamp equivalent noise charge (ENC) as a function of shaping time for various external detector capacitance

The shaper is split in two gains 1 and 10, although mostly the gain 1 will be read out. The gain 10 is provided to possibly enhance the dynamic range and accommodate other detectors. Gains are given for a preamp feedback of 1.6 pF.

The unity gain gives a signal of 696 mV/pC (5 mV/MIP) with a uniformity of 3% *rms*, the peaking time is 189 ns with a *rms* of 2 ns. The pedestals exhibit a dispersion of 4.8 mV *rms*.

The gain 10 gives a signal of 6294 mV/pC (45 mV/MIP) with a uniformity of 3% *rms*, the peaking time is 174 ns with a *rms* of 2 ns. The pedestals exhibit a dispersion of 8.3 mV *rms*. In both gains, the crosstalk is smaller than 0.2%.

2.1.3. Overall performance

The overall linearity has been measured for the various gain settings and is well within ± 0.2% up to an output voltage of 2.5 V. Residuals for a linear fit are shown in Figure 108 for the nominal configuration of C_F =1.6 pF and unity gain.

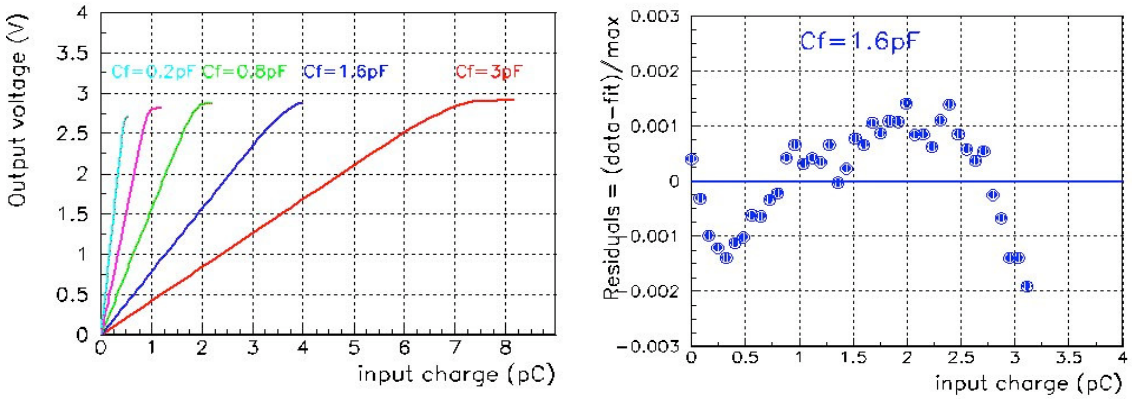


Figure 108. Left : output voltage as a function of input charge for various gains.
Right : Linearity of the readout in the CALICE setup (C_F = 1.6 pF)

The noise in this nominal configuration, with a total detector capacitance of C_D = 68 pF (including PCB contribution of 47 pF) is 400 µV in G1 and 200 µV without detector capacitance. The dynamic range is thus around 6500 (12.5 bits) with the detector and 13000 without (13.5 bits). Using the bi-gain readout with the gain of 10, the dynamic range can be extended to 14-16 bits.

The MIP signal is clearly visible, with a signal to noise around 8, through the full readout, as shown in Figure 109

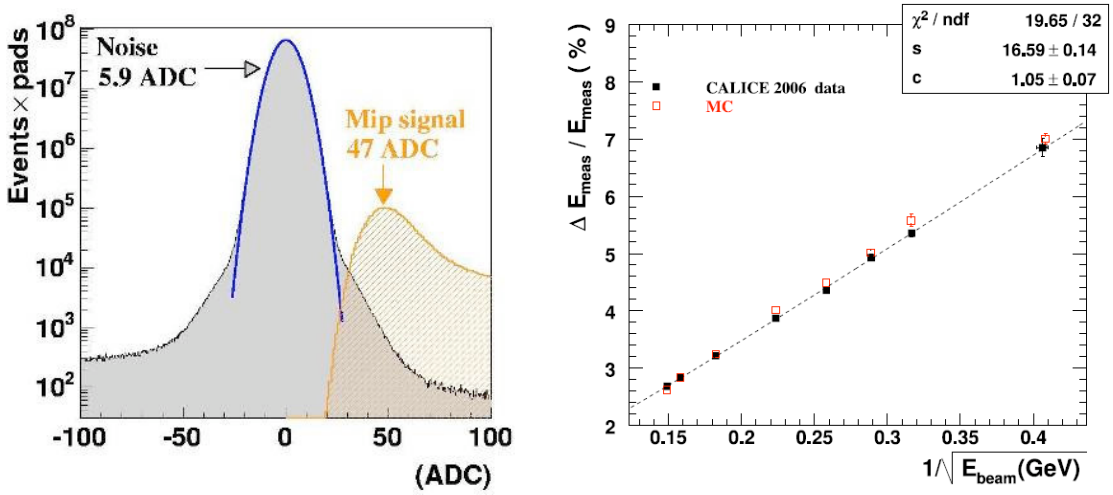


Figure 109. Left : MIP signal and noise histogram. The MIP/noise ratio of 8 allows to cut away signals below ½ MIP in the analysis. Right : preliminary energy resolution obtained at CERN testbeam.

.

2.2. Technological prototype : EUDET module and SKIROC ASIC

The EUDET module addresses several issues crucial to build a detector that can be used at the ILC, in particular in what concerns going to large scale. The issues are the following :

Integration of the front-end electronics inside the detector without cooling

Producing and connecting elementary front-end boards (called ASU for Active Sensor Unit)

Triggerless operation : self-trigger on 1/2MIP = 12 000 e-. Low noise fully integrated readout ASIC with pulsed power and data storage and digitization inside the chip.

Sparsified DAQ with minimum number of lines to enable connection between boards.

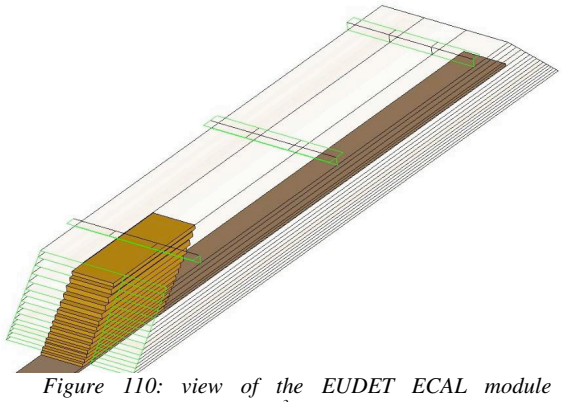


Figure 110: view of the EUDET ECAL module of dimensions 180x50x30 cm^3

2.2.1. Front-end boards

The front-end boards called ASU (Active Sensor Unit) hold the sensing wafers, the readout electronics and bring the signals outside as shown in Figure 111. As thickness is a crucial parameter, it is limited to 800 μm which precludes the use of any external components and imposes to insert the chip as a bare die inside a cavity dug into the PCB. The electrical connections between ASUS are also much complicated by this constraint and this limits to a bare minimum of 100 lines the number of signals that are coming to the outside.

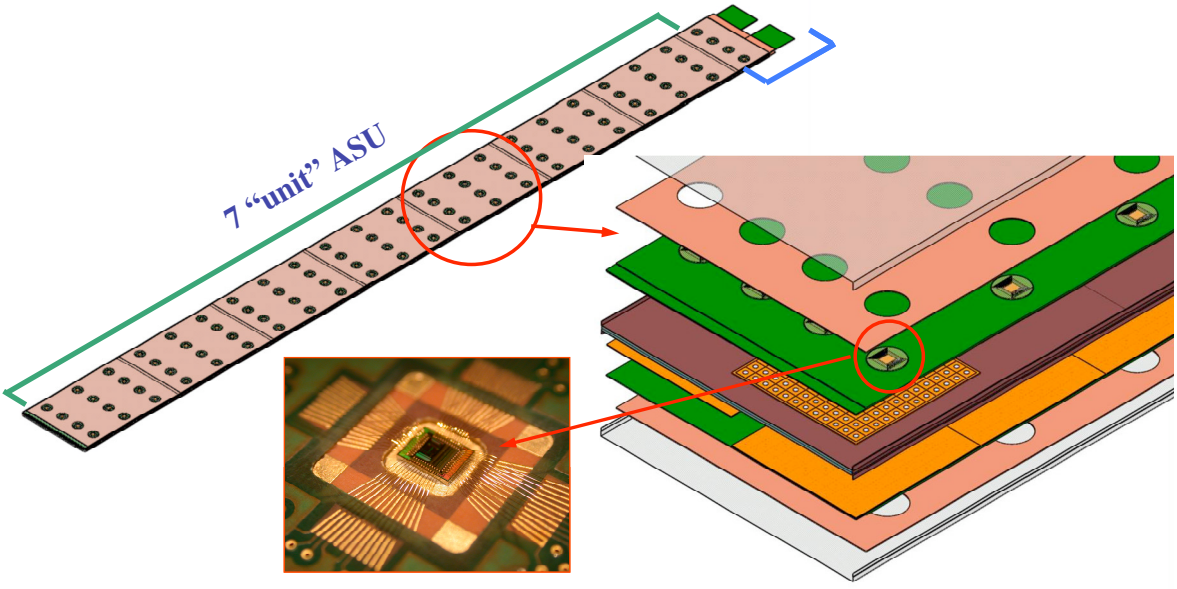


Figure 111: detail of the front-end boards used to form a slab

The technological challenge of realizing such PCBs was fully realized in 2008, when after almost a year of tentatives by various companies in several countries, the results did not meet the requirements, as shown in Figure 112. In particular, the gold plating of the pads receiving the bonding wires roved out to be extremely difficult to perform due to the cavity and the two staggered layers of receptacles to accommodate the bonding of staggered pads on the HaRDROC ASIC[64].

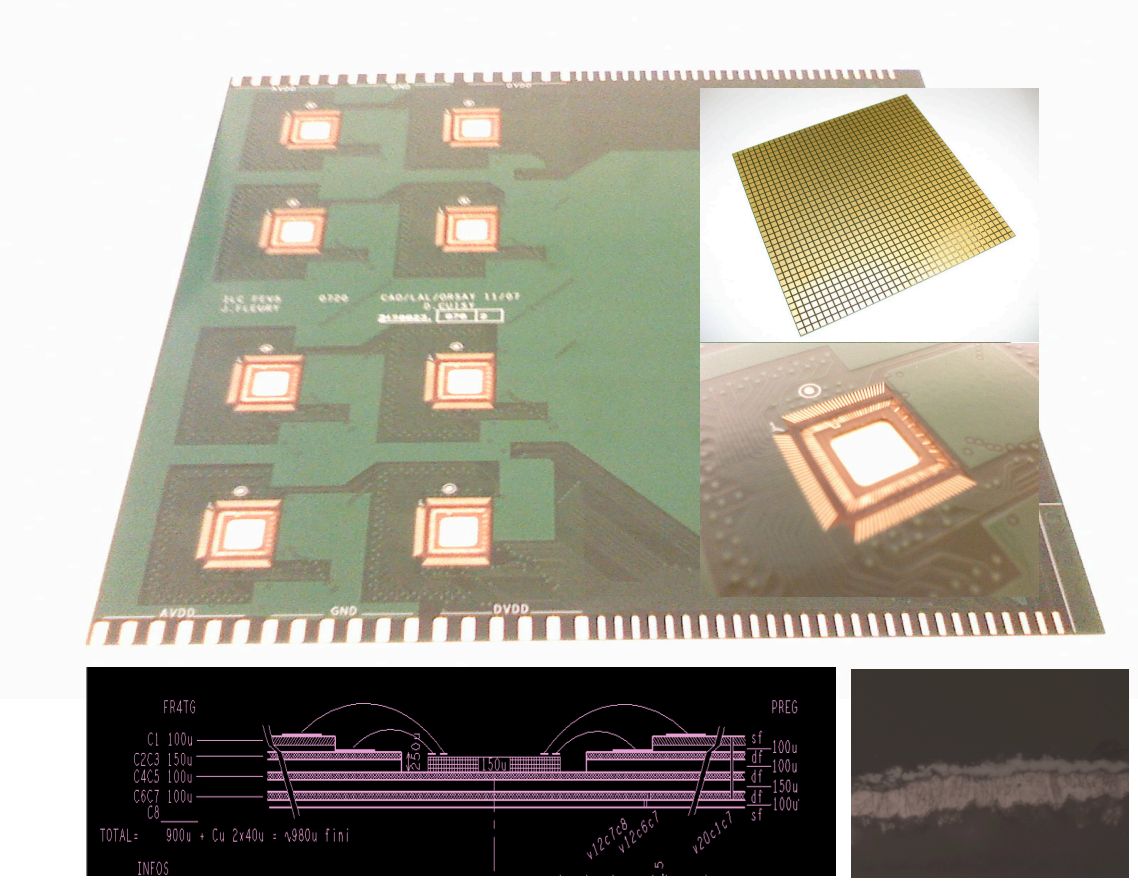


Figure 112: photograph of FEV5. This Front End Board which matches EUDET dimensions can accommodate 4 wafers of 9 x 9 cm² with 324 channels each. One wafer is readout by 4 HARDROC chips which are bonded in a cavity inside the PCB. This allows the total thickness of the PCB and its readout electronics to remain around 1 mm. The bottom right metallurgical curve shows that the gold plating was too thin to allow proper chip bonding on this PCB.

2.2.2. SKIROC1 ASIC architecture

The analogue core of SKIROC (Silicon Kalorimeter Integrated Read-Out Chip) is based on the front-end electronic designed for that physics prototype. It has been enhanced in many ways using an intermediate prototype called ILC_PHY4. The maximum input charge has been extended from 500 to 2000 MIP. The number of channel has been doubled – reaching 36 - to fit a pad size reduction[65] in the silicon detector design conducted concurrently. A stand alone working capability comes along with the full power pulsing feature. That means SKIROC does not need any external component such as decoupling

[64] The FEV5 board was realized with HARDROC as SKIROC was not yet available for detector characterization. Hardroc, although not fulfilling the sensitivity requirements of the ECAL could at leas allow to test the readout scheme.

[65] The pad size has been reduced to 5x5 mm² in order to improve the particle identification algorithm

capacitance or bias resistor involving a huge room saving. Its synoptic diagram is shown in Figure 113. The first prototype has been realized in may 2006 in SiGe 0.35 µm and it covers an area of 20 mm². Due to lack of time, the digital part has been left outside and requires an external FPGA to operate.

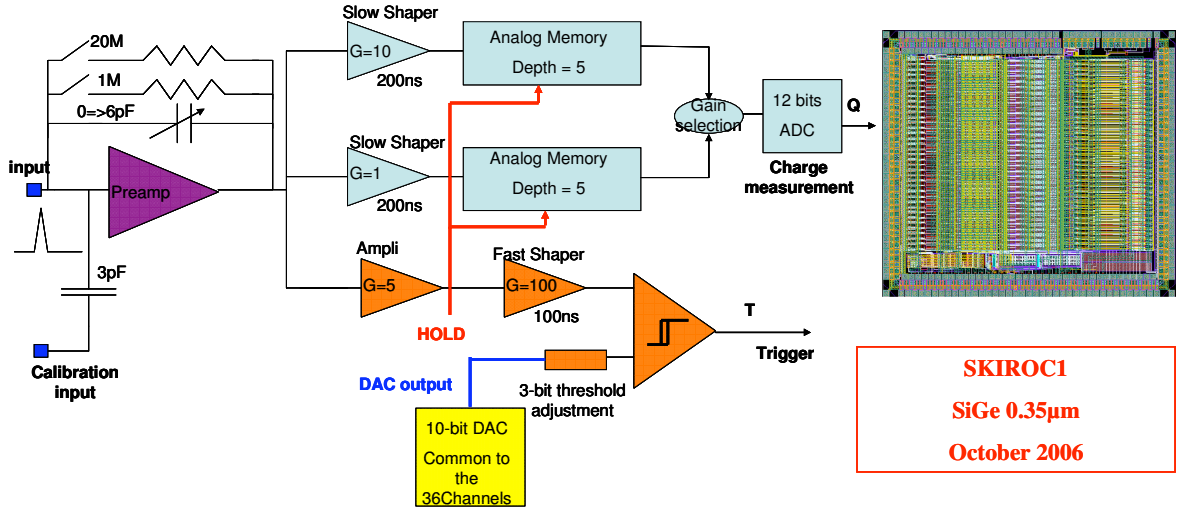


Figure 113: synoptic diagram of 1 channel of SKIROC1 and chip layout

As shown in the synoptic diagram of Figure 113, each channel is made of a variable-gain low-noise charge preamplifier followed by both a dual shaper – one with a gain 1 and the other with a gain 10 - to filter the charge measurement and a trigger chain composed of a high gain fast shaper and a discriminator. The measured charge is stored in a 5-depth SCA that can be read either in an analogue way or can be connected to a multi-channel 12 bit *Wilkinson* ADC. Thresholds are set with a 10-bit DAC for trigger level and for automatic gain selection level. A bandgap ensures the stability versus supply voltage and temperature for all the requested reference in the analogue core.

2.2.3. SKIROC1 Blocks measurements

The analogue core of SKIROC is mainly inspired from ILC_PHY4 front-end chip prototype. The equivalent noise charge of the preamplifier is measured around 2000 electrons. After shaping, the simulated MIP to noise ratio is 16 for the trigger line and 11 for the charge measurement.

Crosstalk is around the per mil level.

The 12-bit 36-channel ADC is a Wilkinson using a full differential structure.

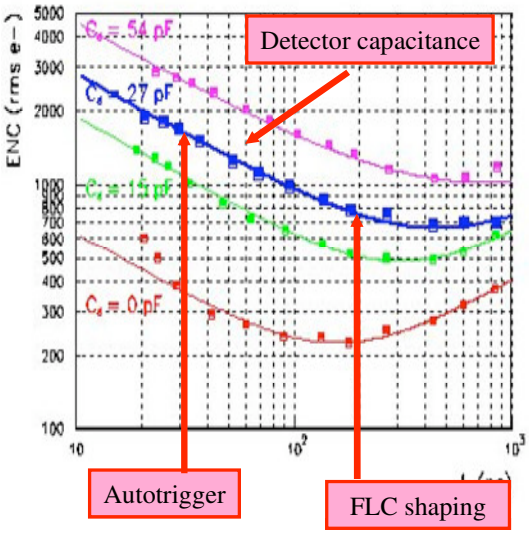


Figure 114 : Equivalent Noise Charge of the preamplifier as a function of shaping time, as measured on the ILC-PHY4 chip.

3. Digital Hadronic calorimeter (DHCAL)

With the very fine granularity foreseen at the ILC and the much larger size of hadronic showers, it has been recently shown in simulation by *JC Brient* et al.[66] that digital calorimetry would give a similar (nay even better) than analog one, provided the cell size could be brought down to around 1cm². Although the simulations look convincing, the proof has still to be made and this is a very important part of the CALICE R&D program.

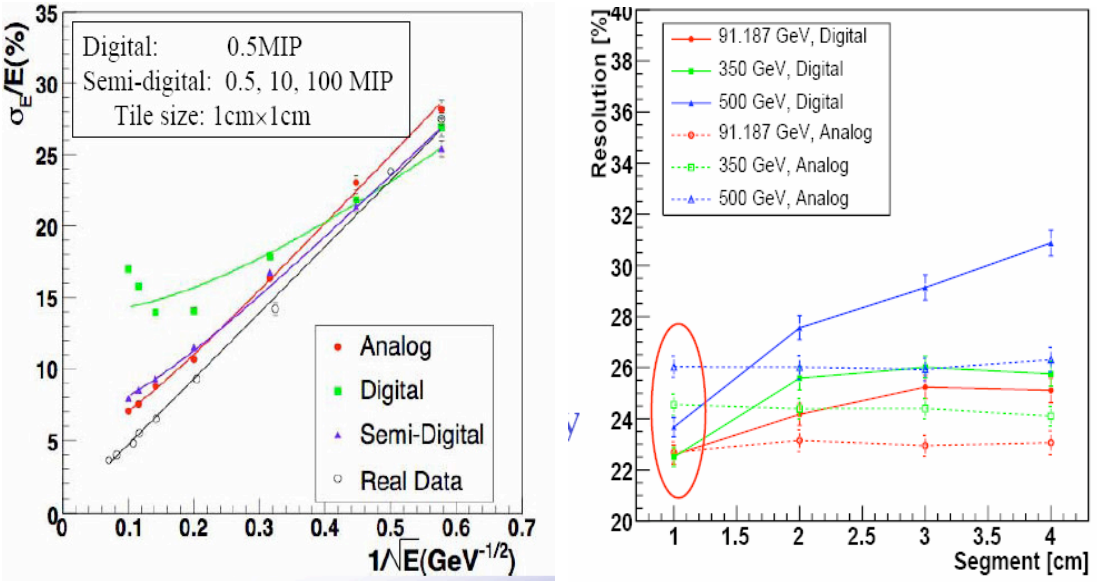


Figure 115. Left : simulated energy resolution for analog, digital and semi-digital hadronic calorimeters between 100 and 3 GeV. The semi-digital option with three thresholds gets the best performance at both low and high energy. Right : resolution at different energies as a function of pad size. The best performance is obtained for 1 cm² pad size.

At the beginning, a cubic meter of DHCAL physics prototype was to be realized along with the ECAL and AHCAL and tested in beam to allow the choice between analog and digital HCAL. This physics prototype, which was mostly in charge of the US groups led by *J. Repond* (Argonne) used RPC or GEM detectors, but was unfortunately delayed by repeated budget cuts and could not proceed at the same pace as the ECAL or AHCAL.

It was then decided by the CALICE collaboration to proceed on the European side with the technological prototype (with similar goals as the ECAL or AHCAL EUDET modules) but while also allowing going in testbeam with a cubic meter prototype. This European DHCAL, led by *I. Laktineh* (IPNL) has received an ANR funding in 2006 and support from Spanish and Russian groups. It will be built with large area RPCs (and/or MicroMegas chambers) and be compatible with the ECAL and AHCAL EUDET modules[67].

This detector, for which 400 000 readout channels will be necessary, was an excellent starting point for developing the readout of all the calorimeters, as it is simpler than the two others having no ADC inside. In October 2006, HARDROC ASIC was developed to perform the read-out. Subsequently, another ASIC (DCAL) developed by Fermilab was designed and produced in 2009 to equip the US physics prototype.

∞

[66] and vigorously contradicted by *R. Wigmans* et al

[67] the DHCAL was not funded by EUDET, except for its electronics frontend

HARDROC has been retained to equip the European DHCAL and study technological prototype issues such as power pulsing, highly integrated and reliable readout.

3.1. HARDROC1 ASIC description

HARDROC1 (HAdronic Rpc Detector ReadOut Chip) is the first prototype of the second generation ASICS for (DHCAL) of the future International Linear Collider. HARDROC readout is a semi-digital readout with two thresholds (2 bits readout) which allows both good tracking and coarse energy measurement, and also integrates on chip data storage.

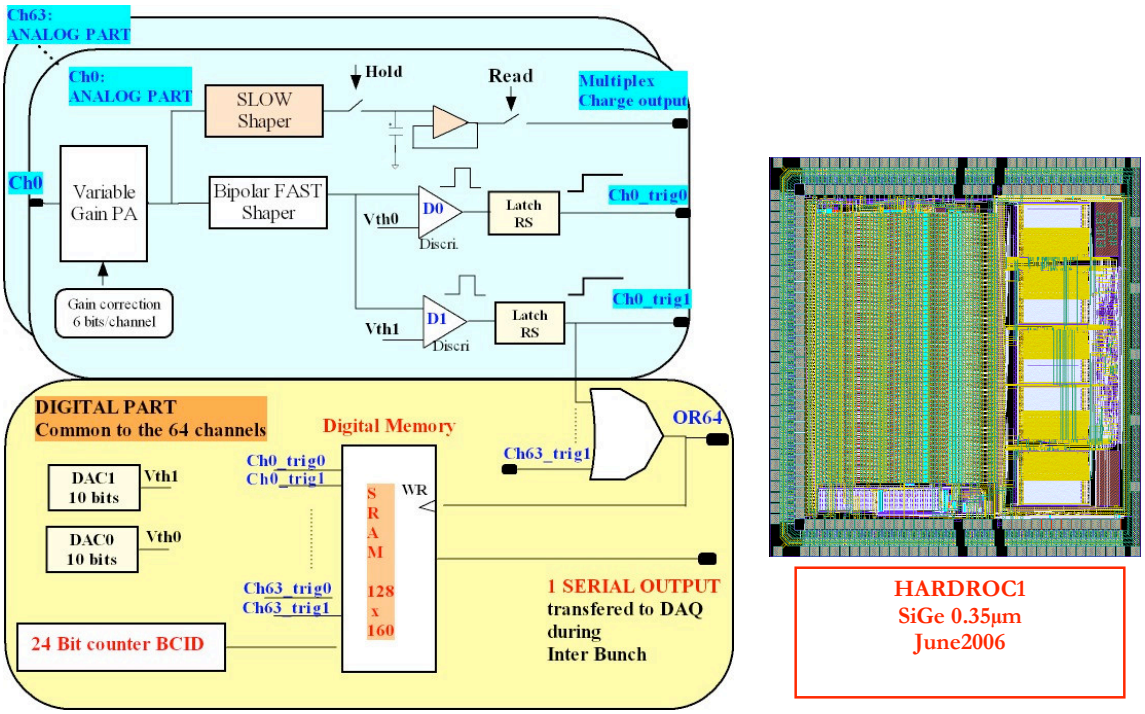


Figure 116: synoptic diagram of HaRDROC and chip layout

The 64 channels of the ASIC are made of :

- ∞ Fast low impedance preamplifier with 6-bit variable gain (tuneable between 0 and 4)
- ∞ Variable shaper (50-150 ns) and Track and Hold to provide a multiplexed analogue charge output up to 10 pC that is used for diagnostics and other applications (medical imaging)
- ∞ Variable gain fast shaper (15 ns) followed by two low offset discriminators to auto-trigger down to10 fC. The thresholds are loaded by two internal 10 bit DACs.
- ∞ A 128 deep digital memory to store the 2*64 discriminator outputs and bunch crossing identification coded over 24 bits counter.

HARDROC1 has been fabricated in AMS SiGe 0.35µm technology in September 2006. It has an area of 16mm² and is packaged in CQFP240 package.

3.1.1. Chip design

The block diagram of the ASIC is given in Figure 117 and is similar[68] to the MAROC chip designed for multi-anode photomultipliers (*cf* Chapter 5 §2). Each input signal is first amplified thanks to a variable gain current-sensitive preamplifier which exhibits low noise and low input impedance to minimize crosstalk. It allows to tune the gain depending of the detector choice, up to a factor 4 to an accuracy of 6% with 6 bits. The amplified current then feeds a slow shaper combined with a Sample and Hold buffer to store the charge and provide a multiplexed charge output (5 MHz) up to 10 pC that can be used for detector characterization or for diagnostics but not is not active in normal operation.

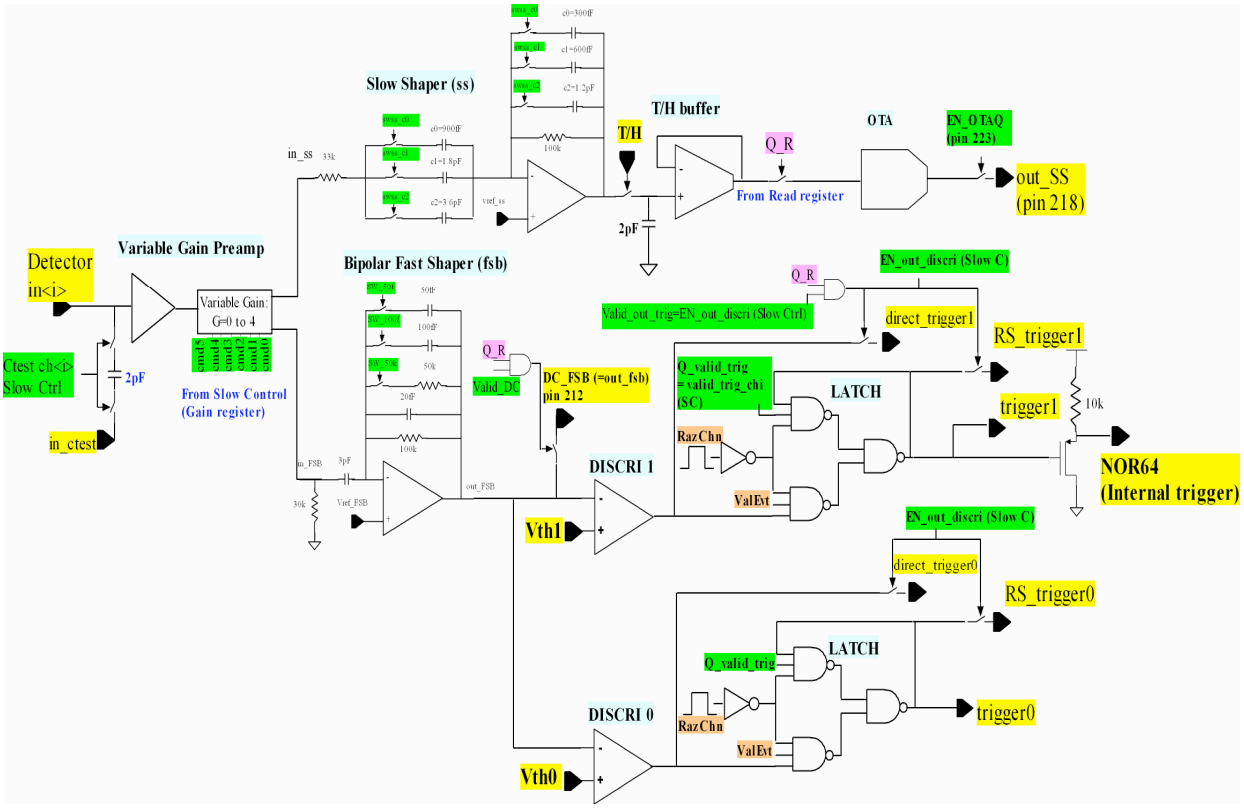


Figure 117: schematic diagram of the analog part of one channel of HARDROC1

In parallel, trigger outputs are obtained via fast channels made of a fast (15 ns) shaper followed by 2 low offset discriminators. The discriminator thresholds are set by two internal 10 bit DACs. Each trigger output is latched to hold the state of the response until the end of the clock cycle. The trigger1 outputs are OR-wired to generate an internal trigger used to start the memorization of the 128 trigger outputs as well as the Bunch Crossing Identification delivered by a 24 bit *Gray* counter, needed to associate hits in the DAQ to bunch crossing identification (BCID). It is also possible to capture event data using an external trigger provided from outside the chip.

The chip is power pulsed to decrease the power consumption down to10 µW/channel as targeted with a 1% beam duty cycle.

∞

[68] The variable gain current conveyor is well suited for fast, possibly in-homogenous detectors. The MIP levels are comparable aournd 1 pC and the threshold required are also similar at 50-100 fC. The low input impedance of the architecture is well suited at minimizing the crosstalk in a detector where multiplicity is a concern.

3.1.2. Testbench measurements

HaRDROC1 has been extensively measured from December 2006 to December 2007. In particular, it was the first time that the power pulsing could be tested as well as the readout scheme of the calorimeter with built-in memory, token ring and daisy chain mechanism.

The analogue part, largely reused from MAROC, worked as foreseen. . The bipolar fast shaper gain is around 3.5 mV/fC and its peaking time is equal to 15 ns. The Slow Shaper gain is around 50 mV/pC and its peaking time can be tuned from 100 ns to 150 ns. The crosstalk has been measured by sending 100 fC in one channel and looking to the direct neighbours, it amounts to 2% with a well differentiated shape and located at the input.

The linearity of the two 10 bits integrated DACs used to generate the thresholds of the discriminators, has been measured (Figure 118) and the residuals of both DACs are within ± 5 mV for a 2.6 V dynamic range which corresponds to an Integral Non Linearity of 0.2% (2 LSB). The slope is 2.5 mV per DAC unit.

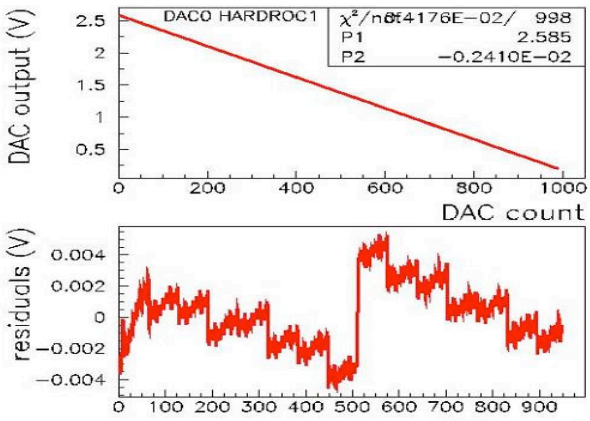


Figure 118 : 10-bit DAC linearity

The trigger sensitivity (s-curves) has been measured on the 64 channels of the chip. The quite large non uniformity between channels (±25 %) is explained by current mirror mismatch (small transistor size to optimize speed at low current) and can be corrected using the gain tuning of the input preamp as shown in Figure 119. The s-curves also show a total noise around 1fC.

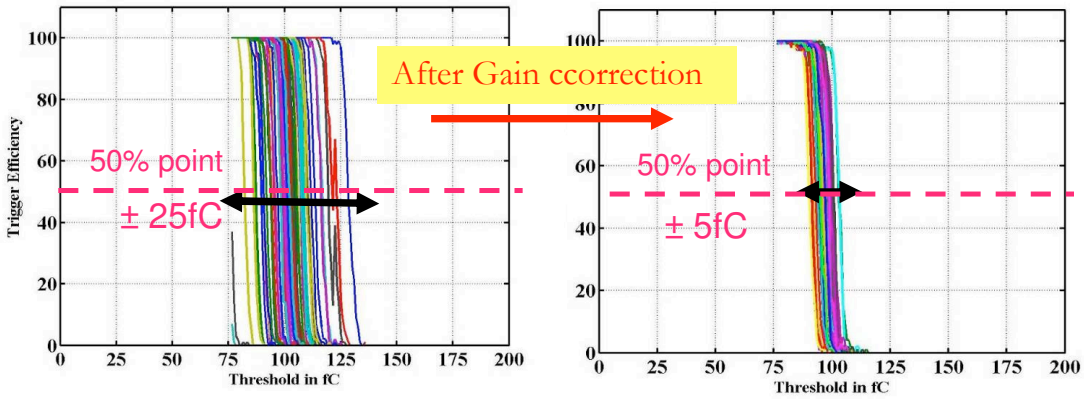


Figure 119: s-curves of the 64 channels of HARDROC1 before and after gain correction

As can be seen in Figure 120, the dispersion between channels is small enough to bring the threshold down to 10 fC. In particular, the pedestal is uniform within 1 DAC count (2.5 mV or 1 fC in high gain) which shows the excellent offset control obtained with this SiGe bipolar technology.

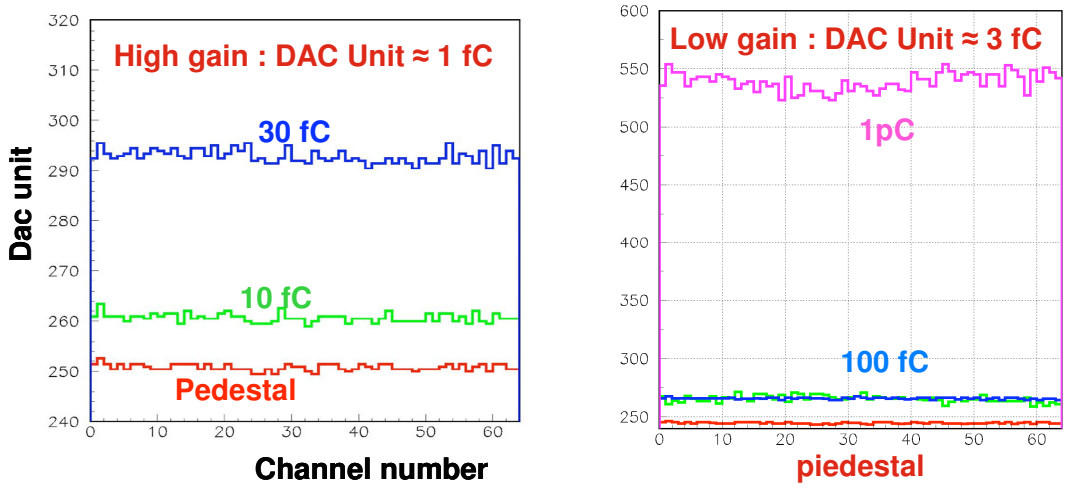


Figure 120: : threshold for 50% trigger efficiency for the 64 channels of HARDROC1

Last, but not least, the power pulsing capability has been tested on HARDROC1. There are three independent signals of power-on : Analog, Digital and DAC. Each stage can be forced "on" by slow control, overruling the power-on pulse. As can be seen in Figure 121, it takes only 2 µs for the analog part to be "awake" and provide a discriminator output ("trigger") when an input charge of 100 fC is sent 2 µs after the power-on signal. As could be expected[69], the DAC is much slower to settle (this is the reason why it had a separate power-on signal) and in it needs 25 µs to reach its nominal value within a few mV.

These fast turn-on times make it possible to operate the chip with a duty cycle of 1 ms/200 ms = 0.5% and hence bring the power dissipation from 0.5 mW down to 10 µW/channel.

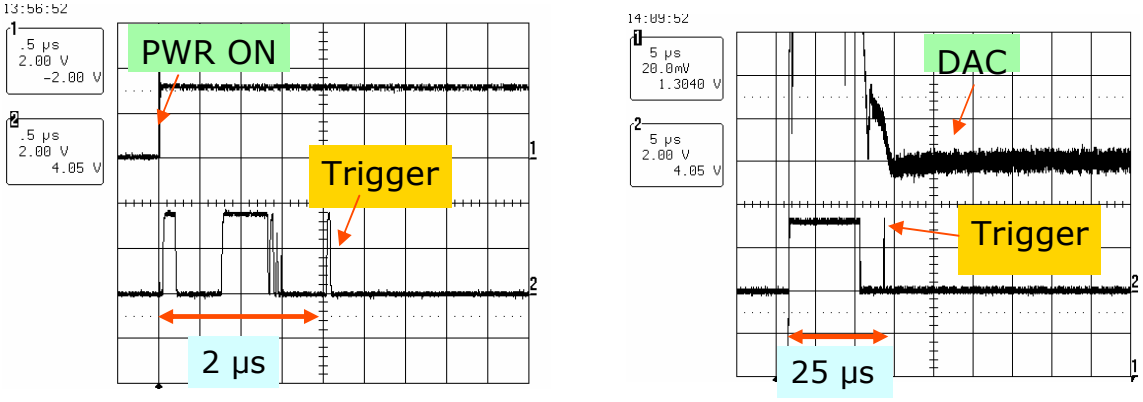


Figure 121: power-on of the analog part (left) and of the DAC (right)

[69] The DAC outputs are filtered internally by a large 200 pF capacitor that reduces the noise and minimizes inter-channel coupling when several channels trigger.

3.1.3. HaRDROC digital part:

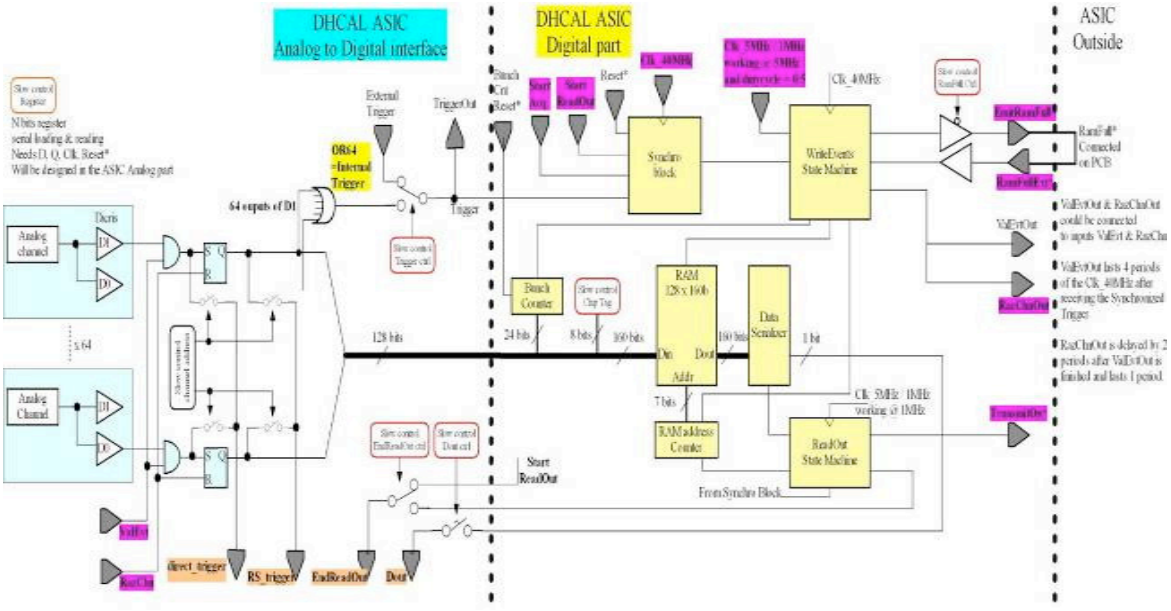


Figure 122: digital part of HARDROC1

Because of the very high number of electronic channels foreseen in the final detector, chips will be embedded inside the detector and are designed to be daisy chained without any external circuitry, to limit to a bare minimum the number of output lines on the detector. A SRAM memory[70] has been integrated in HARDROC to store during the bunch train the 2-bit trigger outputs of each channel as well as the BCID, and this for every hit with a depth of 128.

The output data format is thus : 128(depth)*[2 bits * 64 ch + 24 bits (BCID) +8 bits (header)] =20 kbits. There is one serial output which is transferred to the DAQ during the interbunch.

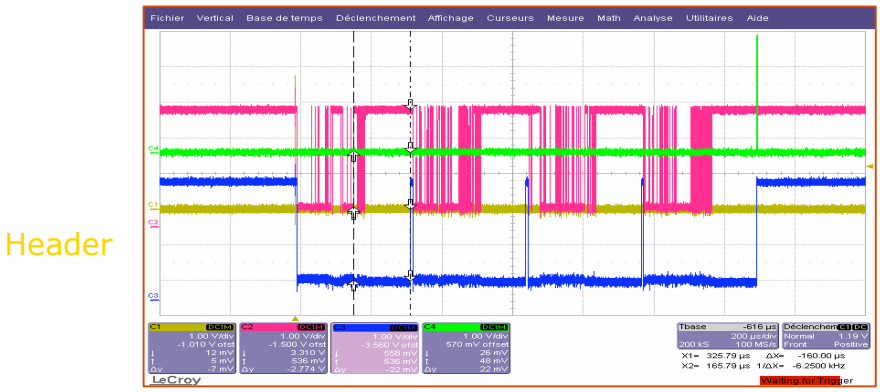


Figure 123: Four chips read-out sequentially, with the scheme described in §3.1.3. Each chip provides 128 events with 2 bits of data per event together with the BCID and chip header.

∞

[70] It uses an IP block from AMS which is a 32x128 bit dual port memory. 5 such blocks are necessary to cover the 64 channels, with 2 trigger bits/channel and BCID counter on 24 birs.

A PCB hosting four HARDROC1 chips (4X64 channels) has been designed by IPNL/LLR to study the signal connection between the different chips before extracting it through a USB device (Figure 124. The PCB board has been associated to both RPC and μMEGAS detectors in order to validate the whole concept through exposure first to cosmics and then to beam test at CERN.

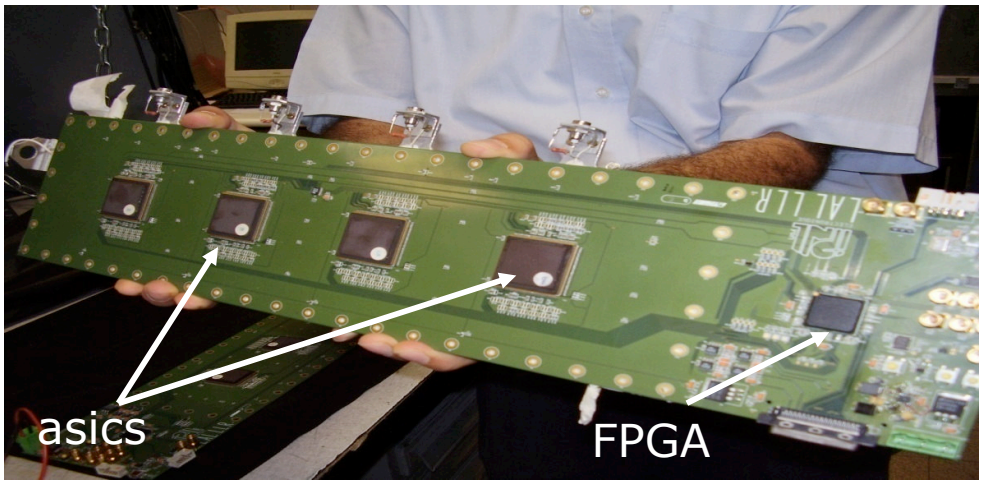


Figure 124: RPC detector of 8x 32 cm2, readout by 4 HARDROC1 chips [IPNL, LLR, LAL-OMEGA]

3.1.4. Testbeam results

The RPC detector shown in has been used in test-beam in 2008 and 2009. It was the first time that the readout could be tested in real conditions and good data have been achieved allowing detector characterization.

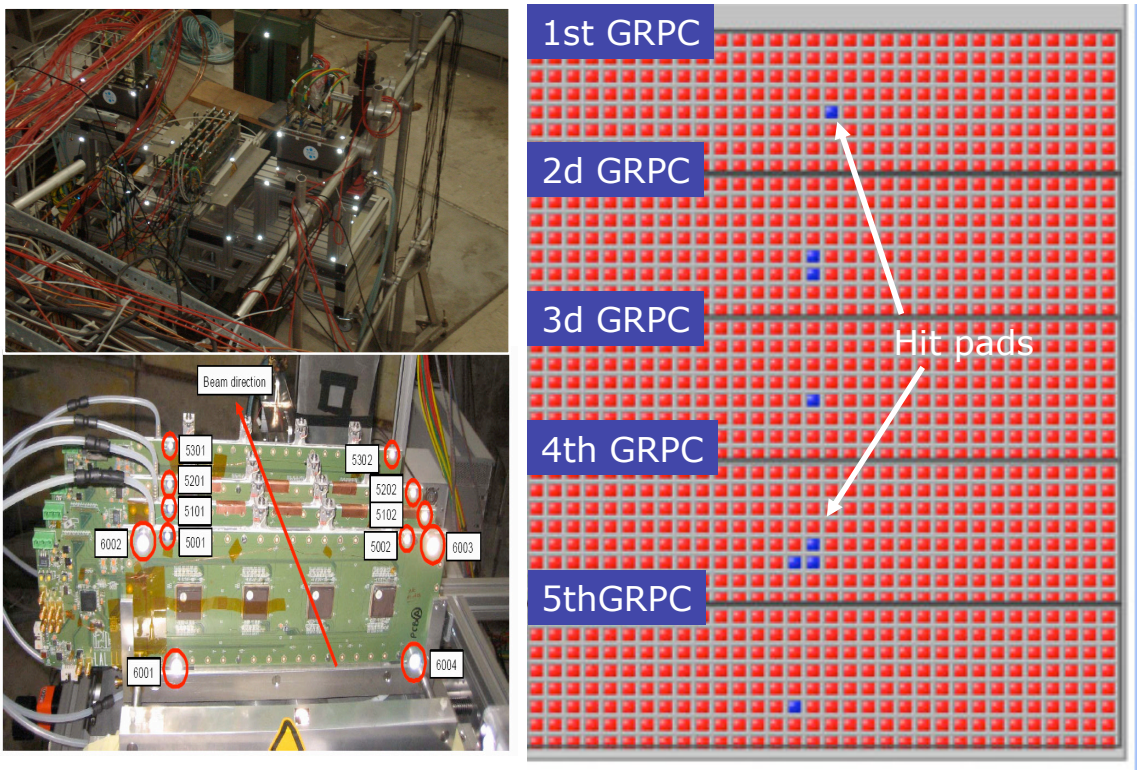


Figure 125 Left : testbeam arrangement at CERN, consisting of 5 RPC planes of 32x8 cm2 radout by HARDROC1. Right : view of a muon track in the 5 RPC planes.

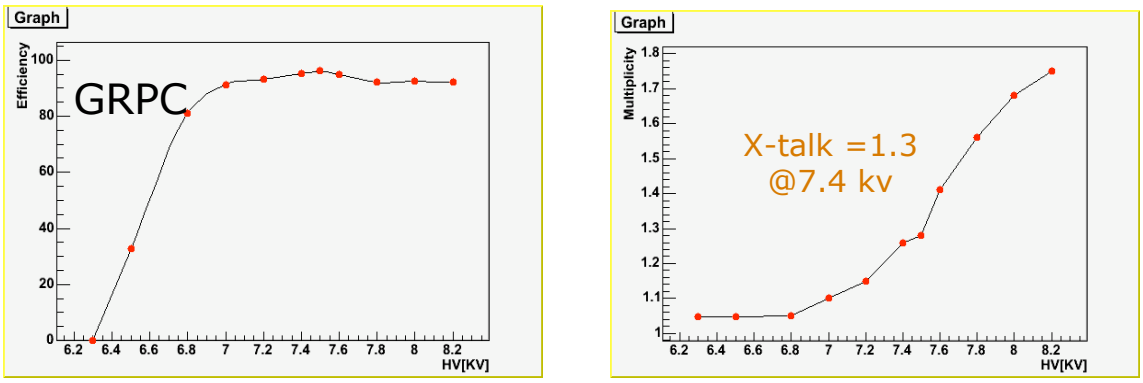


Figure 126 Left : effiiciency as a function of high voltage. The chamber uses Lycon resistive paint (20 M) and TFE 93%, Isobutane 5%, SF 2% gas mixture. Right : Multiplicity as a function of High voltage. With this chamber an efficiency >95% with a multiplicity of 1.3 is obtained at HV=7.4 kV.

3.2. HaRDROC2 version

As shown in the previous section, HARDROC1 has exhibited good performance both on test-bench and on test-beam. A second version was notwithstanding fabricated in order to :

∞ Change the package from PQFP240 to TQFP160 and achieve the 1.4 mm thickness. This required to change the pad ring on the chip to match it to the new package and to have it on a single row.

∞ Extend the dynamic range to three thresholds in a ratio of 1-10-100 for better physics performance of the semi-digital

∞ Correct a bug in the power pulsing, where the bandgap remained "on" all the time and add a "clock power-on" module to switch off internally the clock during the readout phase[71], when the chip is not sending data on the line.

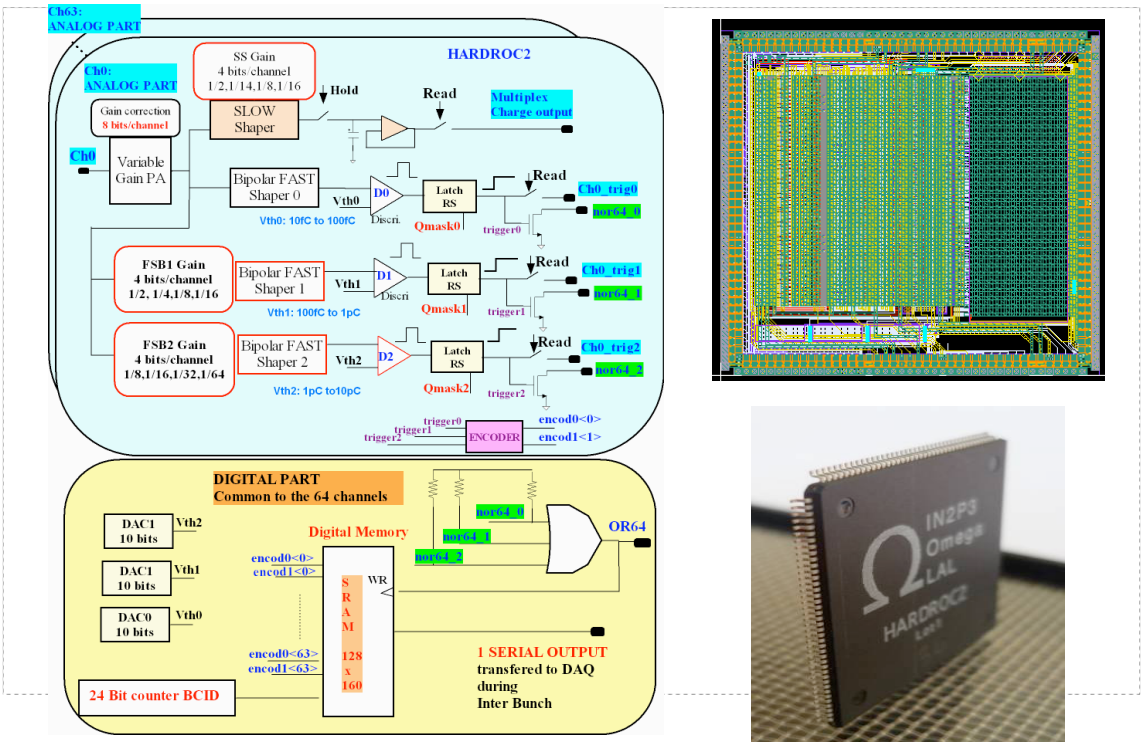


Figure 127: synoptic view of HARDROC2, layout and packaged chip in TQFP160 plastic package

The experimental results obtained with HaRDROC2 are similar to those of HaRDROC1. A better uniformity has been obtained by improving the layout of the current mirrors in the preamplifier and adding 2 bits to perform the gain adjustment on 8 bits instead of 6. The linearity of the adjustment is displayed in Figure 128, showing residuals of ±2% over the 8 bits. This finer adjustment allows to equalize the gains to 1.5% as shown in Figure 129, which displays the gain dispersion[72] before and after adjustment, for HaRDROC1 and HARDROC2. In HaRDROC1, the gain dispersion started from 9% *rms* and could be tuned down to 5%, whereas in HaRDROC2, the dispersion starts from 6% and goes down to 1.5%.

∞

[71] The LVDS clock receivers cannot be operated continuously as they draw 200 µW

[72] The gain is measured in DAC units as 50% trigger efficiency for 100 fC injected charge.

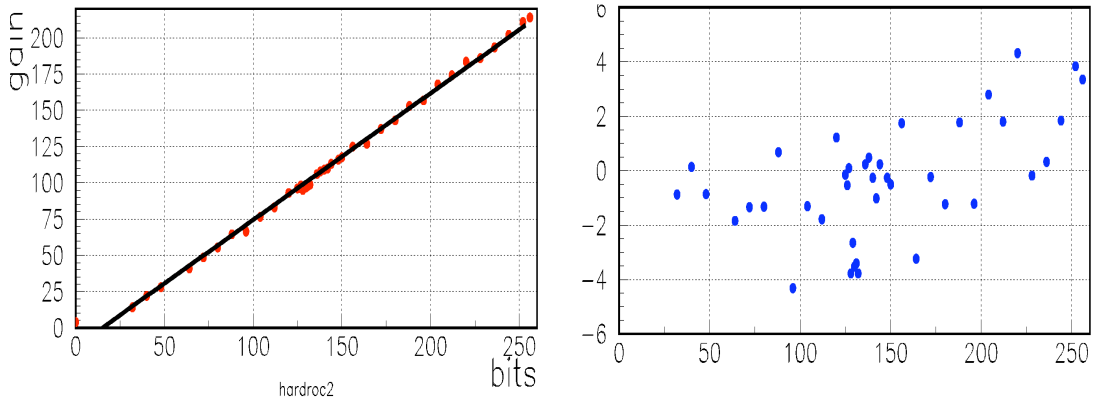


Figure 128 Left : preamp gain adjustment as a function of bit setting. Right : residuals of the linear fit, giving ± 2% non linearity

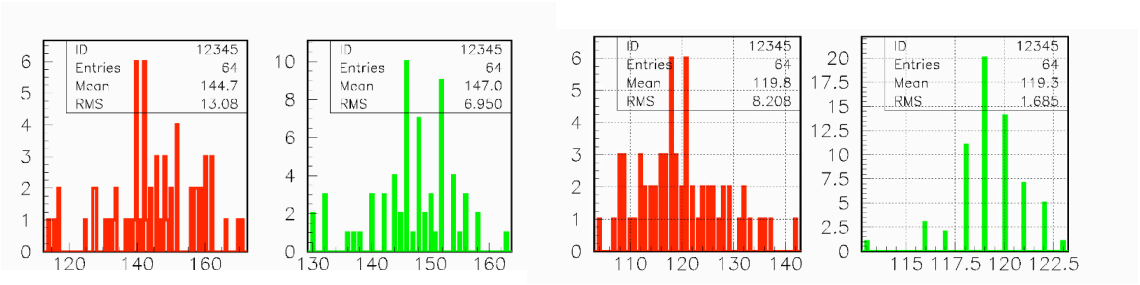


Figure 129 Left: gain dispersion on HaRDROC1 before(red) and after (green) preamp gain adjustment. The dispersion are respectively 9% and 5%. Right : Same plot for HaRDROC2, for which the dispersions are 6% and 1.5%. The better figures are due to a better layout of the current mirrors and 2 additional bits for gain tuning.

The other modifications behaved as foreseen[73] and the power pulsing can now be exercised meaningfully. The power dissipations of the various stages are shown in Figure 130, giving a power dissipation per channel of 29 mA * 3.3 V / 64 channels = 1.6 mW/channel un-pulsed. As for HaRDROC1, the turn-on time is 2 µs for the analog part and 20 µs for the DAC which allows a 0.5% duty cycle, bringing the power down to 8 µW/channel, well below the target of 10 µW. It goes further down to 5 µW/ch in the purely digital option (1 threshold instead of 3)

stage	current "on"	current "off"
Preamp	5.4 mA	0
Fast Shaper	12.3 mA	0
Discris	7.3 mA	1 µA
DAC	2.0 mA	0
digital	1.1 mA	3 µA
TOTAL (64ch)	29 mA	4 µA

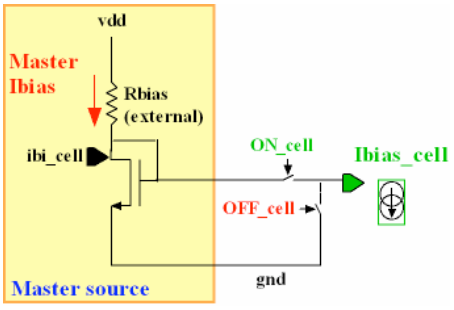


Figure 130 Left : Table of power consumptions for the various stages of HaRDROC2. Right: scheme for powering off bias cells

∞

[73] Except for the slow control register, for which some configurations could not be loaded on certain chips. This has been traced to the clock distribution line inside the chip, which is very long, dispersive and heavily loaded, producing too slow a rising edge.

The power pulsing operation necessitates to remove the decoupling capacitors on the various reference voltages and bias points, which can make the chip more sensitive to various couplings or external noise. In particular, the minimum threshold that can be achieved can be jeopardized by discriminator output coupling to the inputs. This effect has been measured (Figure 131) and amounts to 3 fC, which is smaller than 5σ noise (4 fC). Thus, the minimum threshold[74] obtained with HarDROC has been measured as 5 fC, very close to the theoretical minimum of 5σ noise, which has been obtained with very careful layout and substrate decoupling. This also allows to be insensitive to internal digital noise, despite a large digital core running at 40 MHz on the chip

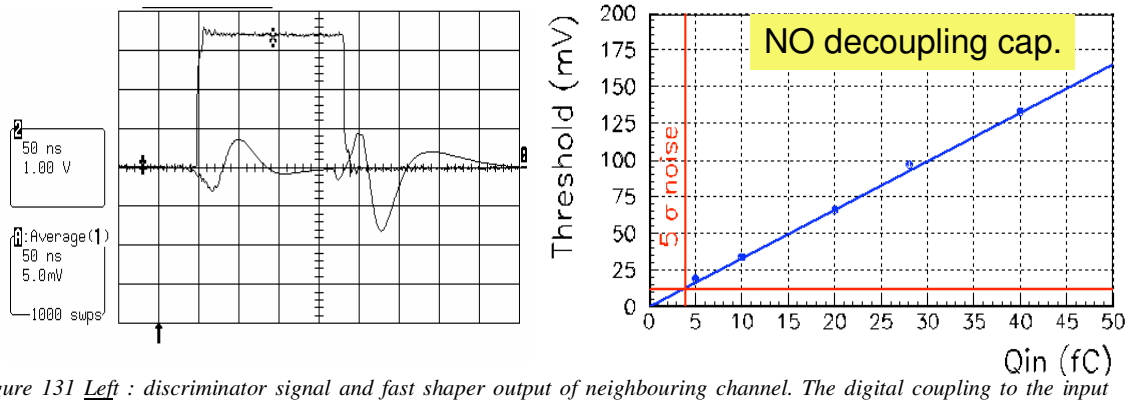


Figure 131 Left : discriminator signal and fast shaper output of neighbouring channel. The digital coupling to the input amounts to 3 fC. Right : Threshold as a function of injected charge, showing a minimum threshold of 4 fC consistent with 5σ.

3.3. Square and cubic meter prototypes

The good results obtained with the 8x32 cm² detector and HaRDROC1 pushed for moving towards the square meter, scalable, prototype in order to address all the large dimensions issues, as much for the detector as for the readout electronics. This was first realized at IPNL with 6 boards of 32x48 cm².

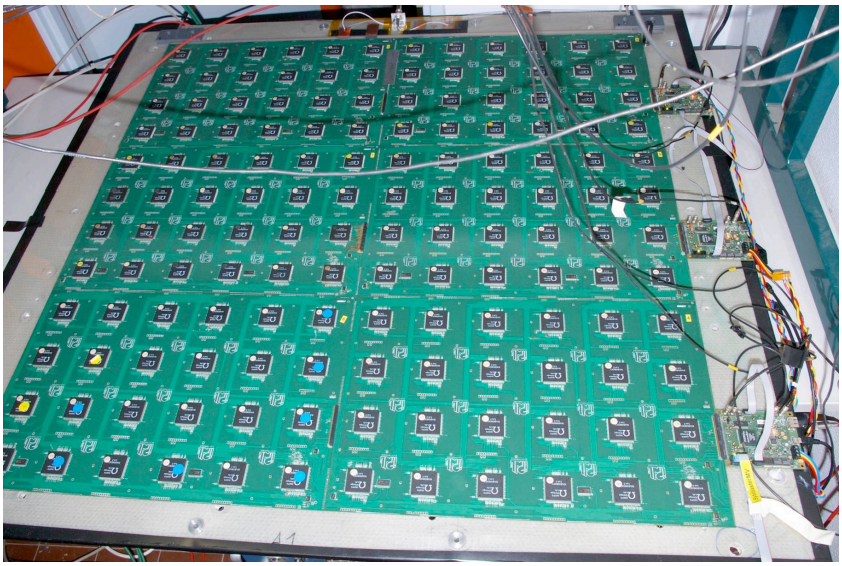
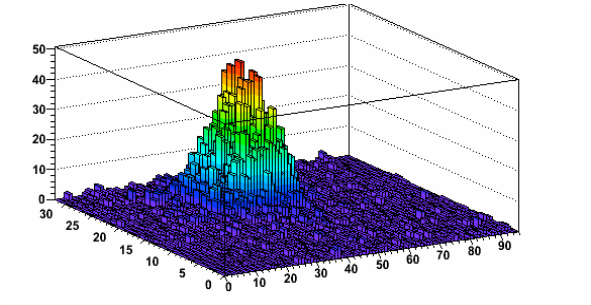


Figure 132 : square meter prototype of RPC detector with 1 cm² granularity, designed by IPNL group. The detector is read-out by 96 HaRDROC1 chips

∞

[74] On one given channel. For the whole chip, the minimum is ~10 fC due to the ~5 fC threshold dispersion between channels



This board has been tested in testbeam in june and august 2009 and allowed to exercise the full readout. It was the first time the full scale readout could be exercised and has been a very valuable exercise for the whole calorimeter system.

A similar board has been realized by the LAPP (Annecy) group led by *Y. Kariotakis* and *C. Adloff*, for µmegas chambers. It is read-out by the HaRDROC2 chip and has benefited from the synergies of RPC detectors on the readout scheme which has allowed to have it operational very quickly.

Figure 133 : µmegas detector of 32x96 cm^2 designed by LAPP and readout by 96 HaRDROC2.

Once the tests of square meter prototypes are completed, a large quantity (5 000) of HaRDROC will be produced in a dedicated run to equip 40 layers of detectors and validate the concept of scalable, power pulsed, digital hadronic calorimeter, as defined in the ANR project.

4. Analog Hadronic Calorimeter (AHCAL)

The analog hadron calorimeter has been proposed very early in CALICE in order to have a conservative, yet powerful tool to measure the jets. It is based on scintillating plastic tiles of 3x3 cm² readout by a Silicon Photomulitplier[75] (SiPM) because of the large (5 T) ambient magnetic field. This detector has been designed by the DESY group, under the leadership of *F. Sefkow*.

As for the ECAL, two paths have been followed :

- A physics prototype of 1 m³, using conservative techniques (even though the SiPM was a brand new photodetector, never used before in a physics experiment !) in order to take testbeam data as early as 2004. This detector was readout by an ASIC (FLC_SiPM) developed by Orsay.
- A technological prototype, funded by EUDET to study the technological issues when going to large dimensions.

4.1. AHCAL physics prototype

4.1.1. Overview of the detector layout

The detector is composed of 40 layers of 1 square meter 2 cm thick steel plates interleaved with sensitive "cassettes" of 296 scintillating tiles readout by SiPMs (Figure 134).

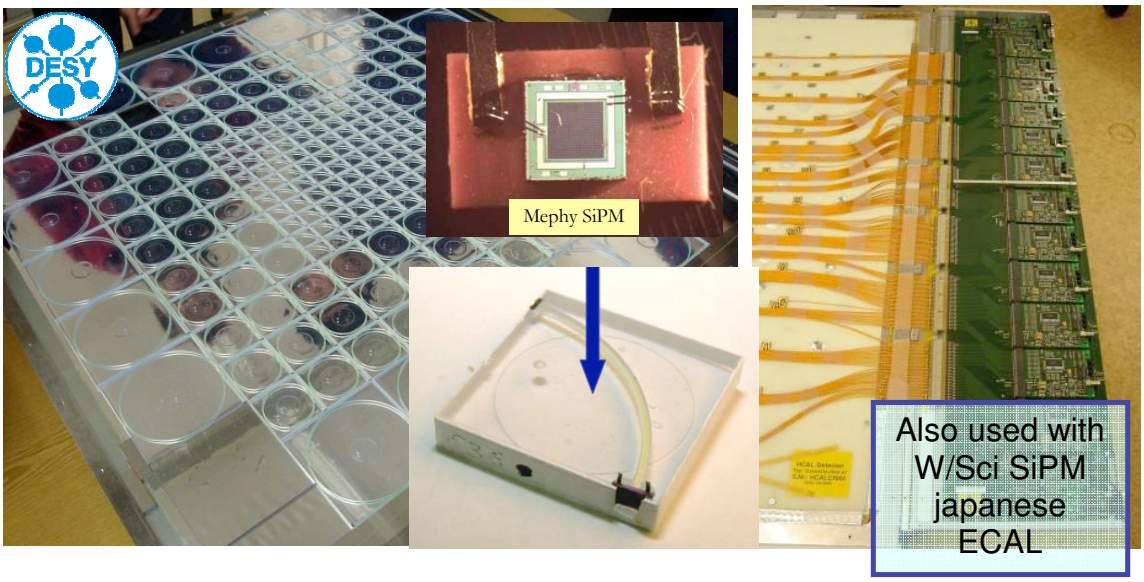


Figure 134: view of one layer of the AHCAL with scintillating tiles, detail of SiPM implementation and electronics readout. [design by DESY]

4.1.2. FLC_SiPM : readout ASIC [22]

The readout ASIC was designed by Orsay as it was re-using several parts of the ECAL chip FLC_PHY3 and was connected to the same DAQ boards. The sensor was extremely interesting as it was brand new and promised to a bright future. Its high gain (~10^6) relaxed a lot the noise constraints in the

[75] A SiPM is a solid state photon detector, pioneered by Russian groups, in which individual photons discharge small pixels (typically 20-50 μm) operated in Geiger mode. It provides single photon detection up to a few thousands of photons in 1 mm²

design, although the large dynamic range of 20 000 was not giving that much space[76]. We re-used the low noise preamp from FLC_PHY3 and mounted in voltage amplification as the 50 Ω termination for the cable was providing a low impedance source. The shaper was taken again from FLC_PHY3, although it was made variable to have a fast setting (50 ns) that provides large gain for small calibration signals and a slow setting (150 ns) that gives a lower gain to accommodate the maximum signal but also was slow enough to allow the hold signal coming from the beam chambers to arrive around the signal peak. This latter was difficult to obtain with the fast pulses of the detector + preamp and it was necessary to add a 10 kΩ series resistor in the input to further spread the signal and slow it down, at the expense of a non negligible noise contribution.

The chip schematic diagram is shown in Figure 135.

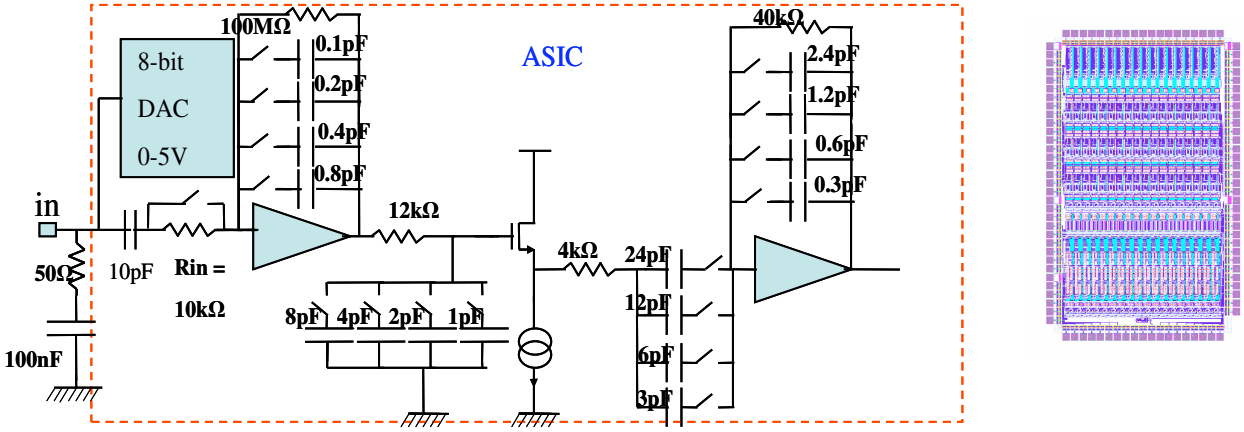


Figure 135: schematic diagram of FLC_SiPM and chip layout realized in AMS 0.8µm BiCMOS

The chip was started in april 2004 and submitted in june 2004. It was tested in the fall 2004 and as there was only one bug found it was decides to launch directly the production in November 2004. The series of 1000 chips fully tested was made available to the collaboration in april 2005, which constitutes our record of turn-over time for a new chip : one year from project start to full production delivery !

4.1.3. FLC_SiPM performance

The chip behaved as anticipated, except for the DAC which added noise in the prototype version : the noise was increasing with the DAC setting, almost doubling for large DAC values. This was traced to insufficient filtering of the DAC transimpedance OTA, which was exhibiting some ringing around 1MHz. It has been solved in the production version by increasing the dominant pole in the OTA.

The waveforms in the chip are shown in Figure 136. The physics mode allows to experience the full dynamic range of 2000 photoelectrons (p.e.) with a MIP response around 20 mV and a single photoelectron around 1.5 mV. The peaking time of 160 ns was the longest obtainable with reasonably large capacitors in the CRRC^2 *Sallen-Key* shaper, it turned out to be just sufficient to accept the latency of the external hold signal. The noise in this mode is 1 mV *rms*, giving a dynamic range of 11 bits. In the calibration mode, a faster shaping can be used as the hold signal can be generated in advance by the light pulsing system. This immediately increases the signal amplitude, by roughly the shaping time used and we

∞

[76] The maximum signal is given by the number of pixels of the SiPM (here 2000) and the noise needs be typically ten times smaller than the single photo-electron signal in order to distinguish properly the photons peaks

get 12 mV for 1 photoelectron (160 fC) with a noise of 1.2 mV *rms*, giving a photoelectron to noise ratio of 10.

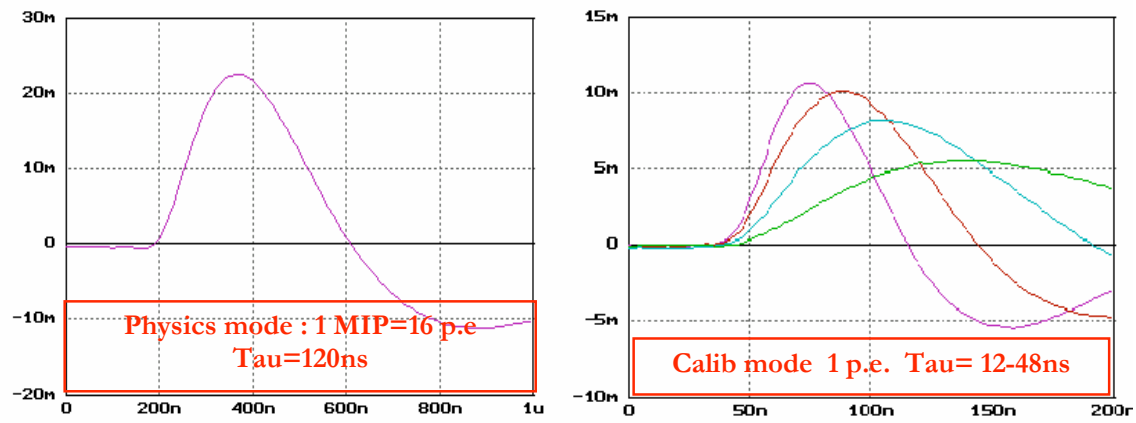


Figure 136: MIP and single photoelectron response in physics and calibration modes (50 ns and 150 ns shaping time)

The input DAC covered the range 0-5 V and behaved as expected, allowing to tune the operating point of the detector channel by channel. Figure 137 shows the DAC linearity, measured to be within ±2%, with a rather large notch at the MSB transition, which was fortunately in the good direction to prevent having a gap in the SiPM bias setting.

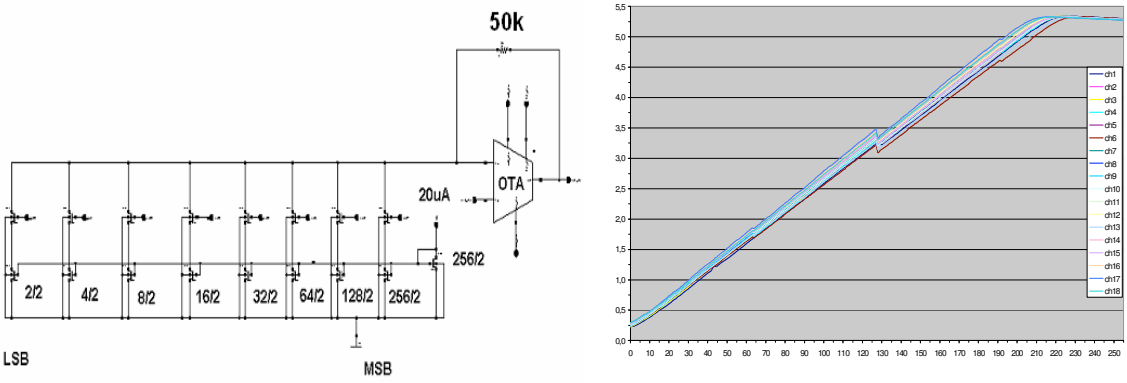


Figure 137: Left : input 8bit 5V DAC schematic. Right : linearity of the 18 channels, exhibiting residuals within ±2%

The chip is mounted on a front-end board named "HBU[77]" designed by DESY as shown in Figure 138. The connection scheme also shown in Figure 138 was made such that only one coaxial cable is used to connect to the SiPM and bring the high voltage together with the signal.

∞

[77] Hadronic Board Unit

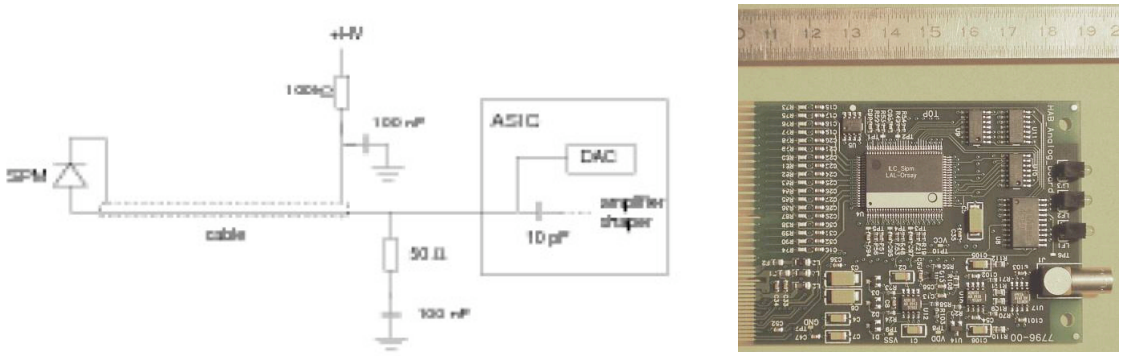


Figure 138: front-end board and detector connection to the ASIC and photograph of the HBU board designed by DESY to read 18 channels

More than 8 000 channels of SiPM have now been routinely operated since 2006 in test beam at DESY, CERN and FNAL. The overall performance is good as displayed in Figure 139 with the plot of the calibration spectrum showing the single photoelectron peaks, which exhibits a signal photo-electron to noise ratio of 4.3. With a MIP signal of 14 p.e. in average, the cut at ½ MIP is easy to achieve and allows good imaging as displayed by the typical pion event of Figure 139.

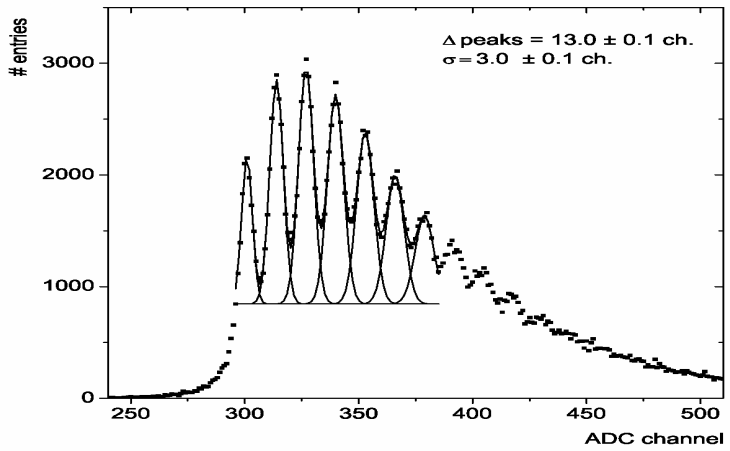


Figure 139: photoelectron spectrum from calibration LED pulser

4.2. AHCAL technological prototype and SPIROC

As for the ECAL and DHCAL, the AHCAL must also prove that it is scalable to large modules. There, the main issues are the integration of the electronics inside the detector with its power dissipation and readout issues (similar to the ECAL and DHCAL) and mechanical assembly of the system. Also the thickness is a very important issue, although not as critical as in the ECAL.

Once again, the ASIC is a central, critical issue of the whole detector usual coined as "no chip, no detector[78] !". For this purpose, a fully integrated ASIC named SPIROC (for Silicon Photomultiplier Integrated Read Out Chip) has been developed by the Orsay group.

∞

[78] Dixit *F. Sefkow*

4.2.1. Detector overview

The EUDET module for the AHCAL, designed by the DESY group, is depicted in Figure 140. As in the ECAL, it consists of motherboards called HBU[79] that services 12x12 tiles for an area of 36x36 cm². The HBUs can be connected between each other to bring all the signals to the edge of the module.

The cross section of one HBU is shown in Figure 140. Sandwiched between the two absorber plates that insure the mechanical rigidity, the sensing elements are made of scintillating 3x3 cm² tiles, attached to a SiPM. The SiPM are soldered to a PCB that covers the whole area and provides signal routing to the SPIROC ASICs. 4 ASICS or 36 channels service one HBU. As for the ECAL, these chips are daisy chained and connected to the edge of the board to connect to the neighbouring boards. At the end, the signals are handled by a DIF board.

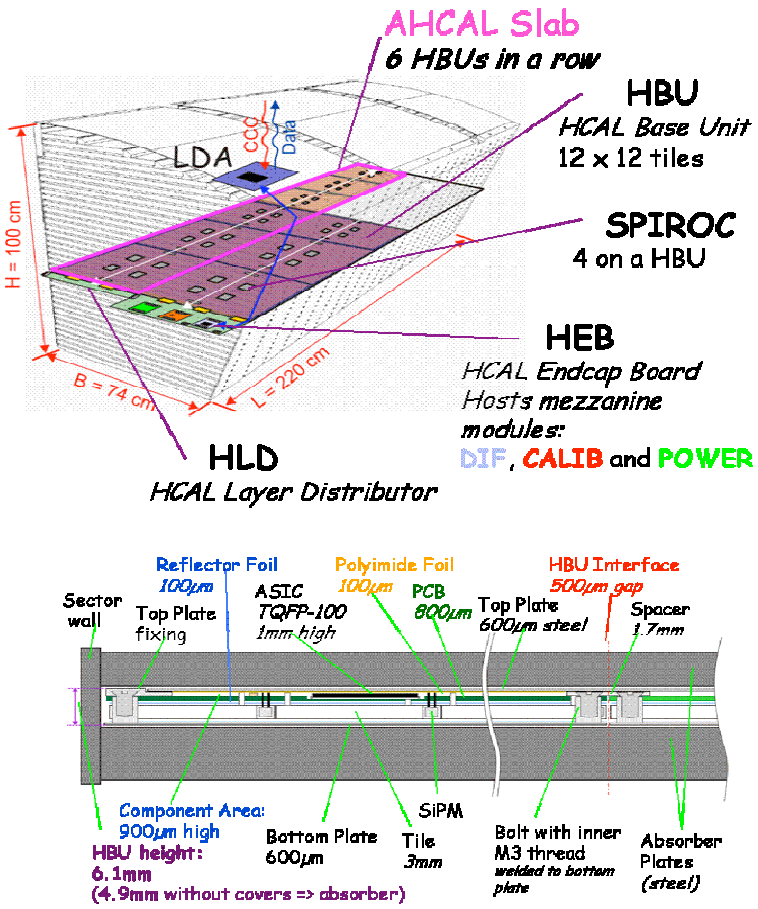


Figure 140 : schematic view of the EUDET AHCAL module (DESY design)

4.2.2. SPIROC ASIC architecture

The SPIROC ASIC that reads 36 SiPMs is an evolution of the FLC_SiPM used in the physics prototype. As for the ECAL, it keeps most of the analog part, adds an analog memory to record up to 16 events of a train and adds the auto-triggering capability. The digitization is brought inside the chip as well as the data handling.

The first prototype has been fabricated in june 2007 in AMS SiGe 0.35µm. The chip layout is shown in Figure 141, its area is 35 mm² for 36 channels and it is packaged in a CQFP240 package

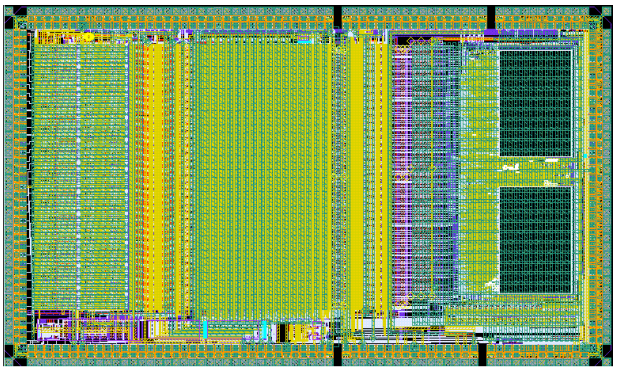


Figure 141: layout of SPIROC1

[79] HCAL Base Unit

It is the most complex chip realized by the group so far as shown in the synoptics of Figure 143. The schematic diagram of one channel is shown in Figure 142.

The 8-bit input DAC has been conserved, however its power dissipation has been brought down by 3 orders of magnitude to 1 µW/channel as it is not power pulsed[80]. The DAC also has the particularity of being powered with 5 V whereas the rest of the chip is powered with 3.5 V.

The voltage amplifier architecture with variable gain has also been kept, with a gain variable on 4 bits. However, the high gain/low gain separation splitting is now done at the preamp level by having two preamps on parallel on the input.

The charge is measured on both gains by a "slow" shaper (50-150 ns) followed by an analog memory with a depth of 16 capacitors.

The auto-trigger is taken on the high gain path with a high-gain fast shaper followed by a low offset discriminator. All these blocks are new. The discriminator output is used to generate the hold on the 36 channels. The threshold is common to the 36 channels, given by a 10-bit DAC similar to the one from HARDROC with a subsequent 4-bit fine tuning per channel.

The discriminator output is also used to store the value of a 300 ns ramp in a dedicated analog memory to provide time information[81] with an accuracy of 1 ns

A 12-bit Wilkinson ADC is used to digitize the data at the end of the acquisition period.

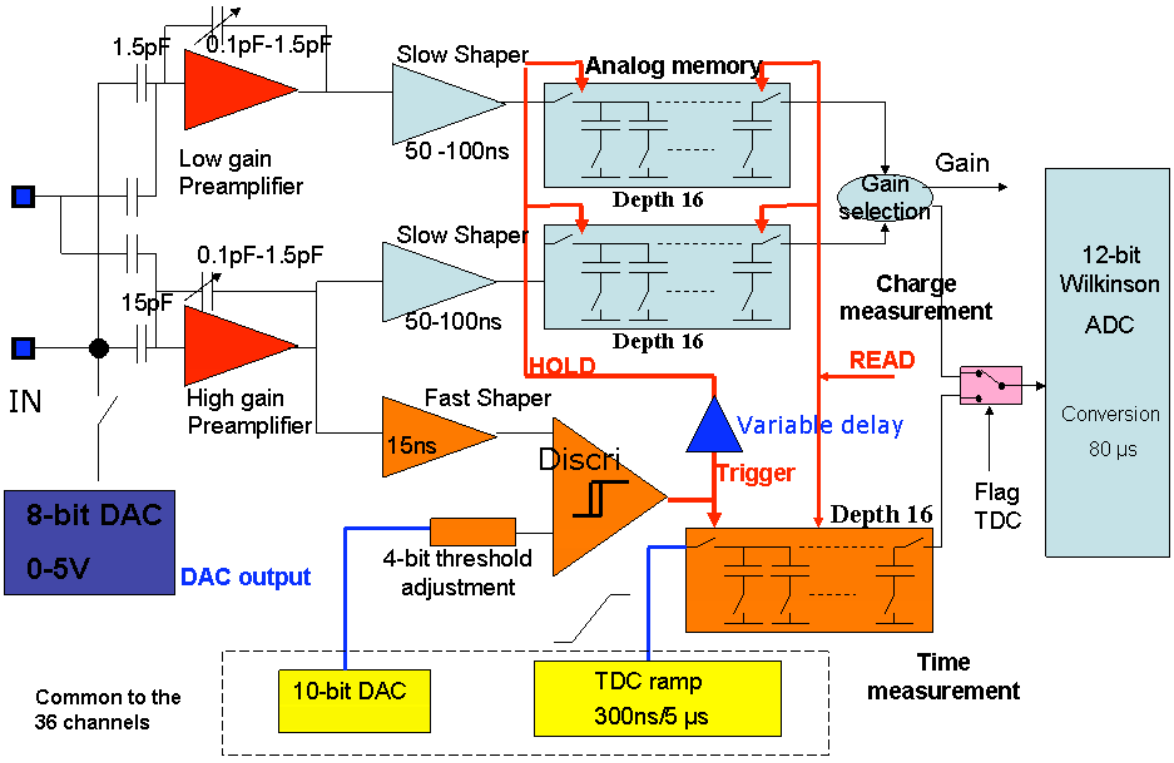


Figure 142: schematic diagram of one channel of SPIROC1

The digital part is very complex is it must handle the SCA write and read pointers, the ADC conversion, the data storage in a RAM and the readout process. It has been written in VHDL, synthetized

∞

[80] In order to keep the operating point of the SiPM as stable as possible

[81] This feature which was not requested at design phase will be used to tag delayed neutrons in the hadronic showers.

and routed, using the memory blocks IPs from AMS, as for HaRDROC. The DAQ part is identical to the one from HaRDROC, exploiting optimally the synergies between these chips.

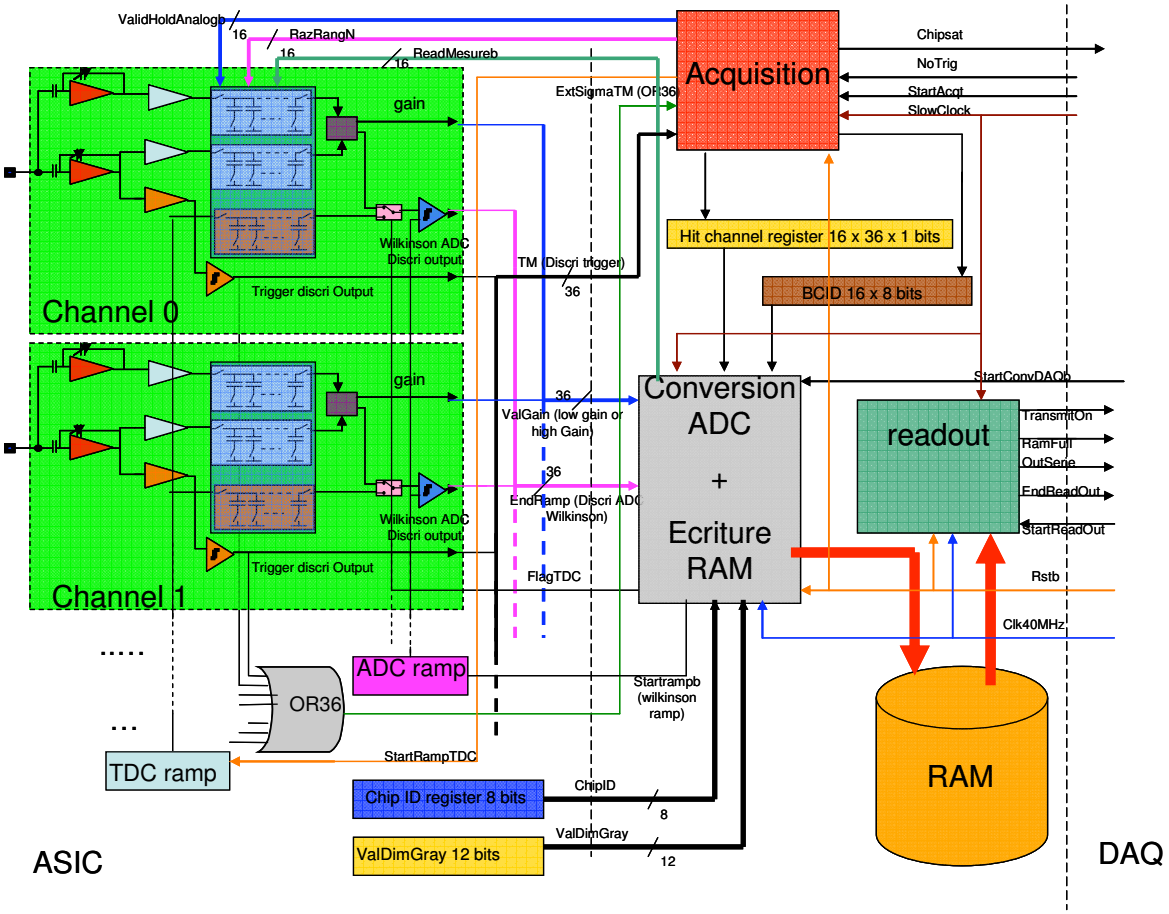


Figure 143: synoptic of the digital part of SPIROC1

4.2.3. Measured performance

The chip has been received in October 2007 and underwent a long series of tests both in Orsay and Hamburg. The analog performance has shown good results but an inverted polarity in the ADC discriminators has unfortunately precluded any measurements with the internal ADC.

∞ Input DAC : the span goes from 4.5 V down to 0.5 V with a LSB of 20 mV. The default value is 4.5 V in order to operate the SiPM at minimum over-voltage when the DAC is not loaded. The linearity is ±2% (5LSB), just enough for the SiPM operation but consistent with the allocated area[82]. Also, the dispersion between channels, although not fundamental could also be improved. The power dissipation is well within the specifications and the 100 nA bias current to Vdd makes the chip difficult to measure without special precautions[83].

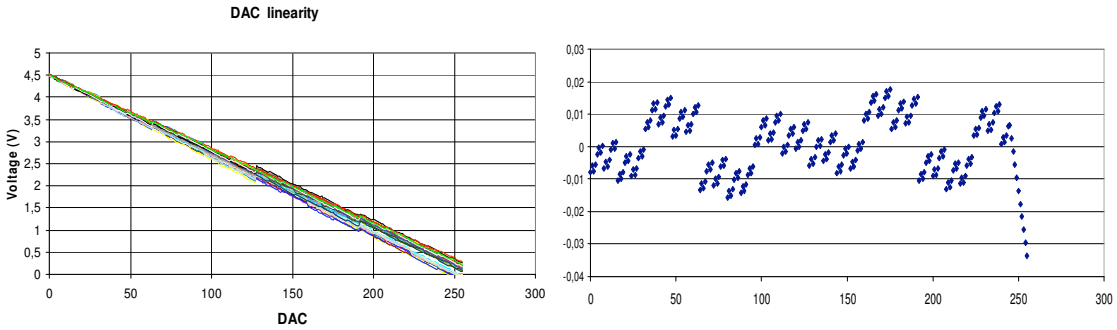


Figure 144 : input DAC linearity over the 36 channels

∞ Threshold and gain selection 10-bit DACs behave similarly to the HARDROC, with a 2 mV step and 0.1% linearity.

∞ Charge path.: the internal waveforms can be output thanks to a "probe register" that allows to connect various internal points to the output. Although not perfect[84], this system is convenient to characterize the chip

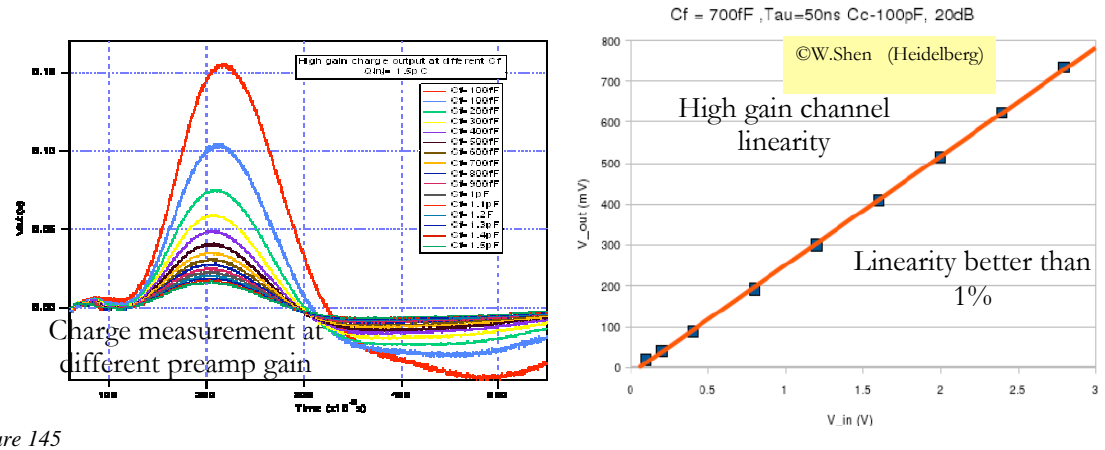


Figure 145

∞

[82] The transistors are PMOS ranging from 1/2 to 256/2. The anticipated offset from a 256/2 is Voff= 20mV/√512 = 1 mV which produces a current mismatch of dI/I=gmVoff/I=qVoff/kT=1 mV/26 mV=4% in good agreement with measurements. Clearly the operation at very low current and thus in weak inversion is very penalizing in terms of mismatch and the performance is governed by the transistor size, which is difficult to further increase as the input DAC already represents 10% of the chip area.

[83] The usual 10 MΩ input impedance of table voltmeters draws 500 nA from the 5V output, exceeding the bias-current of 100 nA of the DAC output amplifier. It can however sink the leakage current of the SiPM up to 2 µA as this now adds to the bias current.

[84] The probe register is a very long "snake" shift register (800 flip-flops) that is touchy to load correctly.

∞ Auto-trigger and discriminators. The ability to self-trigger on single photoelectrons or on the MIP is a new feature of SPIROC. This has been tested as displayed in Figure 146, showing as for HaRDROC the good dispersion between channels. The Auto-trigger on 50 fC is established and the minimum threshold is also given by 5σ noise, showing the low digital couplings inside the chip.

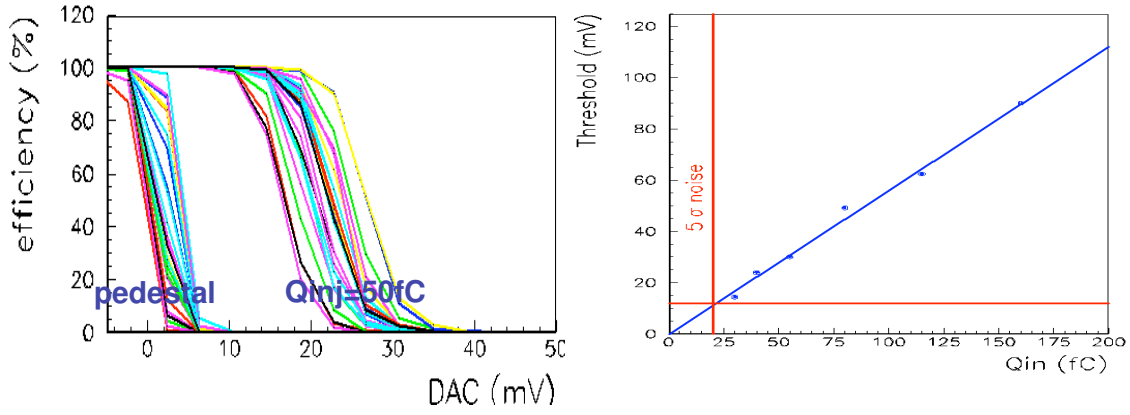


Figure 146. Left : Trigger efficiency as a function of DAC setting for 0 and 50 fC charge input, corresponding to 1/3 phototelectron. Right : 50% Trigger as a function of injected charge, showing a minimum threshold of 25 fC.

4.2.4. SPIROC2 version

As was explained earlier, it was necessary to fix the bug in the internal ADC in order to complete the measurements. This has been done in a second prototype SPIROC2 submitted in june 2008. In this version, the number of pins has also been reduced in order to fit in a smaller, thinner package TQFP208. The digital part has also been aligned to the improved version of HARDROC2, in particular concerning the power pulsing and the robustness of the DAQ.

The ADC exhibits good 12 bits performance, as shown in Figure 147 and Figure 148, with a non linearity of ± 1 LSB and a noise between 0.5 and 1 LSB. The uniformity between the 36 channels is particularly good, as shown in Figure 148, with a dispersion of 0.1%.

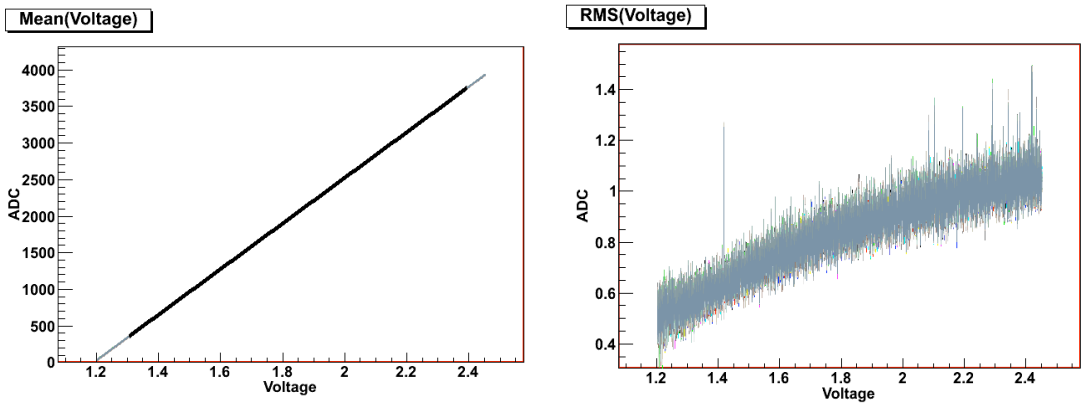


Figure 147. Left : response of the 36 ADC channels with superimposed linear fit. The residuals and dispersion are shown in the next Figure. Right : noise as a function of the input voltage for the 36 channels.

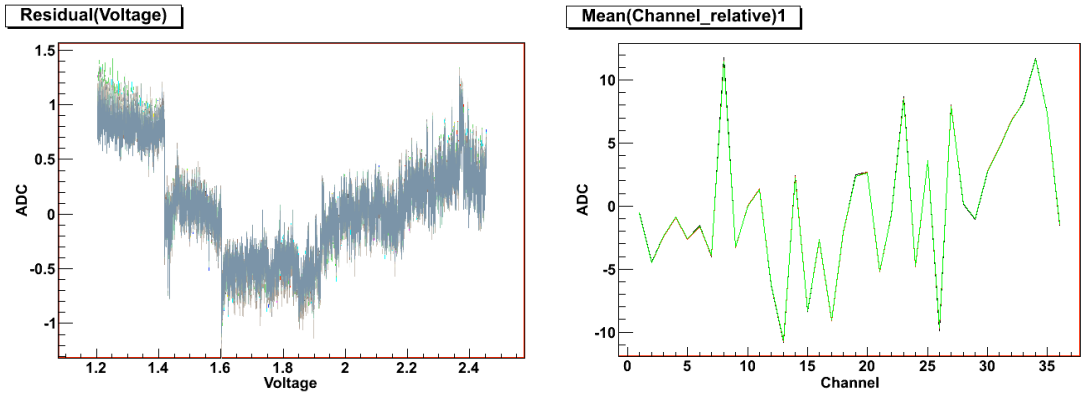


Figure 148. Left : Residuals to the linear fit of the 36 channels in ADC counts. The integral non-linearity (INL) is 1 LSB, making it a real 12 bit ADC. Right : dispersion at mid scale between the 36 channels. The uniformity is at per-mil level.

SPIROC is still the only chip that reads SiPM and its performance together with the excellent record of FLC_SiPM on 8 000 channels makes it in high demand.

5. Conclusion on ILC chips

The family of ROC chips represents a key milestone to validate the highly integrated read-out electronics necessary for the ILC particle-flow calorimeters. The chips are very complex, and although the bench tests show good performance, a long campaign of measurements is still necessary to validate them on detector. Once completed, they will be produced in a dedicated engineering run[85] to equip a real scale module of each type of calorimeter (EUDET ECAL, AHCAL and ANR DHCAL).

∞

[85] An engineering run produces between 10 and 20 8-inch wafers. Each wafer exhibits 64 replications of the elementary reticle of 20x20 mm², on which it is possible to include several different ASICs. As an example, the ILC engineering run should include SKIROC2, 6 HaRDROC3, 2 SPIROC3, 1 SPIROC0 and 1 MAROC3

CHAPTER 5

MULTIANODE PHOTOMULTIPLIER READOUT

1. Introduction

The appearance of multi-anode photomultipliers (MAPMT) by Hamamatsu at the very end of the century greatly changed the use of large area scintillators with wavelength shifting fibers. They could be read out by a compact detector, provided the readout electronics be also compactified. One drawback of these multi-anode devices was the large pixel to pixel gain variation, up to a factor of 3 which can be compensated for in the preamplifier by an innovative variable gain preamp. All experiments then requested 100% detection efficiency on the single photoelectron (typically 160 fC at canonical gain of 10^6).

The first request was brought by the OPERA experiment [23] for which *J.P. Repellin* took interest into and its target tracker dedicated at finding the emulsion bricks where the neutrino interaction would have taken place and doing some basic calorimetry. The target tracker was fabricated by the group of Strasbourg, we were in charge in Orsay of the front-end electronics and Lyon was in charge of the DAQ. For this purpose, we designed a dedicated chip OPERA_ROC that would provide a multiplexed charge output on 32 channels and a discriminator per channel that would produce a trigger for the DAQ.

The second request came from the ATLAS luminometer [25] in 2003. In order to measure the absolute luminosity, roman pots with scintillating fibers would be located at 200 m from the interaction point and come very close to the beam to measure diffracted protons at very small angle. To obtain a position resolution of the order of 50 μm ten layers are necessary leading to a around 1300 fibers that are readout by 20 MAPMTs. By that time, the 0.8 μm technology that was used for OPERA_ROC was now obsolete and the chip was then redesigned in 0.35 SiGe BiCMOS, scaled up to 64 channels and several external features were included to form the new MAROC chip.

The principle of highly integrated readout chips for multi-anode photomultipliers has also been scaled to arrays of photomultipliers in view of the next generation of large neutrino experiments (Megatonne). There, in order to obtain huge areas of photodetection, instead of producing ever larger photomultipliers it has been shown advantageous by Photonis to use arrays of smaller, cheaper photomulitipliers read out by a common multichannel chip. This has led to an ANR project granted in 2006 and led by *J.E. Campagne* called PMm^2 (for square meter photomultipliers).

2. OPERA target tracker and OPERA_ROC ASIC (NIM paper [24])

The OPERA experiment [23] is located in Gran Sasso tunnel and aims at measuring the appearance of tau neutrinos in neutrino oscillations from a muon neutrino beam coming from CERN.

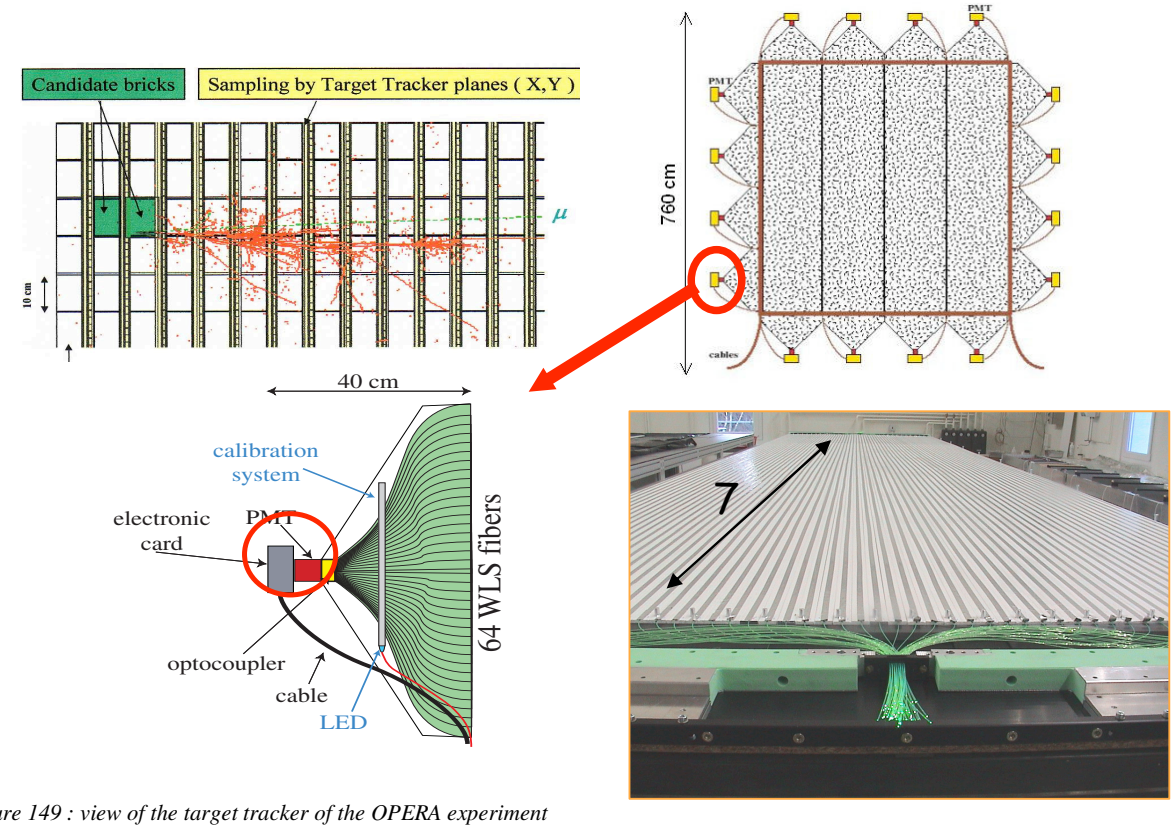


Figure 149 : view of the target tracker of the OPERA experiment

2.1. Overview and requirements

The readout electronics of each Target Tracker is based on a 32-channel ASIC, referred to in the following as the OPERA_ROC (OPERA Read Out Chip). Two such devices are used to readout each PMT for a total of 1,984 chips for the full detector.
The main requirements driving the chip design are the following :

- the chip needs a large bandwidth necessary for a good matching with a fast PMT signal shape.
- the chip must correct the signal for anode-to-anode gain variations up to a factor of 3.
- the ASIC must deliver a global auto-trigger as time information, with a 100% trigger efficiency for particles at minimum of ionization (MIP)
- finally, the chip must deliver a charge proportional to the energy deposited in the scintillator for a charge ranging between 1 and 100 photoelectrons (0.1 - 16 pC)

PMT pixel-to-pixel gain variation have been measured to exhibit variations by a factor as large as 3 inside the same PMT. In order to compensate this large difference between channels, the front-end electronics must be equipped with an adjustable gain system, directly incorporated in the preamplifier stage. This allows good integration density and delivers a signal of identical range to the fast and slow shaper of every channel.

The auto-trigger stage has been designed to be a low noise, 100% efficient in the detection of particles at minimum of ionisation (MIP). Typically, particles traversing the scintillator at the center of the strips,

deposit around 6 photo-electrons, which varies with the distance from the impact to the PMT. This distance is ranging from a few cm to 7.6 m with a fiber attenuation length typically above 700 cm. These characteristics impose strong requirements on the trigger capabilities, and a 100% trigger efficiency is required as low as a 1/3rd of photoelectron, which corresponds to about 50 fC at the anode for a PMT gain of 10^6 . Finally, a dynamic range of the charge measurement up to about 100 photo-electrons is required, which corresponds to 16 pC at a gain of 10^6 . This should allow to distinguish MIP from particle showers and provide a measurement of the energy deposition in EM showers relevant for the event classification. The charge measurement must of course be effective for any individual (preamplifier) gain corrections.

The LAL shared the responsibility with Bern University to provide the front end electronics for the 992 PMT's (that is 1,984 chips) used to readout signals from the scintillator Target Tracker of OPERA. While LAL designs the ASIC's used to readout signal from the scintillator Target Tracker, Bern university designs the mother Boards that implements the FE chip.

2.2. Main features of the ASIC

The Read-Out chip is a 32-channel ASIC with individual input, trigger and charge measurement. The ASIC is designed to correct for gain variation among channels via a variable gain preamplifier and returns an auto-trigger multiplexed output to the ADC, as well as a hit register reporting all channels passing trigger requirements.

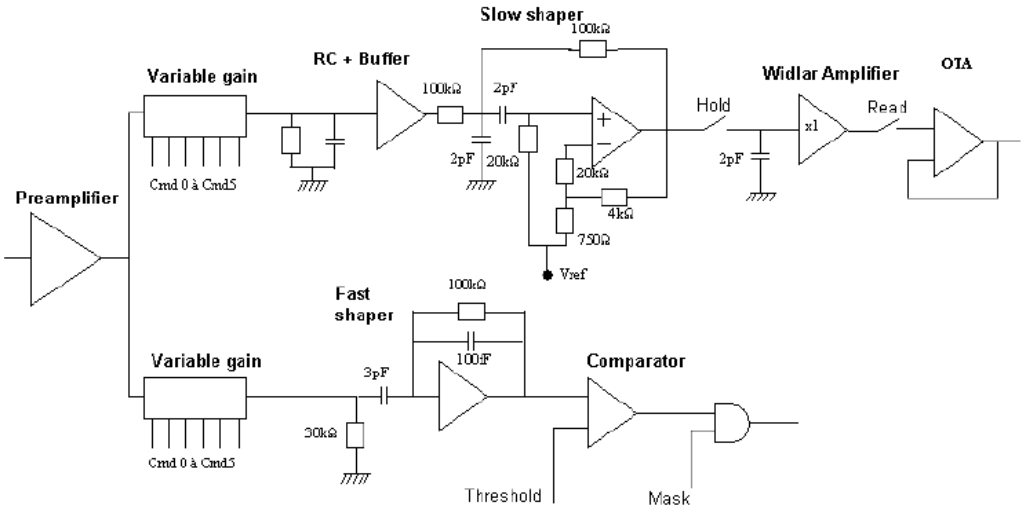


Figure 150 : schematic diagram of one channel of OPERA_ROC

The single channel architecture is presented in Figure 150 as a block functionality diagram. The ASIC comprises a low noise, low impedance variable gain preamplifier that feeds both a trigger and a charge measurement arms. The gain correction functionality makes use of a current mirror structure that is set via a series of switches to amplify the input signal up to a factor 3. The trigger channel includes a fast shaper followed by a comparator, whose reference threshold is set at once externally for all channels. A trigger decision is formed by the logical ``OR'' of all 32 comparator outputs and sets in the Sample and Hold in the charge measurement arm. A mask register allows at this stage to disable externally any noisy or malfunctioning channel. The charge measurement arm consists of a slow shaper followed by a Track & Hold buffer. Upon a trigger decision, charges are stored in 2 pF capacitors and the 32 channels outputs are readout sequentially at a 5 MHz frequency, in a period of time of 6.4 μs.

2.3. Details of ASIC design

As usual, the preamplifier is one of the most critical elements in the design. It is based on a current conveyor using the "super common base" architecture (*cf* Figure 151). This provides a low input impedance, good to minimize the crosstalk, always critical in such a granular detector and a very fast response, insensitive to the input capacitance. The current output can then feed a binary scaled current mirror that is used as a DAC to tune the gain on 6 bits (cf. Figure 164).

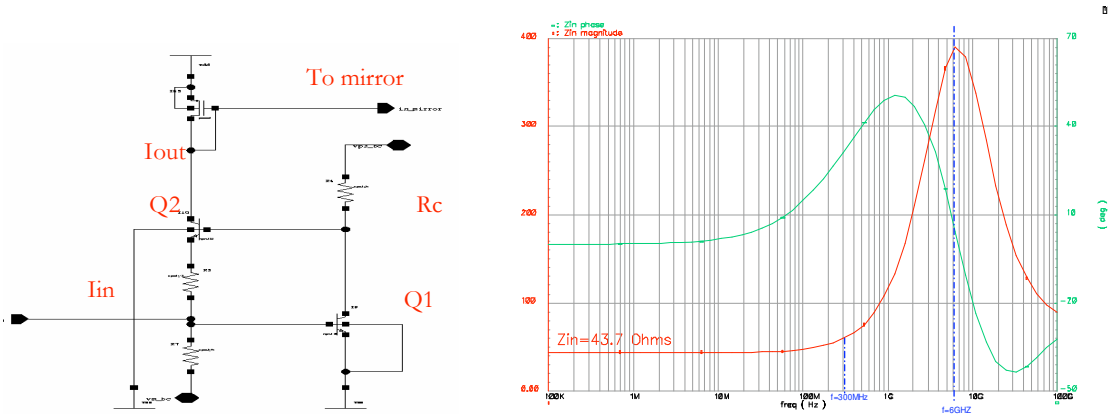


Figure 151. Left : schematic diagram of the input preamplifier. Right : simulated input impedance as a function of frequency

In the super common base configuration Q2 acts as the current conveyor and Q1 R_C as a simple amplifier that amplifies the base voltage of Q2 in order to keep its emitter voltage dynamically to zero. The input impedance R_{in} of such configuration is given by :

$$R_{in} = \frac{1/g_{m2}}{1+g_{m1}R_C} = \frac{V_T^2}{I_{C1}I_{C2}R_C}$$

in which g_{m1}, g_{m2} are the transconductances of transistors Q1 and Q2 biased at a collector current I_{C1} (typically 100 µA) and I_{C2} (typically 20 µA). V_T is the thermal voltage (26 mV at 300K) and R_C is the load resistance in the collector of Q1 (typically 30 kΩ). With such values, the input impedance can be tuned by varying the bias currents. In practice, $g_{m1}R_C$ is set between 40 and 100 and Q2 is biased at a few tens of µA in order to keep the parallel noise to a reasonable value. One difficulty of this configuration is its instability with capacitive sources as the input impedance appears inductive when the capacitance across Rc is taken into account[86]. On that ground, the benefit of bipolar technology is obvious as one can obtain a good transconductance for Q1 while having a very small capacitance, bringing the 'equivalent input inductance down to a few 10 nH, similar to the bonding wire. It can be seen (*cf* Figure 152) that with this configuration, the signal amplitude varies little with the detector capacitance or gain setting.

∞

[86] The gain around Q1 becomes $g_mRC/(1+sR_eC_p)$ which gives a term in sRC in Rin, modelized as an inductance, similar to the calculation of current sensitive preamplifiers made in Chapter 1.

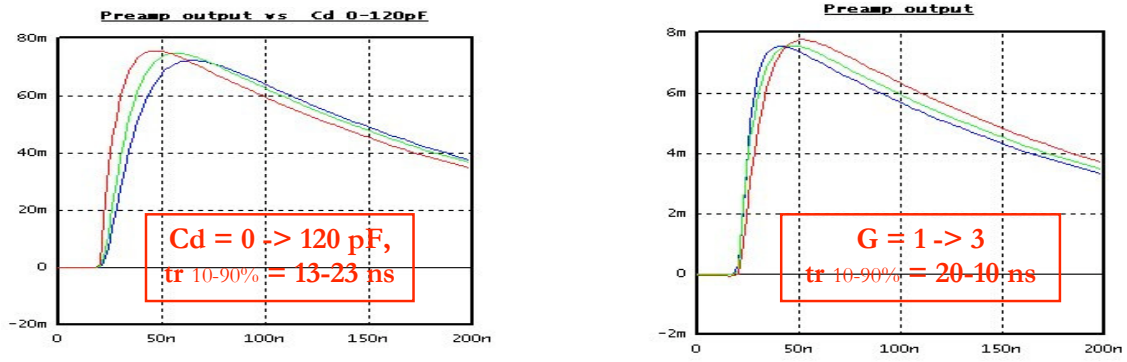


Figure 152 : preamp output signal for various detector capacitances (left) and gain setting (right)

The noise performance is dominated by transistor Q1 for the series noise which dominates at very high frequencies. Here again, as shown in Figure 153, the bipolar technology is providing very good performance with a series noise down to 2.5 nV/√Hz. The parallel noise is less impressive as in all current conveyors with a value of 4 pA/√Hz.

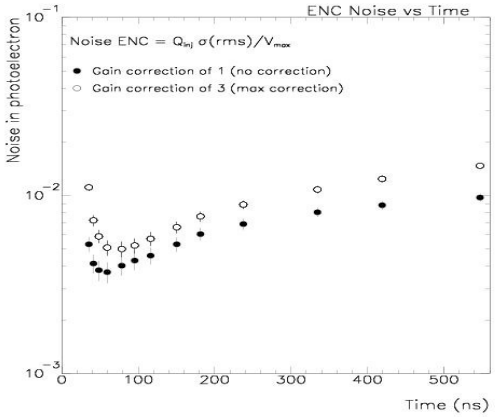


Figure 153 : ENC vs shaping time

2.4. Practical realization and performance

The technology of the chip is AMS BiCMOS 0.8 µm. The chip area is about 10 mm² and it is packaged in a QFP100 case. The chip consumption is around 5 mW/ch giving an overall dissipation of 250 mW for a 5 V power supply.

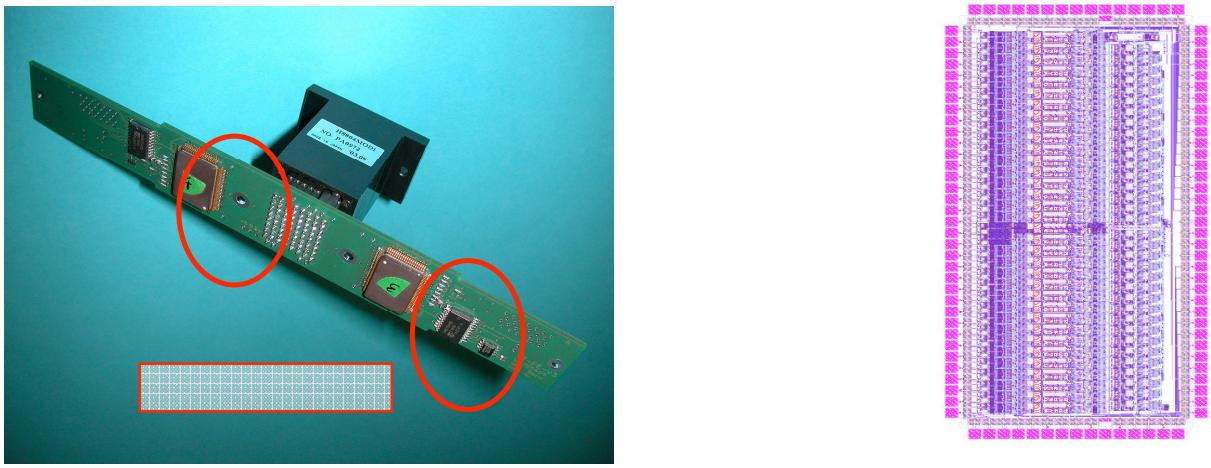


Figure 154. Left : Frond-end board (Bern design) housing one PMT and 2 OPERA_ROC ASICs . Right : chip layout

Two chips are used to readout the PMT on the front-end board designed by the Bern group which also houses the ADC that digitizes the signal in charge. The DAC that sets the threshold is also external and on located on the DAQ board. Typical output waveforms are displayed in Figure 155, showing the good linearity of the gain adjustment setup. The trigger efficiency can be set well below 0.1 photoelectron (=160 fC) allowing to auto-trigger easily on a third of photoelectron, as requested (Figure 156). The auto-trigger is used to generate the hold and the 32 channels are multiplexed with a pedestal dispersion of 2 mV *rms*, small enough not to be corrected for. Finally, the overall charge spectrum obtained with the ASIC is shown in Figure 158, in which the single photoelectron peak is clearly distinguished from the pedestal.

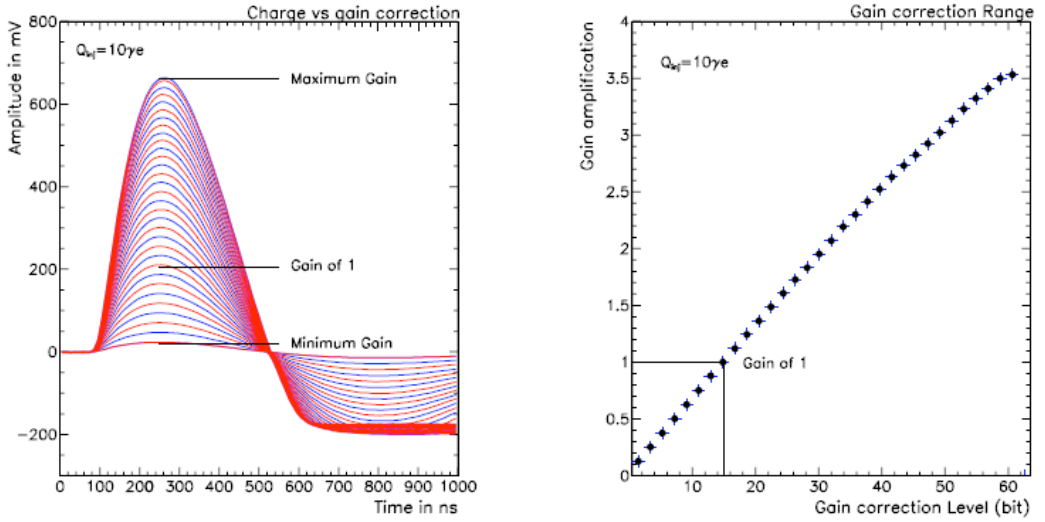


Figure 155. *Left* *: slow shaper output waveform for various preamplifiers gains.* *Right* *: linearity of the gain correction*

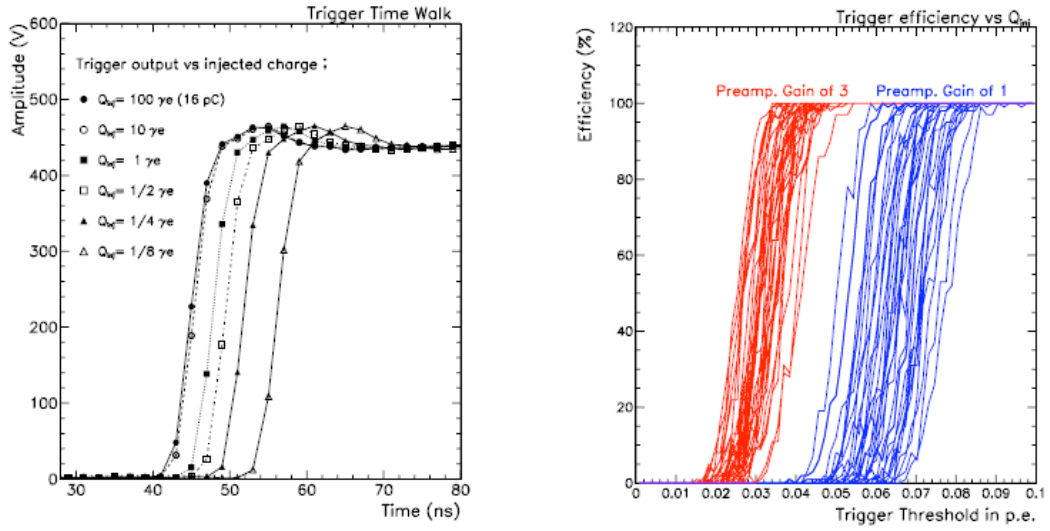


Figure 156. *Left* *: time walk from 0.1 to 100 photoelectrons.* *Right* *: "s-curves" of the 32 channels*

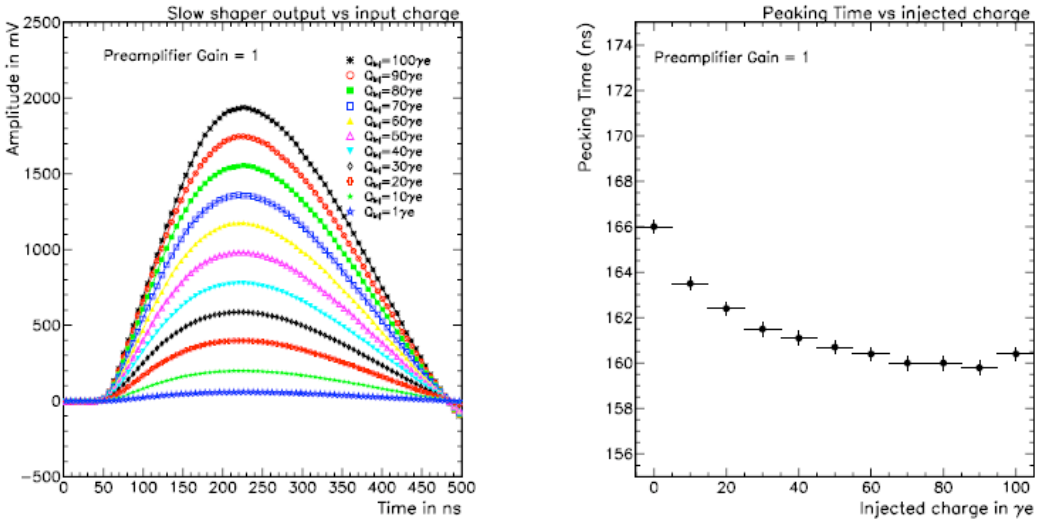


Figure 157: slow shaper output for various input charges and peaking time variation(right)

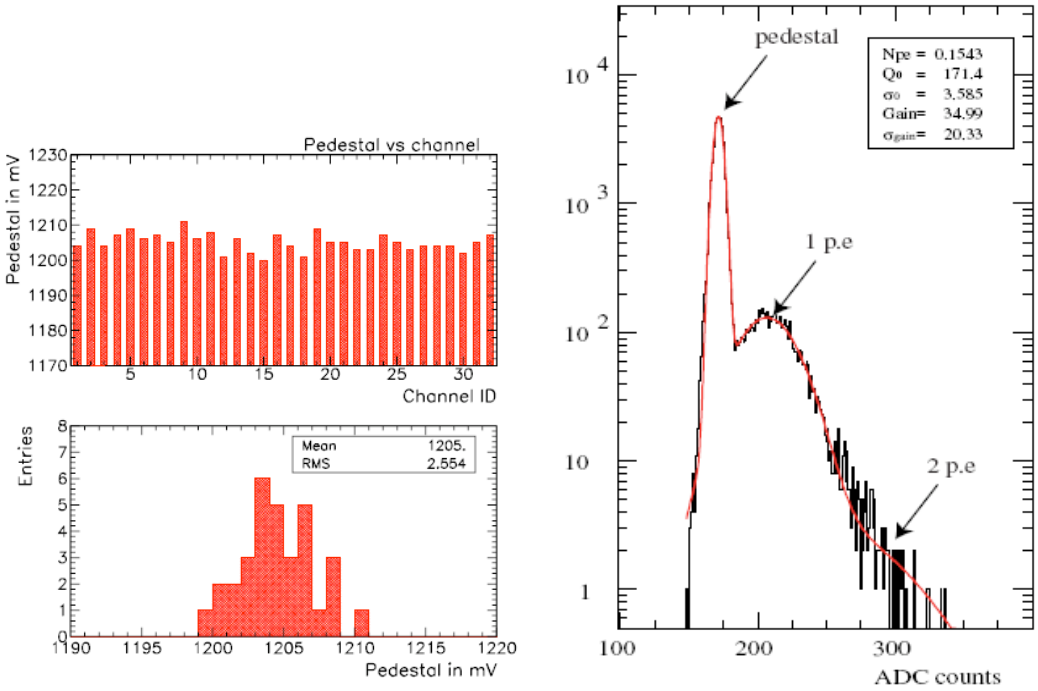


Figure 158. <u>Left</u> : pedestal dispersion for the 32 channels. <u>Right</u> : photomultiplier single photoelectron spectrum taken with the full OPERA readout chain

Performance of the OPERA Read Out Chip

PREAMPLIFIER	
- Gain correction	Range 0-3.5 (6 bit resolution)
- Input for Test Pulse	3 pF alternate (even/odd channels)
- Input Impedance	$Z_{in} \approx 100\Omega$
AUTO-TRIGGER:	
- Fast shaper peak time	10 ns
- Fast shaper gain (Gain 1)	2.5V/pC (400 mV/p.e.)
- Threshold spread (peak-to-peak)	$\pm$0.015 p.e.
- Fast shaper noise (Gain 1)	1.8mV (0.72fC or 0.005p.e)
- Trigger sensitivity	100% at 0.3 p.e.
- Hit Register	Implemented
CHARGE MEASUREMENT:	
- Dynamic range (Gain 1)	16 pC (100 p.e)
- Slow shaper peak time (Gain 1)	160 ns
- Slow shaper Gain (Gain 1)	120 mV/pC (19 mV/pe)
- Pedestal Spread (mV) (peak-to-peak)	$\pm$6 mV ($\pm$0.4 p.e.)
- Noise @ MUX rms (Gain 1)	1.3 mV (12fC or 0.075p.e)
- Cross-talk	$O(0.5\%)$
Linear Voltage range @ MUX	about 1.2 V to 3.2 V
Readout frequency	5 MHz (6.4μs/32ch.)

3. ATLAS luminometer and MAROC (NIM paper [25])

The successful operation of OPERA_ROC on a large scale experiment (60 000 channels) made the chip well known from many MaPMT users. It is no surprise that when ATLAS sought to readout its roman pots for luminometry measurements equipped with MaPMT, the Orsay group was contacted. However, several changes needed to be done :

∞ Technology change : 0.8 µm had fallen into obsolescence and the design had to be migrated into 0.35 µm SiGe

∞ Compacity increase : the PMTs had to be packed together and there was no room to fit any external components : everything had to fit inside the shadow of the PMT, that is 2x2 cm². In a sense, it was our first encounter with "3D" electronics !

∞ Compatibility with ATLAS readout

We thus took over OPERA_ROC basic architecture and migrated it into SiGe. The 64 channels were then integrated on the same die by arranging the bonding pads into staggered double row. The DAC setting the threshold was also integrated as well as a *Wilkinson* ADC in order to provide directly a digitized signal[87].

Concomitantly, design at the PCB level was also undertaken in order to fit in the allocated area.

3.1. Experiment overview and requirements

The ATLAS luminometer is described in [25]. It consists of 1000 scintillating fibers arranged in 10 planes coming to a fraction of millimeter of the beam in order to measure diffractive protons. The fibers are readout by an array of 5x5 multianode PMTs H7500 by Hamamatsu as shown in Figure 159. The detector is designed by the group of *C. Joram* at CERN and 8 roman pots will equip the beam line in 2009 at 240 m from the interaction point.

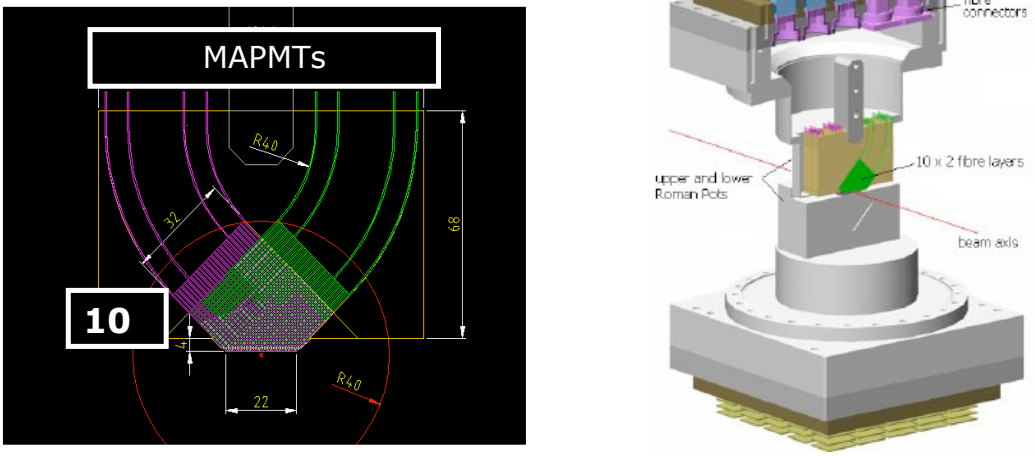


Figure 159 : ATLAS ALFA luminometer for absolute luminosity measurements (CERN design)

Each MaPMT is connected to a front-end board called PMF which is built in 3 stages and originally designed by Lund. Two boards provide the HV divider and the routing of PM signals to connectors on the side. The third board is the active board which houses on one side the MAROC2 readout ASIC

∞

[87] This was not requested nor used by ATLAS which only handles discriminator outputs, but was included for future applications

designed by Orsay and on the other side the Lattice FPGA that handles the digital data and connects to a motherboard designed by Lund and CERN that performs the DAQ.

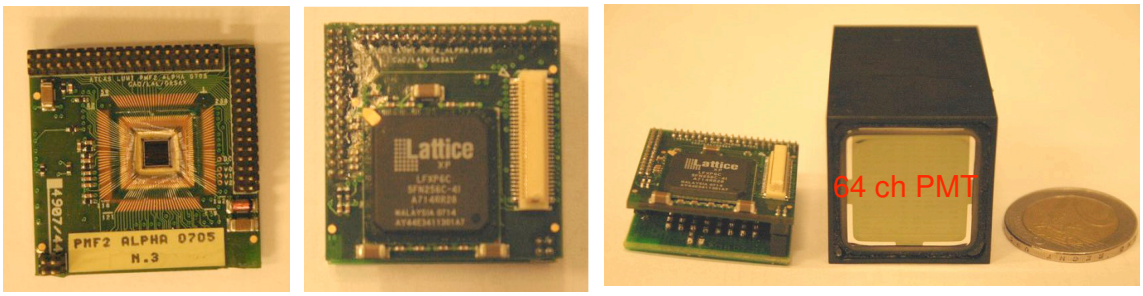


Figure 160 : PMF boards used to read-out each multi-channel PMT.

3.2. MAROC design

The readout ASIC called MAROC for Multi-Anode Read Out Chip opened the "ROC series" in 0.35 µm SiGe technology. It reused most of the analog architecture of OPERA_ROC (current conveyor, variable gain mirror, fast and slow shaper) but optimized with the 0.35 µm technology. The reduced capacitance allowed, in particular in the current mirror, to reduce the bias current and thus reduce the parallel noise and the power dissipation. New features were also tested such as a fast unipolar shaper, allowing a higher counting rate while reducing the DC offset, it will be detailed in section. Also two internal DACs provided 2 thresholds. The overall schematic diagram is shown in Figure 161.

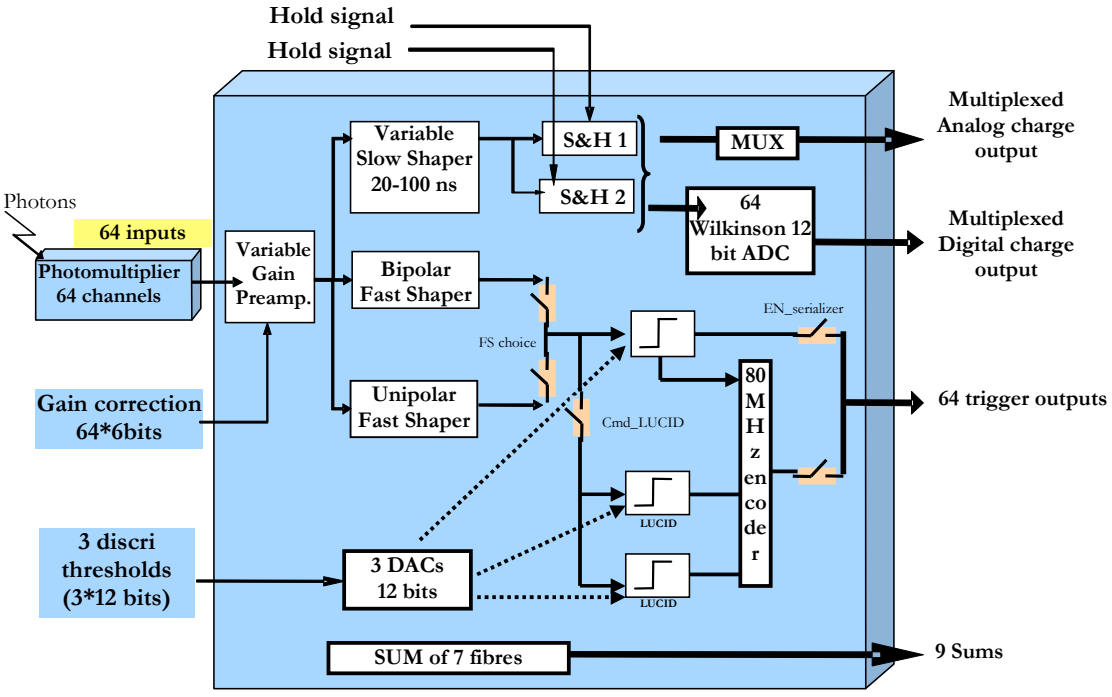


Figure 161: schematic diagram of MAROC2 ASIC.

Three versions of the chip have been realized :

∞ MAROC1 was the first prototype with 64 channels, realized in October 2005. The chip has been used in the first test beam in 2006, although a coupling between preamp outputs and inputs through the substrate was making it unstable when all channels were set with gains larger than 1.

∞ MAROC2 is the production version for ATLAS luminometer. It essentially corrects the instability of MAROC1 by separating all substrate connections from ground connections. Thus, no net current flows into the substrate and the substrate of the different regions are tied to ground externally to form a low pass filter on the substrate noise.

∞ MAROC3 is a version with lower dissipation that reuses several features from HARDROC described in Chapter 5.

The overall schematic of MAROC2 is shown in Figure 162 and the layout in Figure 163.

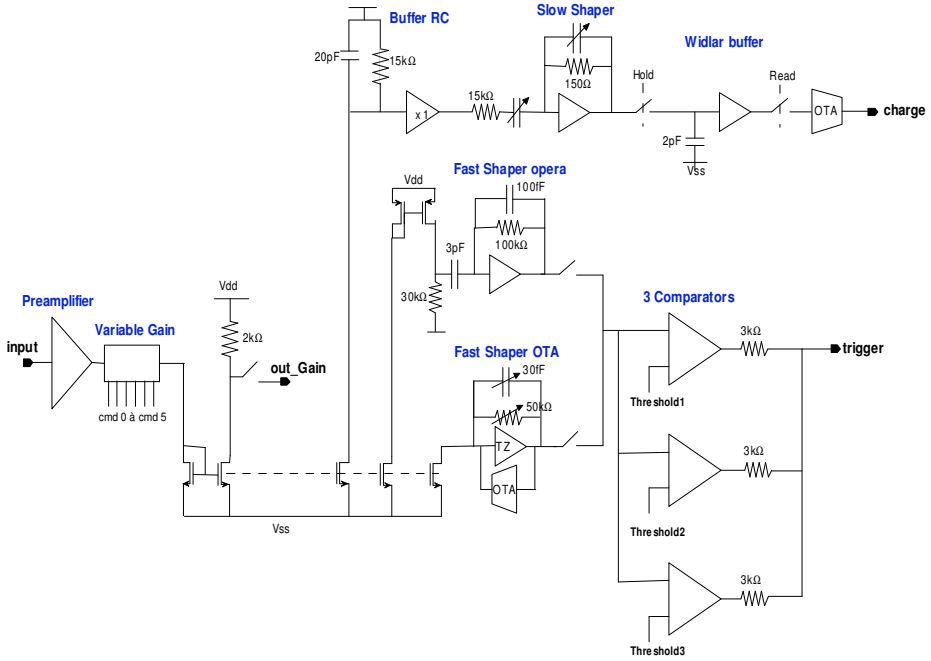


Figure 162: overall schematic of MAROC2

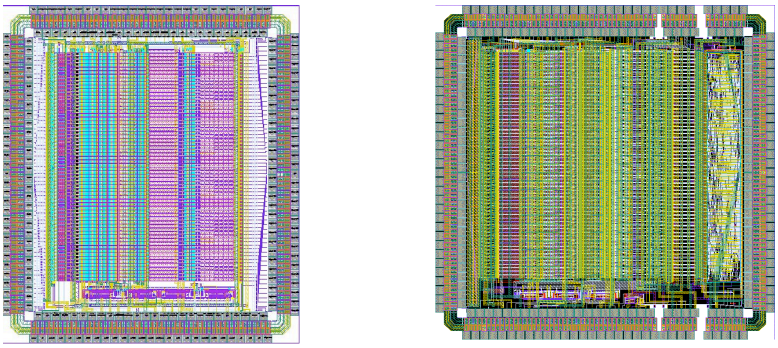


Figure 163: Layout of MAROC1 and MAROC2 in 0.35 µm SiGe BiCMOS. Chip area is 12 and 16 mm^2

3.2.1. Preamplifier design

The preamplifier follows closely the design of OPERA_ROC (cf § 2) with NPN transistors and PMOS mirrors, as shown in Figure 164. The transistor that determines the gain has been designed with an area of A=6 in order to reduce $R_{BB'}$ to 50 Ω for lower noise. The PMOS transistors have been scaled down 32/1 as compared to OPERA_ROC in order to minimize the capacitance and get good speed at small current. The bank of scaled mirrors is also cascoded to improve the linearity and switches in series allow to select the output currents that will be summed in the NMOS mirror that provides the multiple copies for the various subsequent stages (*cf.* Figure 162).

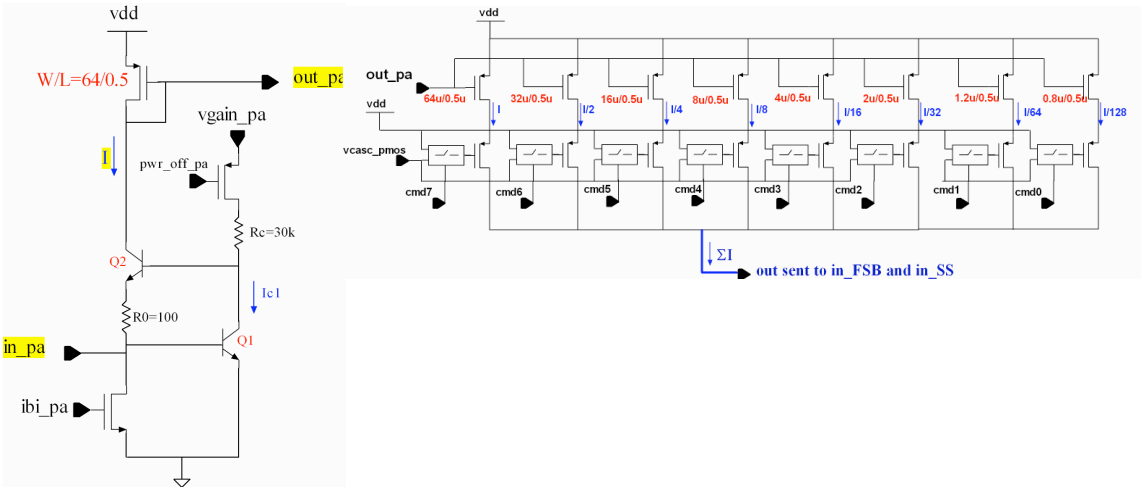


Figure 164: schematic diagram of the preamplifier of MAROC

3.2.2. Bipolar shaper

The bipolar shaper has the same architecture that has been used in OPERA_ROC and all versions of MAROC. The schematic is displayed in Figure 165.

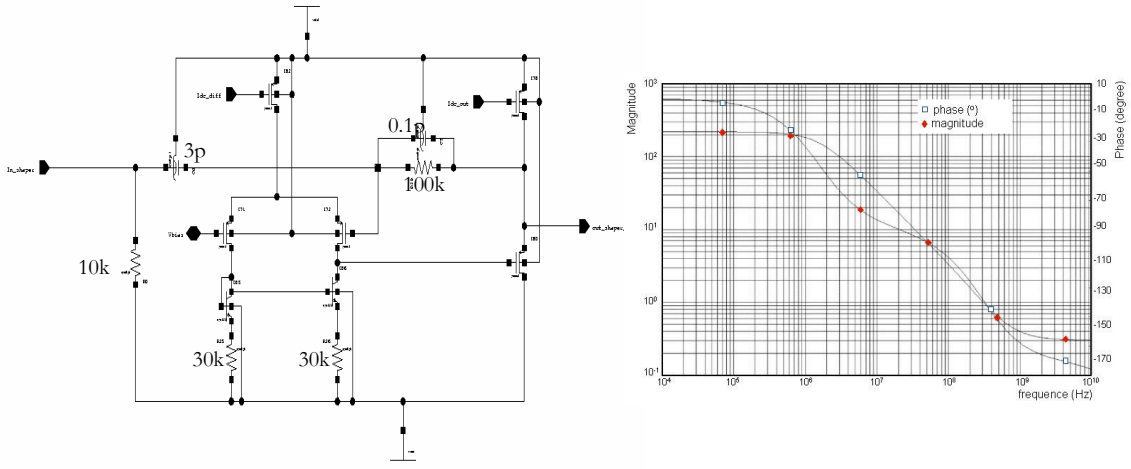


Figure 165. Left : schematic diagram of the bipolar fast shaper. Right : simulated open loop gain of the amplifier

It uses a relatively large PMOS differential amplifier with degenerated NPN as active load to minimize offset. The amplifier achieves an open loop gain of 220 with a gain-bandwidth product of 300 MHz. Coupled with 10 kΩ/3 pF to the input and feedback network of 0.1 pF/100 kΩ, it provides a gain of around 30 with a peaking time of 10 ns.

3.2.3. Fast unipolar shaper

In order to get shorter pulses and get rid of the relatively long occupancy due to the undershoot of the bipolar shaper, a unipolar architecture has been implemented, taking advantage of the low capacitance of the sigbnal source (the NMOS mirror) and the high speed of the SiGe process. It is based upon a transimpedance configuration (R_F=100 kΩ, C_F=20 fF) with a very high speed bipolar amplifier. The DC stabilization is built around a low offset OTA that cancels the DC current from the previous stage, which can vary between 0 and 60 µA, depending on the gain setting. To keep the offset below the mV, the transconductance of this OTA must thus be in the A/V range !

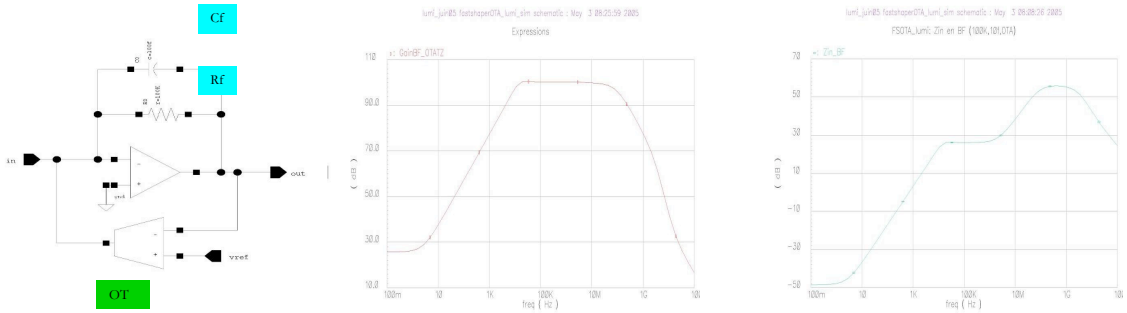


Figure 166: synoptic of the fast unipolar shaper.

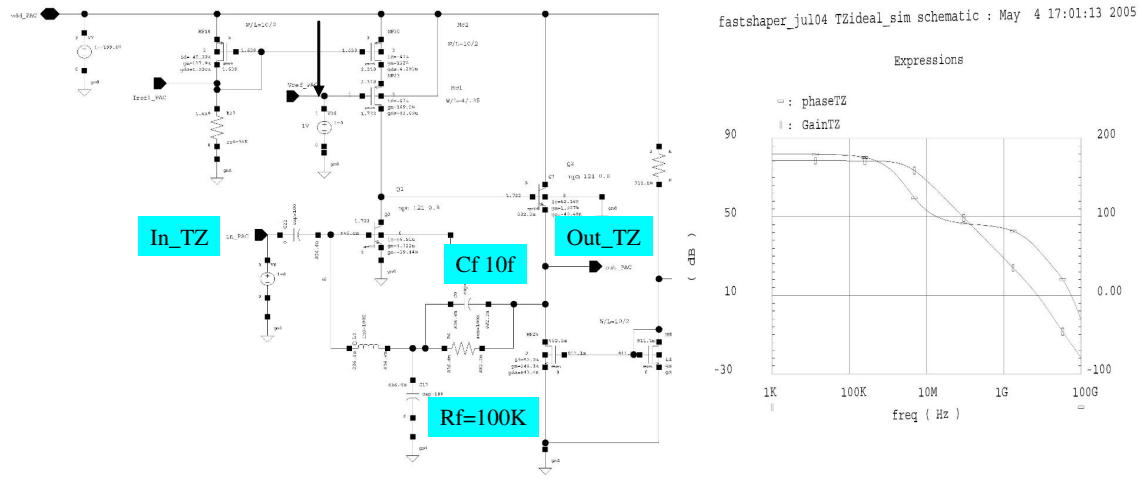


Figure 167. Left : schematic of the transimpedance amplifier in SiGe. Right : simulated open loop gain and phase vs frequency. A value of 70dB with a bandwidth of 3 GHz is obtained.

3.2.4. Discriminator

The discriminator is the same structure that is used on almost all the chips. It is formed of a differential NPN pair mounted in centroïd configuration with resistive load to get a gain around 30, while insuring low offset. It is followed by a second PMOS differential pair loaded by a NMOS small with mirror. The pulse is then enough to drive a series of inverters. The performance is very good with offset lower than 1 mV *rms* while maintaining high speed and low power consumption (100 µW).

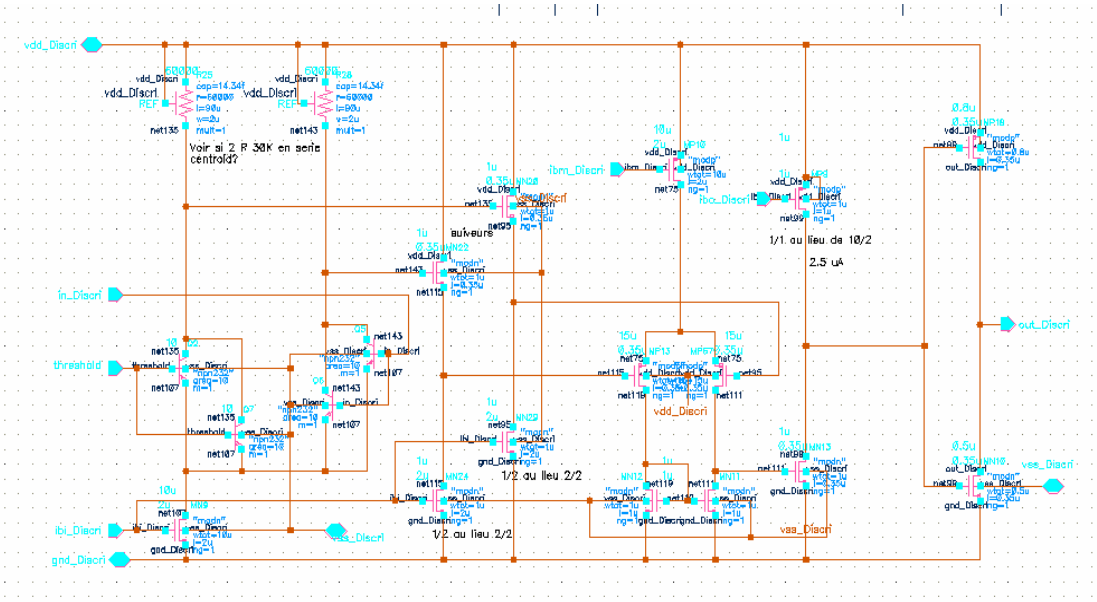


Figure 168 : schematic diagram of the low-offset discriminator

3.2.5. Slow channel

As shown in the top part of Figure 162 , the slow signal is obtained in integrating the incoming current on a 10 pF/ 15 kΩ network. This first is RC shaping is followed by a classical CRRC shaper and a double Track and Hold that allows to sample both pedestal and signal peak. The hold signal comes from outside is directly fed to a CMOS switch. A voltage follower buffers the held voltage and allows to multiplex the 64 channels on one charge output in a few hundred ns.

3.2.6. DAC

The DAC is used to the set the discriminator threshold on the 64 channels. A 12 bit structure is made with 4 bits MSB coming form a thermometer structure followed by 8 bits in scaled mirrors as shown in Figure 169. This complicated architecture did not give better results than a simple binary-scaled array of mirrors[88] and was subsequently dropped in favour of the 10-bit architecture developed for HaRDROC (cf Chapter 4, §4)

∞

[88] In fact, what counts is the overall transistor area for low offset and good randomization of transistor implantation in order to average systematic variations.

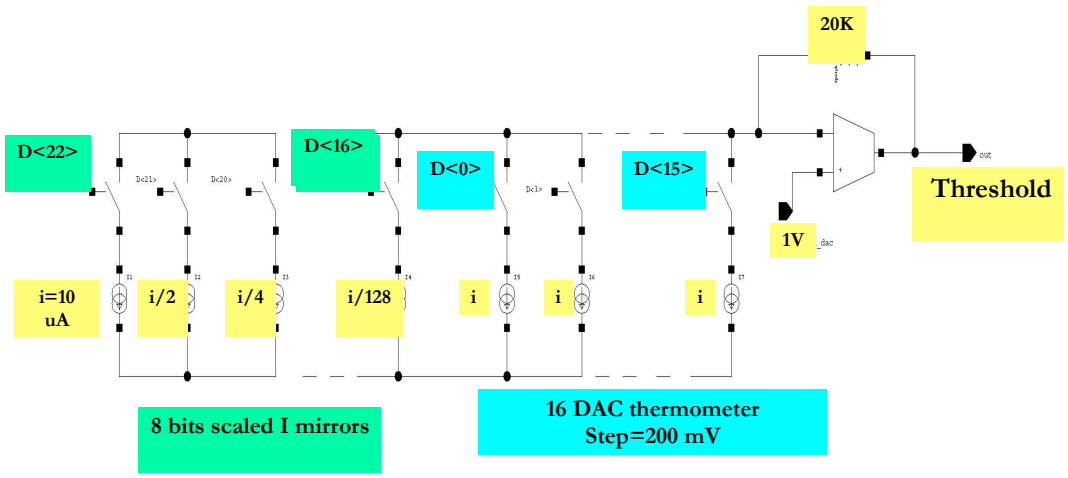


Figure 169: DAC schematic for MAROC

3.3. MAROC1 performance

The most relevant measurements are summarized below. The gain adjustment shown in Figure 170 exhibits a good linearity of ±1% over the adjustment range 0 to 4. The signal shape is well conserved, independently of the gain setting. The gain setting of 0 can be used to mask or disable a noisy pixel. The pedestal dispersion shown in Figure 171 gives an *rms* value of 3 mV, in good agreement with the offset expected from the slow shaper amplifier and voltage buffer in the signal path. The linearity also displayed in Figure 171 exhibits an integral non linearity of ± 2% in line with the simulations and expectations from a simple current mirror at low bias current, in which the signal gets quickly much larger than the bias current.

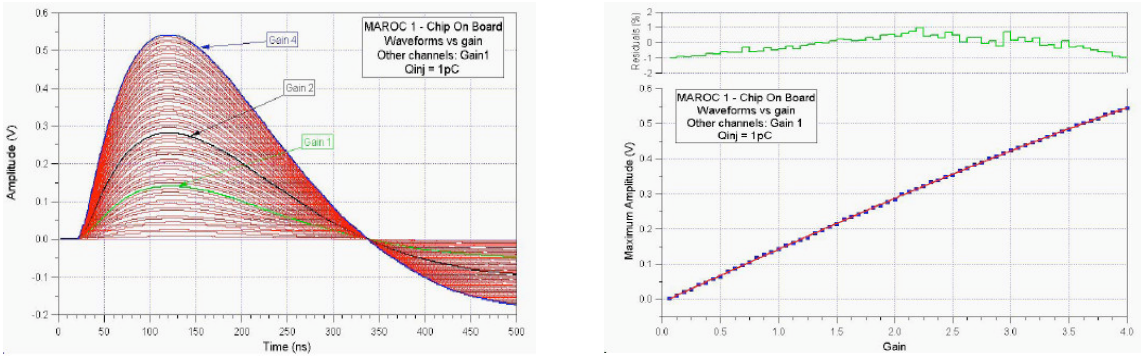


Figure 170 : slow shaper output for different preamp gains (0 to 4) and linearity of the gain adjustment

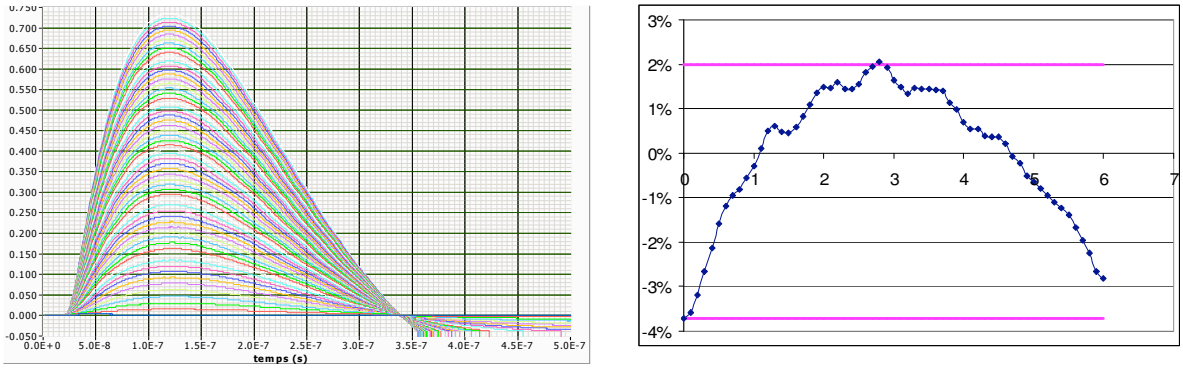


Figure 171 : pedestal dispersion on the 64 channels of the slow shaper and non linearity up to 6 pC input charge (40 pe)

Trigger efficiency : the s-curves (Figure 172) show an easy triggering at 1/3 photoelectron (50 fC) with a nice narrow dispersion of 4 fC over the 64 channels without any tuning. Converted into voltage at the discriminator input, this corresponds to 4-5 mV *rms*. Two contributions (at least) can account for the threshold dispersion : the dispersion of the offsets of fast shaper and discriminator and the variation in gain between the different channels, as is clearly visible in Figure 173. The contribution from the offsets can be extracted by making the s-curves without any signal on the input.

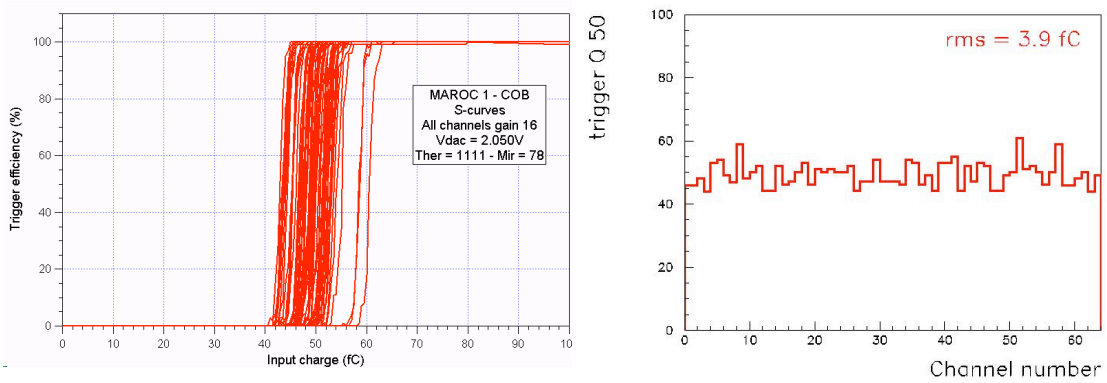


Figure 172 : S-curves on MAROC1 with a threshold of 50 fC. The dispersion is 4 fC rms

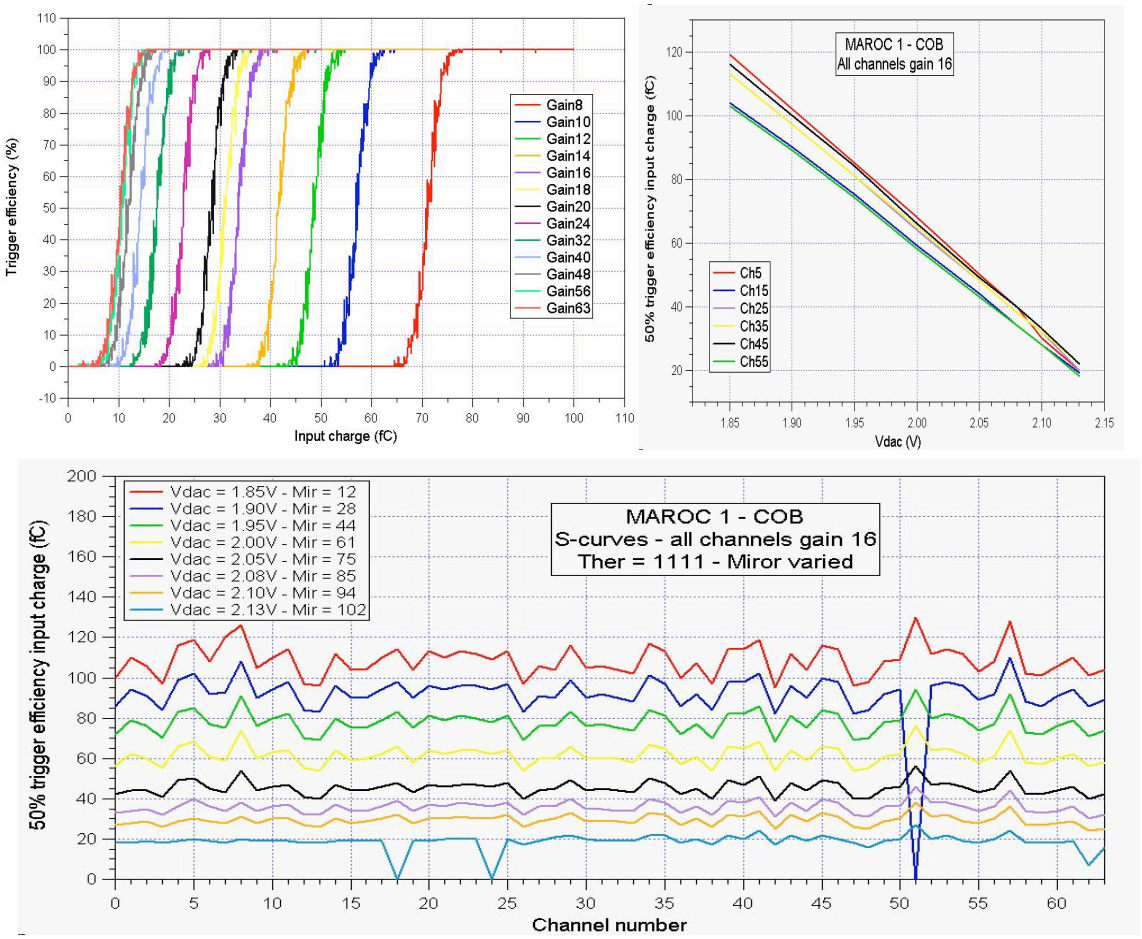


Figure 173 : S-curves for various preamp gain. The trigger scales (fortunately) linearly with the gain setting and the resuslts for various thresholds (lower plot) show the disperison due to gain dispersion from the one due to offsets dispesion

DAC performance : the DAC linearity is displayed in Figure 174, showing an integral non linearity better than ±0.5%, which is far from a real 12 bit but enough for setting a threshold.

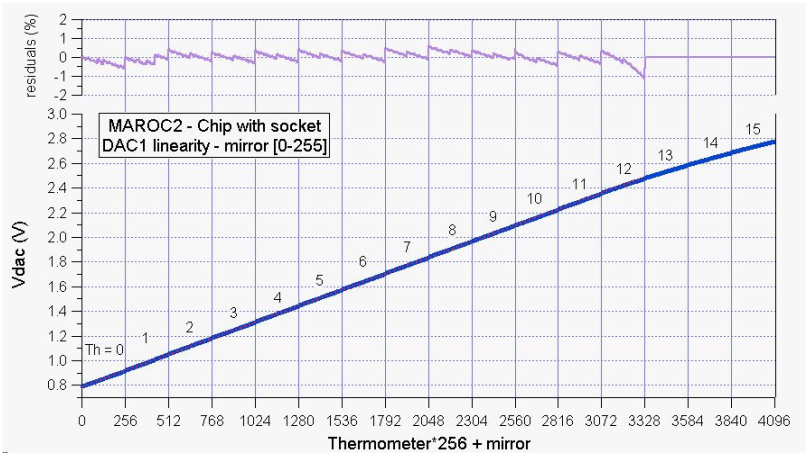


Figure 174 : DAC linearity

Substrate coupling : one unexpected difficulty with MAROC1 was the instability that appeared when trying to raise the gains on all channels above 2 which would make the chip oscillate. This did not happen on OPERA-ROC although a very first prototype had shown us the importance of separating substrate from ground connections[89]. The main difference was a much smaller resistance between the substrate connections of the first and second stage, which came down to a few ohms because of a lower substrate resistivity and also of a much smaller distance between the contacts. The bonding inductance also played a visible role, as the chip on board was better than the soldered chip which itself was much better than the chip in its test socket. In effect, this inductance prevents from keeping the substrate voltage stable at high frequency, allowing the coupling via the substrate resistance between input and output stages, as displayed in Figure 175.

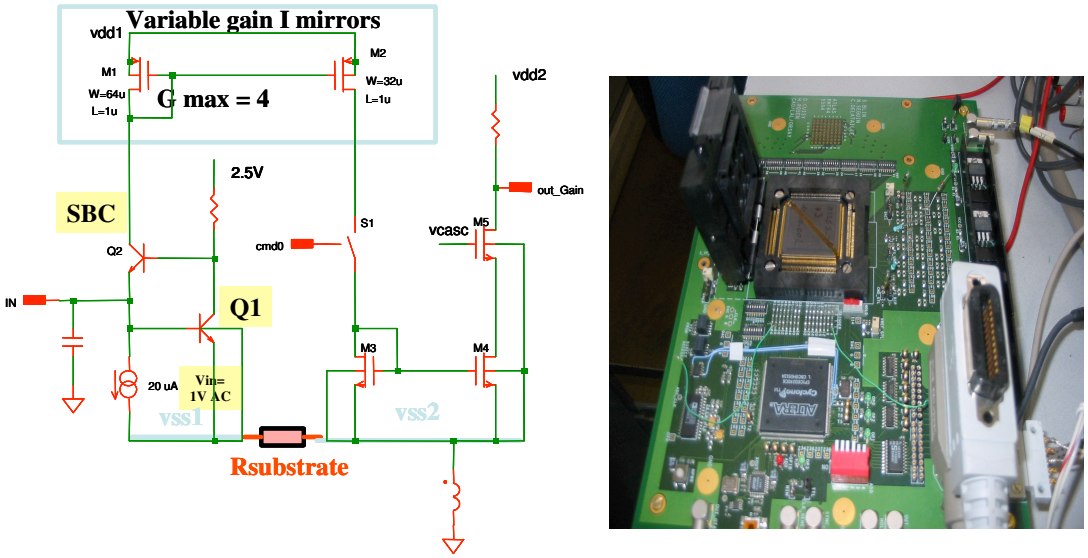


Figure 175: substrate coupling between input common base amplifier and output mirror. This positive feedback coupled with bonding inductance led to oscillations at high gain.

3.4. MAROC2 performance

The main change between the first and second versions concerned mostly the substrate coupling mentioned above and the digital logic levels. The unipolar shaper was also included to increase the speed of response and DC uniformity. Indeed, as shown in the DC pedestals measurements of Figure 176, the dispersion is twice better for the unipolar than the bipolar, coming down to 1 mV *rms*. This reflects in the s-curves[90], which show a dispersion of 2 fC, similar to the noise.

∞

[89] The amplification between input and shaper output is around 10^3: a single photoelectron produces around 500 µV on the input and 200 mV at the output, thus any fraction of mV on the ground can lead to oscillations

[90] Unfortunately, the s-curves could not be performed on the bipolar shaper as its polarity is inverted, producing the reverse pulse polarity which was affecting the reference HSTL voltage and providing meaningless data to the readout FPGA.

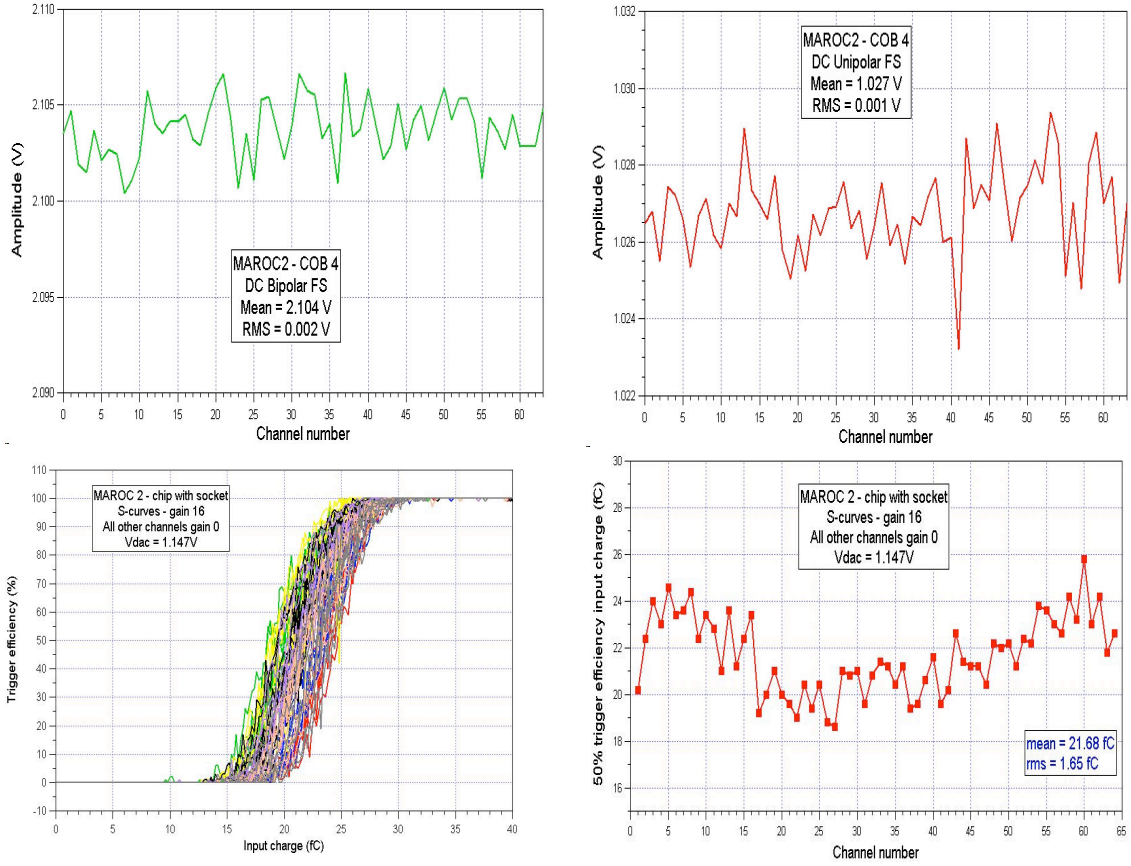


Figure 176. *Top* *: DC uniformity of bipolar and unipolar shapers, showing a dipersion twice better for the unipolar.* *Bottom* *: s-curves (Trigger efficiency vs input charge) of the 64 channels for a threshold of 50 fC and dispersion of the 50% point*

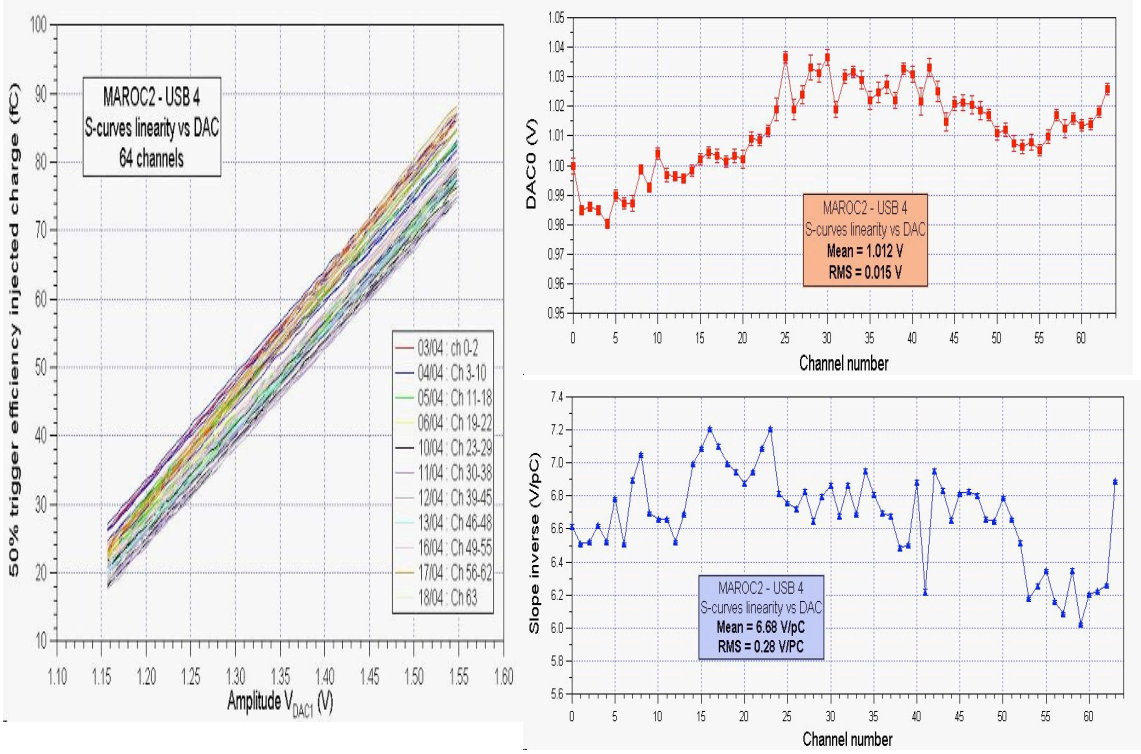


Figure 177 : 50% Trigger efficiency as a function of input charge, allowing to extract gain and pedestal for the 64 channels

3.5. MAROC3 performance

MAROC3 has been submitted in November 2007 and received in march 2008. It incorporates mostly changes based on the results from HARDROC (cf Chapter 5 §2). In particular, the DACs have been changed to go to a simpler 10 bit configuration with only scaled mirrors and a bandgap reference generator has been included. The results are very similar to Hardroc

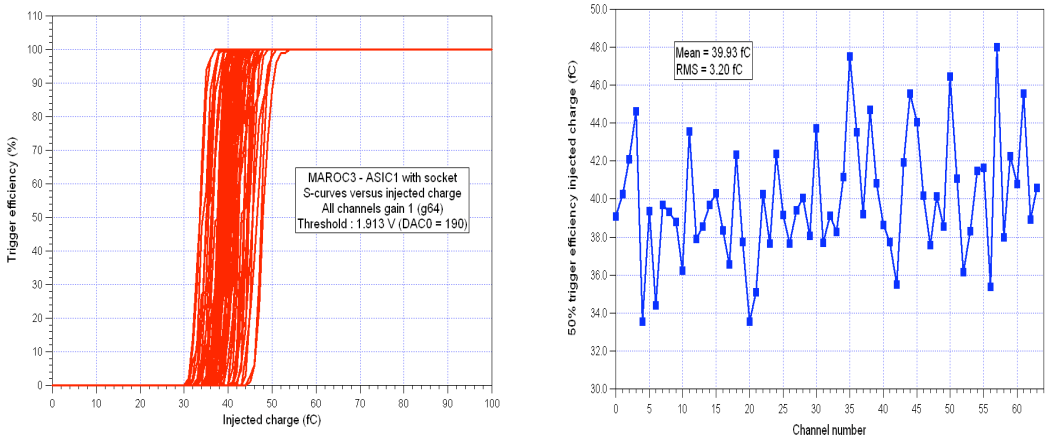


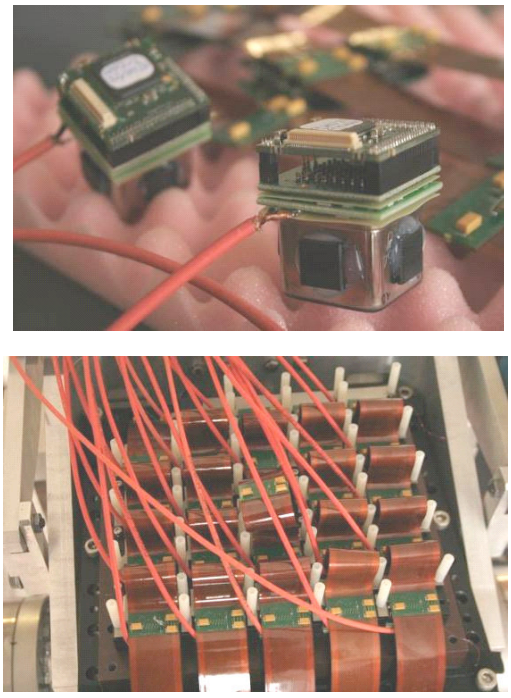
Figure 178 : S-curves on MAROC3 for 40 fC and dispersion of the 50% trigger for the 64 channels, exhibiting an rms of 3 fC

3.6. Conclusion on MAROC

The MAROC was found versatile enough to be used by other experiments, such as double Chooz, which uses a target tracker similar to the one from OPERA. It is also used by various medical Imaging teams that get better spatial resolution by coupling their scintillators directly to a MAPMT.

One drawback of MAROC is the 64 trigger outputs that make a lot of external connections on a PCB that is often very small. In particular, when moving to 256 pixels PMTs, the routing of the PCB gets too intricate and other chips such as HARDROC are being used instead.

	OPERA_ROC	MAROC1	MAROC2	MAROC3	HARDROC
gain correction	0-3.5 (6 bits)	0-4 (6bits)	0-4 (6bits)	0-2 (8 bits)	0-2 (8 bits)
fast shaper gain	2.5 V/pC	1 V/pC	6 V/pC	6 V/pC	3.5 V/pC
fast shaper noise	1.8 mV				1 mV
trigger dispersion at 50fC		4 fC	4 fC	3 fC	1 fC
slow shaper gain	120 mV/pC	150 mV/pC	160 mV/pC		
#channels	32	64	64	64	64
power dissipation/ch	5 mW	5 mW	5 mW	2 mW	1.6 mW



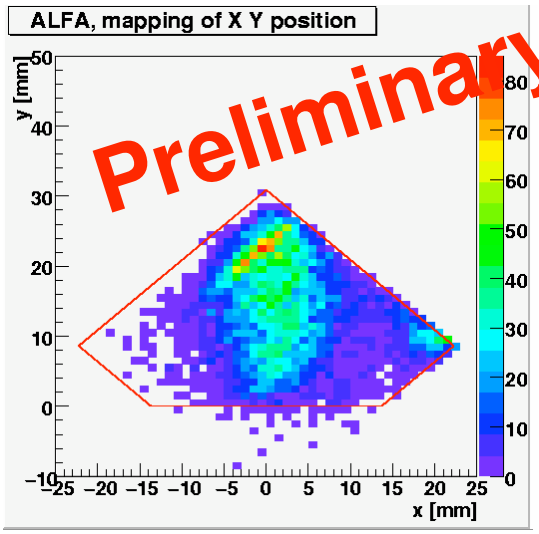


Figure 179 : view of the PMF mounted on the MaPMT and the complete detector with the 25 PMFs, connected with flexible kapton cables. On the right, a reconstruction of the beam profile hitting the fibres in the detector

4. PMm^2 (PhD work by *S. Conforti*)

The concept of low cost multi-channel readout ASIC found an interesting evolution in the readout of huge photodetection areas in proposals of large neutrino experiments using water Cerenkov detectors, as continuation of the *Super-Kamiokande* family. The front-end ASIC has a crucial role in this R&D as it evolves toward a *System-On–Chip* (SoC), self-triggering and digitizing internally the data to turn the detector into a "smart sensor"

4.1. Project overview and specifications (ANR PMm^2)

Replacing large and onerous photodetectors by arrays of smaller ones has been proposed by Photonis at the NNN05 workshop [25] to make the next generation of such detectors affordable[91]. This relies on the integration of the front-end electronics on the array itself to turn it into a "smart sensor".

This project, dubbed PMm^2 standing for "square meter photmultiplier" has been proposed and accepted by the ANR in 2006, led by *JE Campagne* and associating IPNO on the mechanical aspects and LAPP Annecy for the DAQ. It proposes to build a demonstrator of 1 m^2 of 4x4 12" photomultipliers, readout by an ASIC similar to MAROC named PARISROC (standing for Photomultiplier Array Integrated SiGe Read Out Chip).

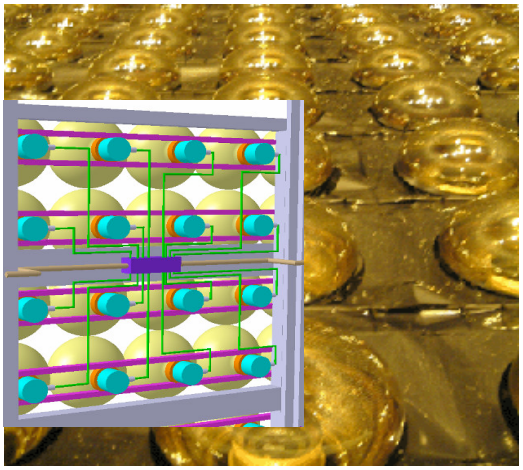


Figure 180 : principle of the square meter photomultiplier array PMm^2

The specifications of the chip are the following :

- ∞ Variable gain to use a common high voltage for the 16 photomultipliers
- ∞ 50 Ω input impedance to terminate the cable from PM to ASIC
- ∞ Auto-trigger on 1/3 photoelectron = 50 fC
- ∞ Charge measurement up to 200 photoelectrons = 32 pC
- ∞ Time measurement better than 1 ns
- ∞ Internal ADC and TDC : digital data out

4.2. chip design

As said earlier, the chip integrates many functions as it globally needs to auto-trigger asynchronously on any single photoelectron and provide the digitized time and charge information to the DAQ. The chip architecture is shown in Figure 181. It follows globally a similar architecture as MAROC with variable gain preampllifer, slow shaper for charge measurement and fast shaper to drive the discriminators. The main differences are the following :

- ∞ the variable gain preamplifier is a voltage amplifier with variable feedback instead of a current conveyor. This provides better linearity and noise.
- ∞

[91] Comparing the cost per photoelectron, per cm2 for 20" and 12" PMTs. A 20" is estimated 2500€ for an area of 1450 cm2 whereas a 12" costs 800€ for an area of 615 cm2. Adding a better quantum efficiency (25% vs 20%) and collection efficiency (70% vs 60%) the price comes to 14.4 €/pe/cm2 compared to 7 €. Moreover the better granularity can largely improve the physics reconstruction and overall efficiency

∞ The Track&Hold is doubled, in a "ping-pong" mode in order to minimize the dead time during digitization : while a channel is digitized, the shaper output is sent to the second capacitor. This allows a random rate of events of 5 kHz.

∞ The hold signal is generated internally form the discriminator (or auto-trigger) signal, after going through a delay box, tunable on 5 bits between 0 and 200 ns.

∞ All channels are handled independently by the digital part. The channels that have triggered are digitized and the data transferred to the internal memory and sent-out in a data-driven way.

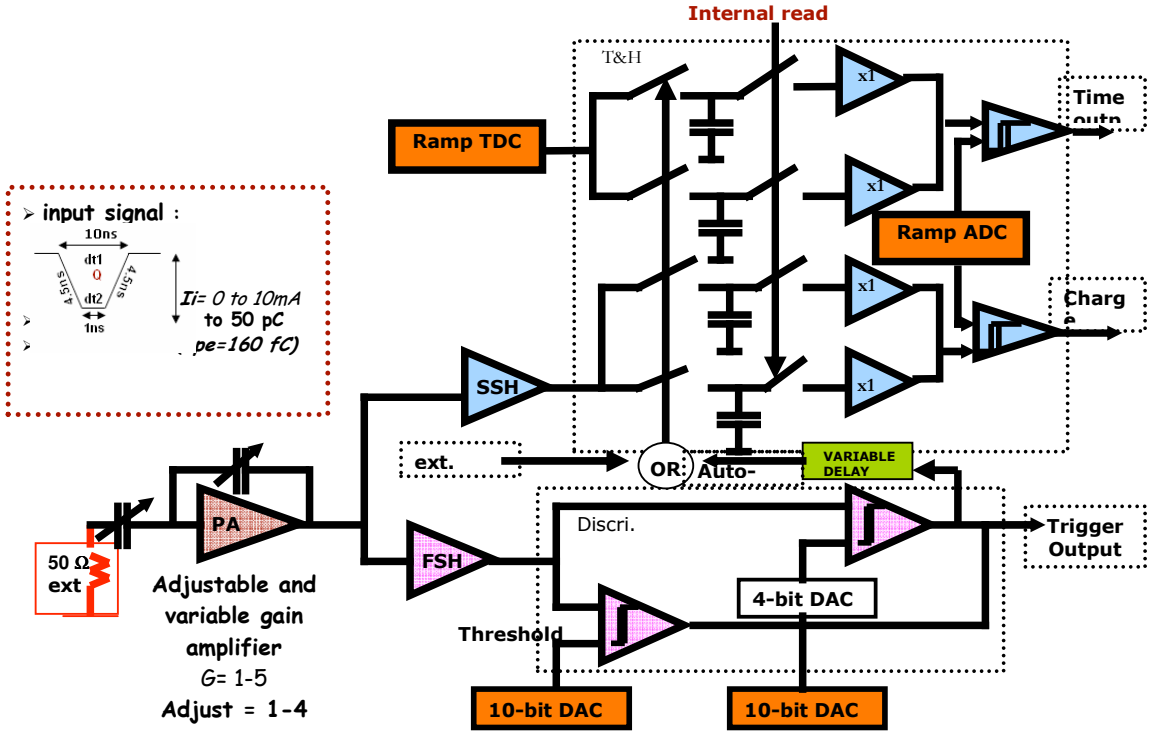


Figure 181 : schematic diagram of PARISROC ASIC

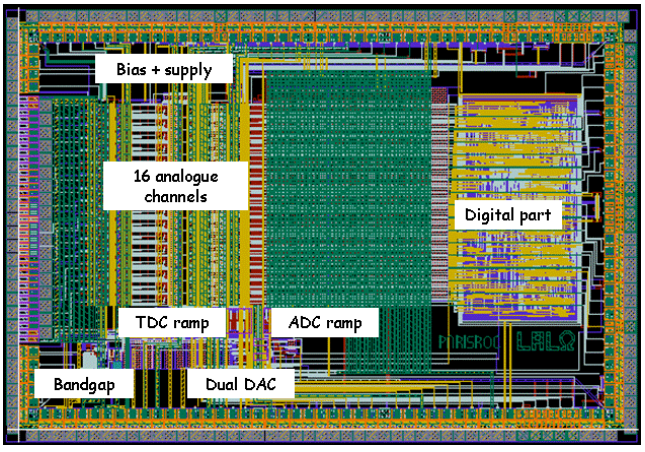


Figure 182 : PARISROC layout. Chip area : 17 mm^2, fabricated in june 08 in SiGe 0.35µm

4.3. Chip performance

Globally the performance is in good agreement with simulations, with a chip functional in its overall behaviour. One unexpected[92] problem is the high clock noise that doubles the noise and prevents operation below 100 fC .

4.3.1. DAC

The DAC linearity is similar to the other chips with 0.1% or 2 mV

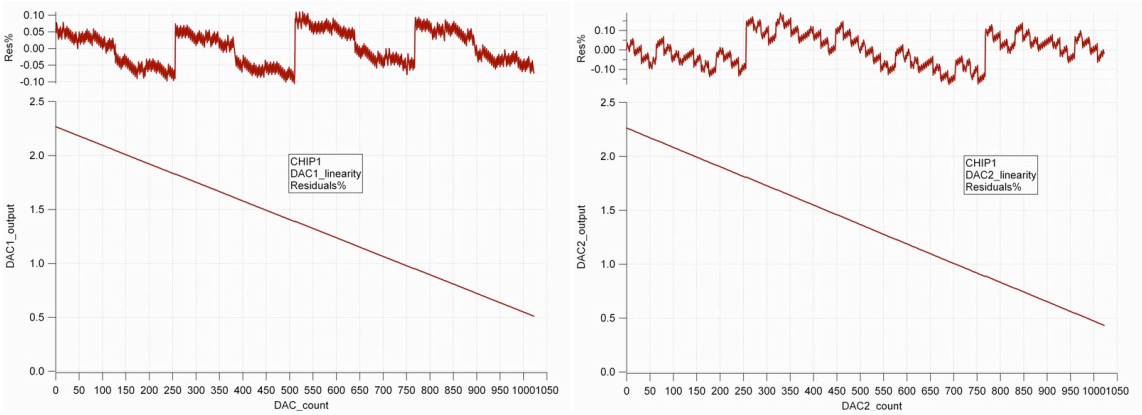


Figure 183 : DAC linearity for the two 10-bit threshold DACs. The residuals are at the level of ±0.1%

4.3.2. Preamplifier :

The preamplifier can be studied thanks to an internal probe register and exhibits a very fast rise and fall time as displayed in Figure 184. The amplitude is 44 mV/pC for a gain setting of 14 (7 pF/0.5 pF).

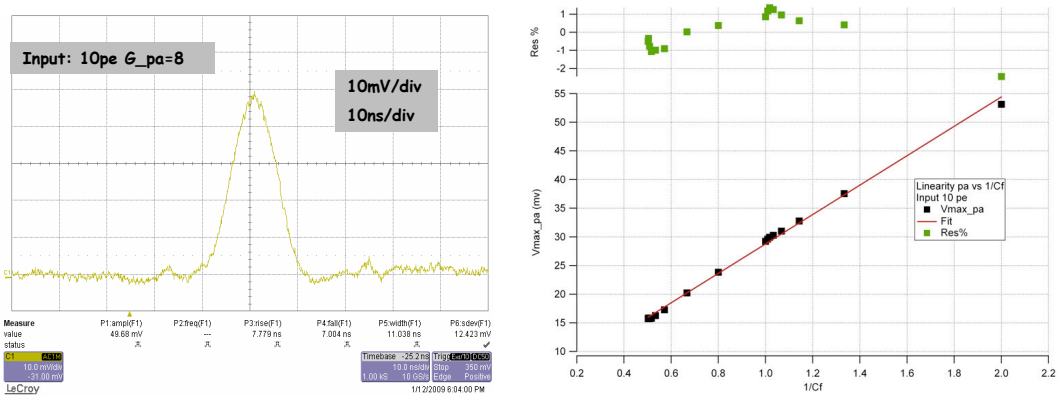


Figure 184. Left : preamplifier output waveform for 10 photoelectron (1.6 pC) input pulse. Right : Linearity of the gain adjustment mechanism around C_F=0.5 pF. A factor of two is obtained in both directions with a linearity of 1%.

[92] The chip architecture is similar to HARDROC or SPIROC which do not exhibit such clock noise. The coupling goes through the substrate (or the power supplies) despite the use of special 3B library with separated gnd and vss.

4.3.3. Fast shaper and discriminator :

The fast shaper is similar to the one used in SPIROC (cf Chapter 4 §4). It exhibits a risetime of 7 ns and a gain of 200 mV/pC. The noise is 2.5 mV *rms*, corresponding to 8 fC. The s-curves shown in Figure 185 exhibit a very good uniformity. The pedestal curves overlap, giving a dispersion of 0.9 mV *rms* (0.4 UDAC) and the response to 10 p.e. shows a dispersion of 4.4 mV *rms* (2.2 UADC) dominated by the gain dispersion.

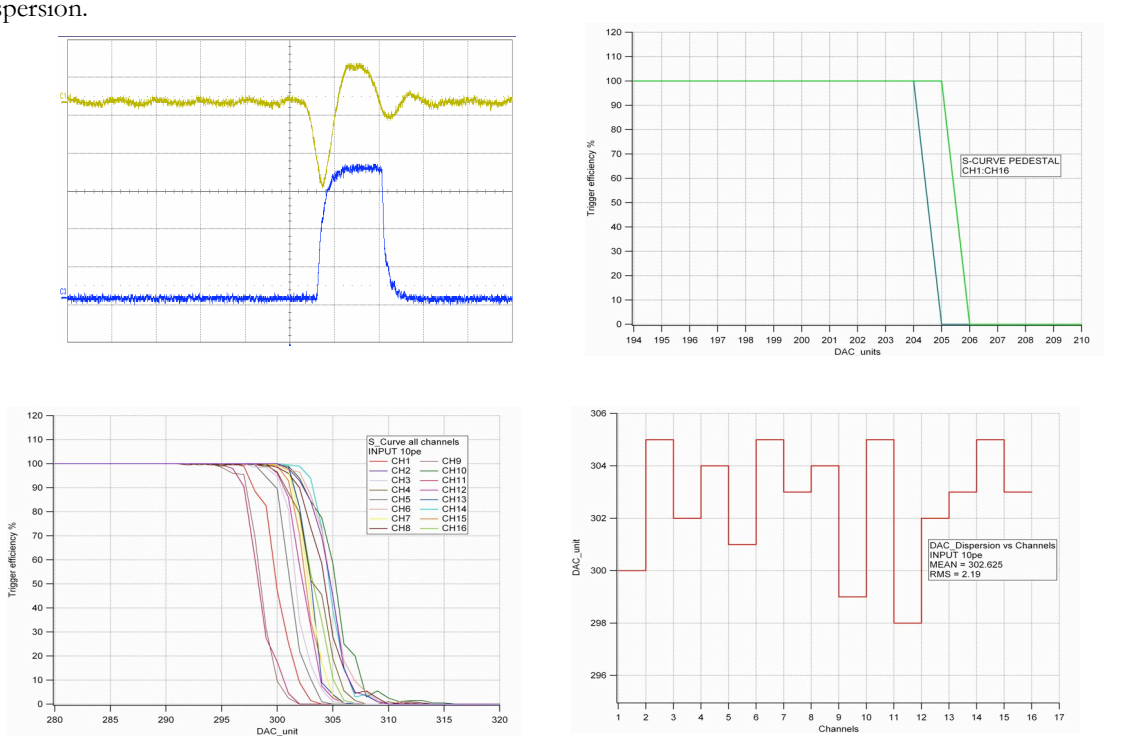


Figure 185. <u>Top left</u> : waveforms of fast shaper and discriminator outputs for one photo-electron input (160 fC) un-averaged to also show the noise. <u>Top Right</u> : S-curve on pedestal. <u>Bottom left</u> : S-curve for 160 fC input signal. <u>Bottom Right</u> : dispersion of the 50% trigger threshold over the 16 channels

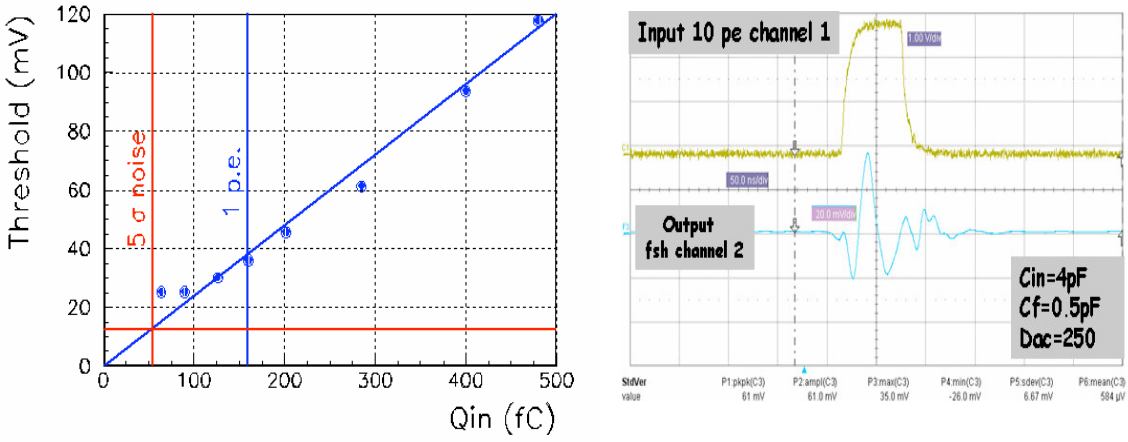


Figure 186. <u>Left</u> :Threshold as a function of input charge. The minimum threshold of 100 fC corresponds to 10 times the noise instead of the theoretical value of 5 because of the discriminator coupling to the input as shown in the right plot.

4.3.4. Slow shaper and Track & Hold :

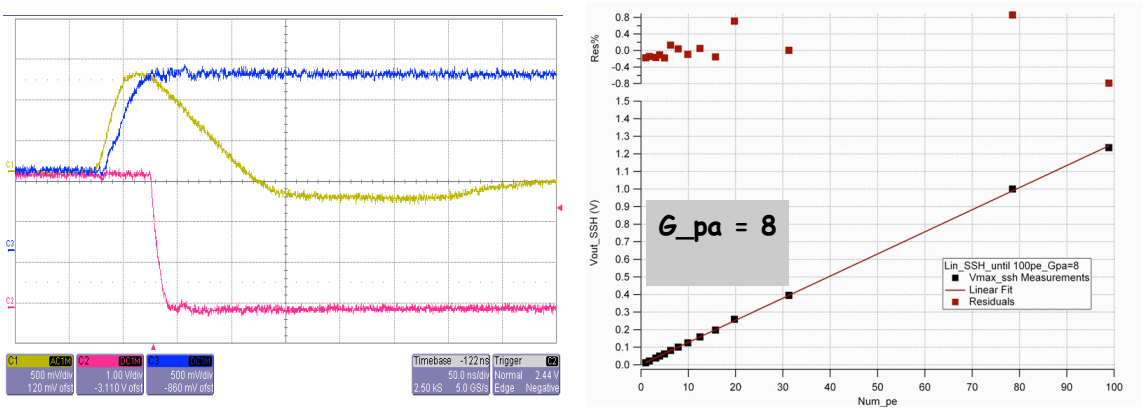


Figure 187. Left : Slow shaper output

4.3.5. Internal ADC :

The Wilkinson *ADC has been measured in standalone mode by sending a DC signal on the test input. The results are shown in*

Figure 188, from the on-line *Labview* display. The 15 channels[93] show a very good uniformity of ± 2 ADC counts. The noise is between 0.5 and 1 ADC count on all channels and there is no count outside ± 2 ADC count.

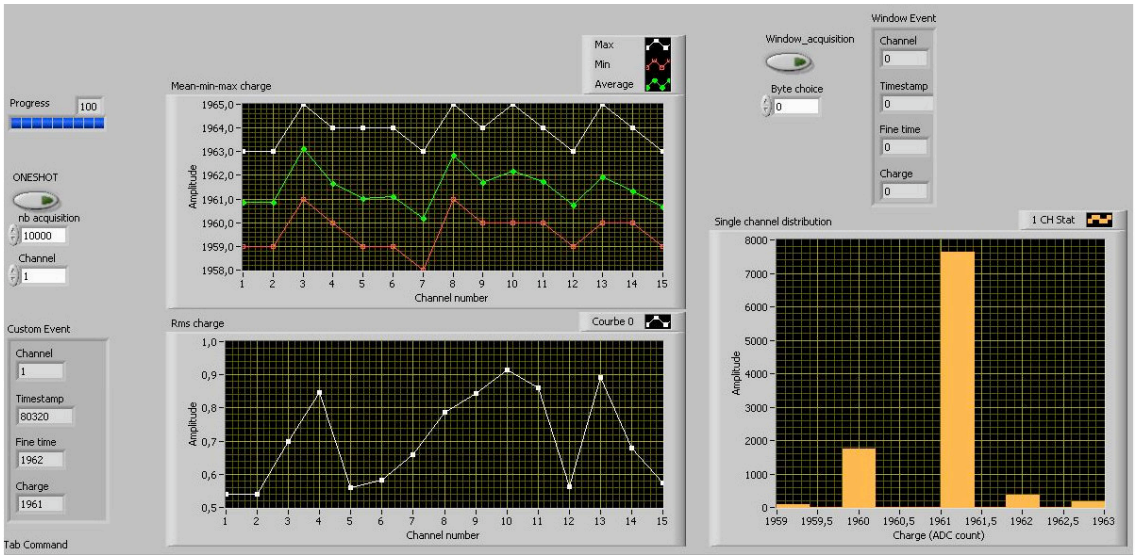


Figure 188 : On line display of ADC measurement. Top left : minimum (red), average (green) and maximum (white) ADC values for the 15 channels. Bottom left : rms dispersion vs channel number. Right : histogram of a given channel.

∞

[93] One channel (#13 !) unfortunately is short-circuited at the input

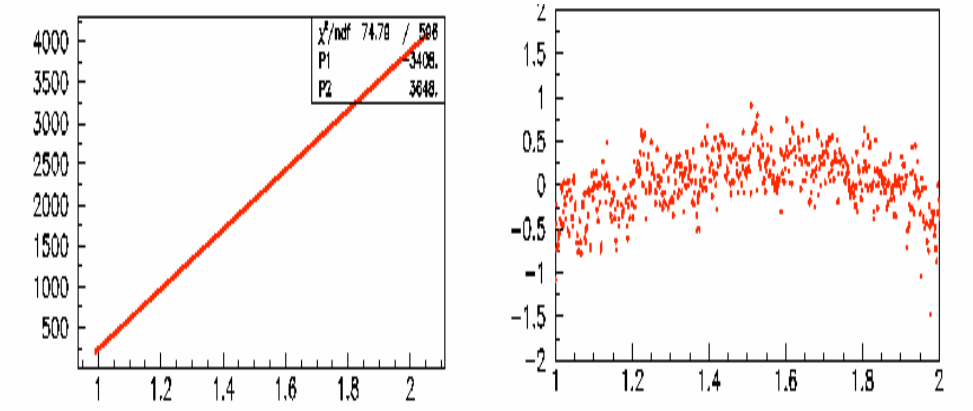


Figure 189: ADC linearity in 12-bit configuration for the 15 channels superimposed

4.3.6. Overall performance

The operation of the full chain has been validated. A signal is sent on the input which auto-triggers the chip, generates the internal hold and digitizes the stored signal. The input signal is varied from 0.5 to 30 pC corresponding to 3 to 50 photo-electrons at a gain of 10^6. The results displayed in shows a linearity within 1% and a noise of 6 ADC counts corresponding to 0.3 photoelectron.

Although very encouraging for a first test of a complete self-trigger-digitizer readout chain, the dynamic range needs to be extended and the sensitivity improved by an order of magnitude to reach the target of 0.3 photoelectron threshold.

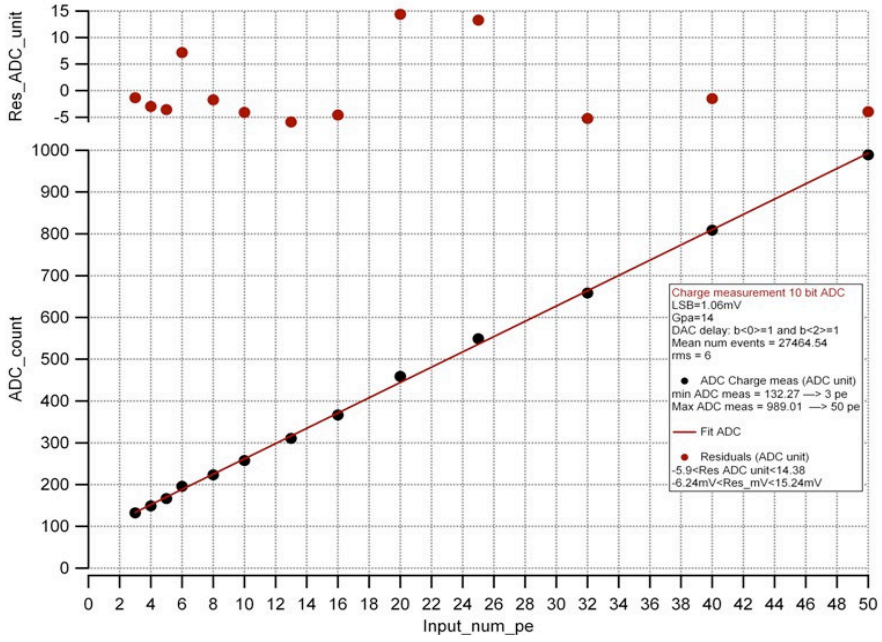


Figure 190: overall response of PARISROC using the auto-trigger, internal track and hold and internal 10-bit ADC

A measurement has alos been performed at IPNO by *B. Genolini* with a real PM to study the behaviour in real conditions. The result is shown below (Figure 191).

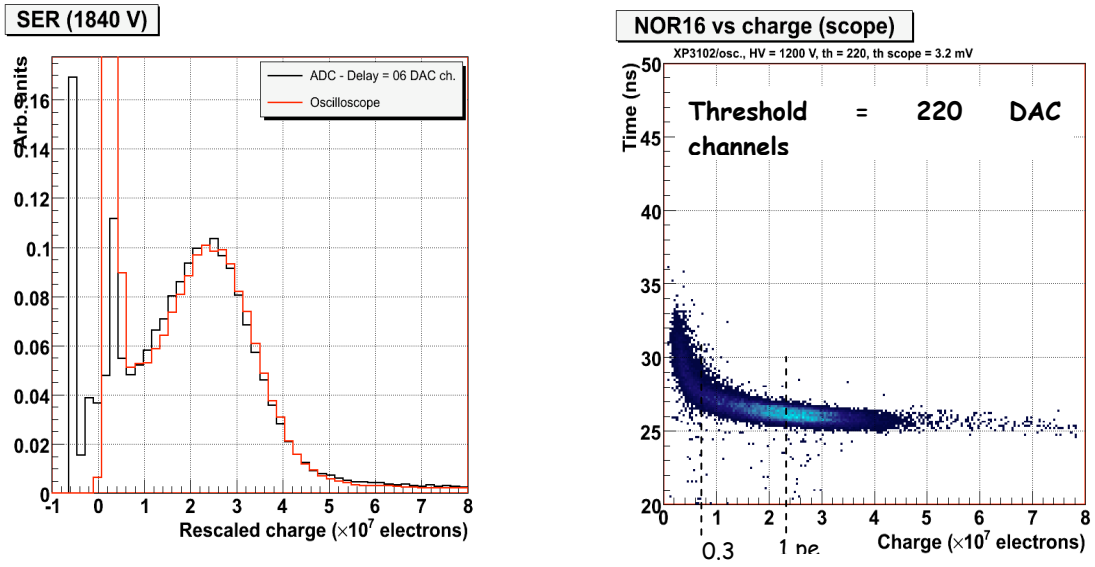


Figure 191. Left : single photo-electron response measured with PARISROC and a XP8010 photomultiplier. The red curve compares to the direct measurement with an oscilloscope and shows the similar spectrum and the good peak to valley of 2 obtained with the system. Right : time measurement measured on the discriminator output of PARISROC and a a XP8002 (2") photomultiplier. The time walk corresponds to the shaper rise time and after correction, the time resolution is 0.6 ns.

4.4. PARISROC2 design

Three main features have to be improved in PARISROC :

- Extend the dynamic range.
- Reduce the dead-time
- Improve the time measurement accuracy

The dynamic range is limited at the low end by the clock noise and digital coupling to the inputs. This should be improved by revisiting the layout to make it more similar to HARDROC or SPIROC which do not exhibit such problem (*cf* Chapter 5). Thus, the nominal sensitivity of 50 fC for the auto-trigger should be reached. On the high end, the maximum signal of 50 pC will be reached by decreasing the gain in the slow shaper to allow it to saturate later[94]. The dynamic range will also be extended by using a bi-gain readout as necessitated by the reduction of dead-time and the use of 8 to 10 bit configuration[95].

The conversion time is presently 100 µs in the 12 bit configuration. With an analog memory depth of 2 and a random particle arrival on the 16 PMTs, a dead-time of 10% has been calculated. By reducing the ADC resolution to 8 bits but using two gains in a ratio of 10, the dynamic range is conserved[96] while the conversion time is reduced by a factor of 16 to 6 µs. The readout rate needs also be increased from 10 to 40 MHz and in that case, the dead-time becomes 0.1?%.

---

[94] Presently, the ADC saturates for 10 pC (50 p.e.) but the noise is 25 ADC counts, which is very good for precise noise studies but useless for the dynamic range.

[95] With a 10bit ADC, a full scale of 50 pC (300 p.e.) gives a LSB of 50 fC which corresponds to the auto-trigger threshold. In the baseline dual-gain 8bit configuration, the LSB is 1 p.e. in the low gain and 0.1 p.e. in the high gain

[96] For Čerenkov applications, the interesting region is the few photoelectrons.

The measurement with the time to amplitude converter (TAC) suffers from a dead region of 30 ns where the two ramps are swapped. By storing each ramp on two separate capacitors and allowing an overlap of the good regions, the time accuracy can be brought down to 100 ps according to simulations performed by the IPNO group.

5. Conclusion on PMT readout

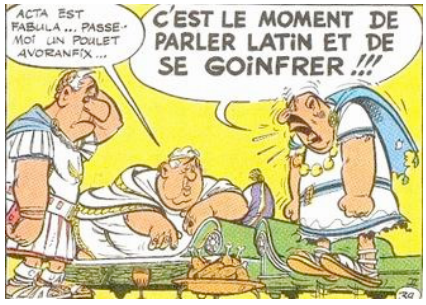
The family of OPERA_ROC, MAROC and PARISROC covers a wide range of applications, from particle physics experiments to medical imaging and is being used by many external groups[97]. They represent the trend towards increased granularity and "smart sensors" with integrated readout electronics. The next generation of photodetectors will thus deliver only bits, with charge, time and position information.

∞

[97] MAROC is used by Double Chooz (Nevis USA), Menphyno (APC), PET imaging Insituto Superiore de Sanita (Roma IT), PET/MRI (Pisa IT) and (Valencia SP)
PARISROC is studied by DUSEL (Univ. Wisonsin USA), LENA (Muncih D)

CONCLUSION

"acta est fabula[98]"



In the light of these different huge international projects, as much in the aspects of realizations than in those of coordination, I have constantly noticed the importance of instrumentation in the overall performance. As shown in this document, it covers a large span, from detector modelization to readout architecture, often finely entangled with detector design and optimization. Therefore, the close collaboration between physics groups and strong instrumentation groups is a key to the success of these designs.

Now, as was shown in the two last chapters of this document, the readout electronics is more and more integrated inside complex ASICs, which include simultaneously more channels and more functionalities. What used to be assembly of commercial components (opamps, ADCs…) is now integrated in the front-end chip and also moved onto (or inside) the detector. Concomitantly, the microelectronics technologies have been changing steadily (Figure 192), getting smaller and smaller and being more and more complex.

This has changed (or is changing) the way chips are being designed, pushing for a more "industrial" organization compared to the traditional handcraft workshop. It is now essential to have strong teams with critical mass of skilled engineers with fluid communication in order to make optimum reuse of tested building blocks from various projects. This has been tried in Orsay, with the creation of OMEGA, standing for Orsay Micro-Electronics Groups Associated by IN2P3 in October 2007. It aims at concentrating a dozen of micro-electronics engineers to service the projects of the 4 laboratories on the Orsay site[99] (see annex 2).

The large family of complex chips ("ROC" chips) which have been developed (Figure 193) in just a few years and are described in the last two chapters of this document shows the validity of the concept.

∞

[98] « La pièce est finie » (et non pas « cet acteur est fabuleux »)

[99] Laboratoire de l'Accélérateurs Linéaire (LAL), Institut de Physique Nucléaire (IPNO), Centre de Spectroscopie Nucléaire et Spectroscopie de Masse (CSNSM) et Laboratoire Leprince-Ringuet (LLR)

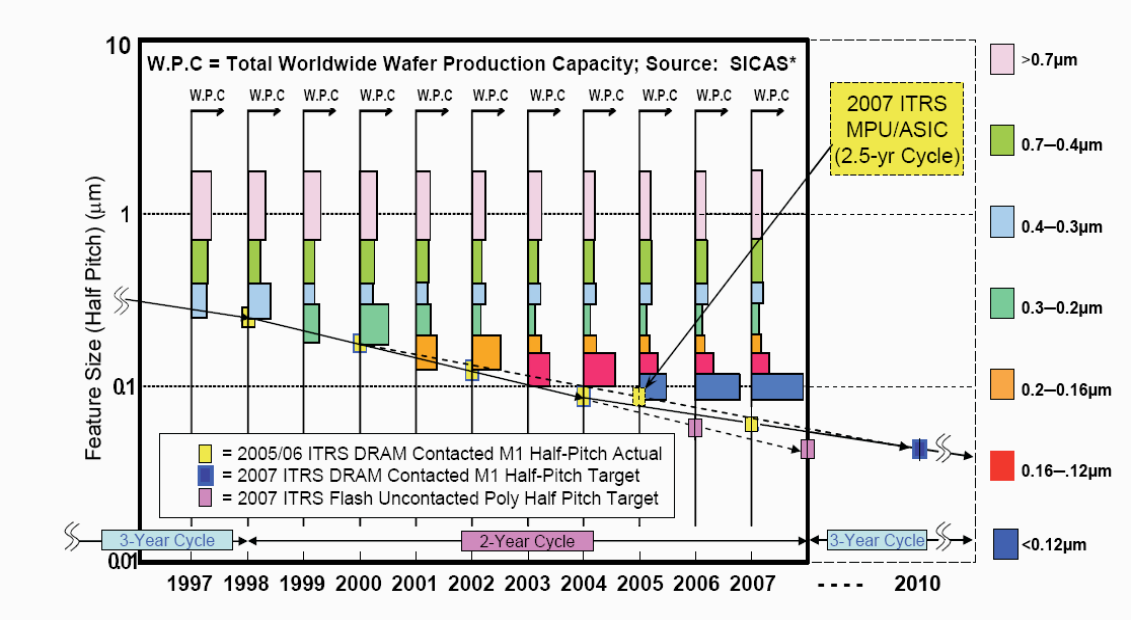


Figure 192 : Roadmap of Semiconductor industry

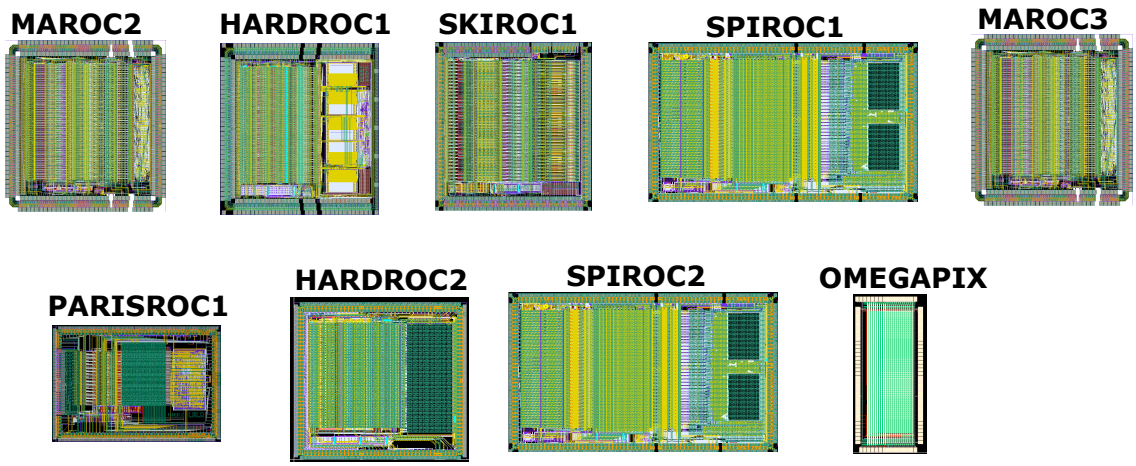


Figure 193: Family of ROC chips realized in 2006-2009 to read out various particule physics detectors (PMTs, Si, RPCs, SiPM…)

REFERENCES

Main publications used to elaborate this document., mainly that I wrote or co-wrote. The external publications are in reference inside these publications, except for the salient ones quoted directly, cited in here in blue.

[1] ATLAS Technical Design Report. CERN/LHCC/96-41. (1996)

[2] F. Gianotti et al. : "Liquid argon calorimetry with LHC performance specifications". *Nucl Instr and Meth.* **A315** (1992) 285-293

[3] B. Aubert et al. : "performance of liquid argon accordion calorimeter with fast readout". *Nucl Instr and Meth.* **A321** (1992) 467-478

[4] V. Radeka, S. Rescia : "speed and noise limits in LAr calorimetry". *Nucl Instr and Meth* **A265** (1988) 228-242

[5] R.L. Chase, C. de La Taille, S. Rescia, N. Seguin : "Transmission line connections between detector and front end electronics in liquid argon calorimetry". *Nucl Instr and Meth* **A330** (1993) 228-242

[6] R.L Chase, C. de La Taille, N. Seguin-Moreau : « Experimental results on cable-coupled preamplifiers (ØT)". *Nucl Instr and Meth* **A343** (1994) 598-605

[7] W.E. Cleland, E.G. Stern : "Signal processing considerations for liquide ionization calorimeters in high rate environment" *Nucl Instr and Meth* **A338**(1994) 467-497

[8] Y. Jacquier : PhD thesis : "Préamplificateur de courant bas-bruit pour le calorimètre électromagnétique d'ATLAS" LAL-97-56

[9] C. de La Taille : "New noise figures for the ATLAS e.m. calorimeter" ATLAS internal note ATL-LARG-96-045 (1996)

[10] R.L Chase, C. de La Taille, J.P. Richer, N. Seguin-Moreau : "a fast monolithic shaper for the ATLAS e.m. calorimeter". ATLAS internal note ATL-LARG-95-010 (1995)

[11] J. Collot et al. "The LAr Tri-gain shaper" ATLAS internal note ATL-LARG-98-092 (1998)

[12] Y. Jacquier, C. de La Taille, L. Serin : "Strengths and weaknesses of digital filtering" ATLAS internal note ATL-LARG-97-080 (1997)

[13] W. Bonivento, E. collet, P. Imbert, C. de La Taillle : "radiation hard micro-coaxial cables for the ATLAS liquid argon calorimeter". *Nucl Instr and Meth* **A451** (2000) 492-505

[14] J. colas et al. "Electronics calibration boards for the ATLAS liquid argon calorimeters" *Nucl Instr and Meth* **A593** (2008) 269-291

[15] J. Colas et al. : "crosstalk in the ATLAS electromagnetic calorimeter". ATLAS Internal note ATL-LARG-2000-004

[16] B. Aubert et al : "development and construction of large size signal electrodes for the ATLAS electromagnetic calorimeter". *Nucl Instr and Meth* **A539** (2005) 558-594

[17] Y. Jacquier, C. de La Taille, B. Mansoulié, J. Schwindling : « Signal and noise crosstalk on calorimeter strips and effect on π^0 rejection". ATLAS internal note ATL-LARG-95-031 (1995)

[18] J. Brau et al. : "ILC reference design report" FERMILAB APC (2007) **arXiv :0707-1245**

[19] CALICE collaboration : http://wiki.cern.ch/twiki/bin/view/CALICE/WebHome

[20] EUDET collaboration : http://eudet.org

[21] J. Fleury et al. : "Front-End ASICs development for W-Si calorimeter at ILC" *Nucl Instr and Meth* **A572** (2006) 371-375
[22] P. Barrillon et al. "Integrated Electronics for SiPM and MPPC" PoS PD07:025 (2006)
[23] T. Adam et al. "The OPERA experiment target tracker" *Nucl Instrum Meth* **A577** (2007) 523-539
[24] S. Bondil et al. "A front-end readout chip for the OPERA scintillator tracker" *Nucl Instr and Meth* **A521** (2004) 378-392
[25] S. Ask et al. : "Luminosity measurement at ATLAS: Development, construction and test of scintillating fibre prototype detectors" *Nucl Instrum Meth* **A568** (2006) 568-588
[26] C. Marmonier (Photonis) NNN05
[27] S. Conforti et al. : "PARISROC : Photomultiplier ARray Integrated Sige Read-Out Chip" *Nucl Instr and Meth* paper in preparation

ANNEX 1

Publications au 31 dec 2008

1. **Design and implementation of the Front End Board for the readout of the ATLAS liquid argon calorimeters.** N.J. Buchanan *et al.* 2008.
   Published in **JINST 3:P03004,2008**.

2. **Construction, assembly and tests of the ATLAS electromagnetic end-cap calorimeters.** By ATLAS Collaboration (M. Aleksa *et al.*). 2008.
   Published in **JINST 3:P06002,2008**.

3. **The ATLAS Experiment at the CERN Large Hadron Collider.**
   By ATLAS Collaboration (G. Aad *et al.*). 2008. 437pp.
   Published in **JINST 3:S08003,2008**.

4. **Electronics calibration board for the ATLAS liquid argon calorimeters.**
   J. Colas *et al.* 2008. 23pp.
   Published in **Nucl.Instrum.Meth.A593:269-291,2008**.

5. **ILC Reference Design Report Volume 4 - Detectors.**
   By ILC Collaboration (Ties Behnke, (Ed.) *et al.*). FERMILAB-APC, Dec 2007.
   e-Print: **arXiv:0712.2356** [physics.ins-det]

6. 6) **HARDROC, HAdronic Rpc Detector ReadOut Chip.**
   Christophe de la Taille (Orsay, LAL) . Sep 2007.
   Published in *Prague 2007, Electronics for particle physics* 30

7. **ILC Reference Design Report: ILC Global Design Effort and World Wide Study.**By ILC Collaboration (James Brau, (Ed.) *et al.*). FERMILAB-APC, Aug 2007. 147pp.
   e-Print: **arXiv:0712.1950** [physics.acc-ph]

8. **CALICE Report to the Calorimeter R&D Review Panel.**
   By CALICE Collaboration (C. Adloff *et al.*). ILC-DET-2007-024, Jul 2007. 77pp.
   e-Print: **arXiv:0707.1245** [physics.ins-det]

9. **Hadron beam test of a scintillating fibre tracker system for elastic scattering and luminosity measurement in ATLAS.**
   F. Anghinolfi *et al.* Jun 2007. 12pp.
   Published in **JINST 2:P07004,2007**.
   e-Print: **arXiv:0706.3316** [physics.ins-det]

10. **The Beam and detector for the NA48 neutral kaon CP violations experiment at CERN.**
    By NA48 Collaboration (V. Fanti *et al.*). May 2007. 40pp.
    Published in **Nucl.Instrum.Meth.A574:433-471,2007**.

11. **The OPERA experiment target tracker.**
T. Adam *et al.* Jan 2007. 25pp.
Published in **Nucl.Instrum.Meth.A577:523-539,2007**.
e-Print: **physics/0701153**

12. **Front-end ASICs development for W-Si calorimeter at ILC.**
By CALICE Collaboration (Julien Fleury *et al.*). 2007. 5pp.
Prepared for 10th Pisa Meeting on Advanced Detectors: Frontier Detectors for Frontier Physics, La Biodola, Elba, Italy, 21-27 May 2006.
Published in **Nucl.Instrum.Meth.A572:371-375,2007**.

13. **First events from the CNGS neutrino beam detected in the OPERA experiment.** By OPERA Collaboration (R. Acquafredda *et al.*). Nov 2006. 12pp.
Published in **New J.Phys.8:303,2006**.
e-Print: **hep-ex/0611023**

14. **Luminosity measurement at ATLAS: Development, construction and test of scintillating fibre prototype detectors.** S. Ask *et al.* May 2006. 16pp.
Published in **Nucl.Instrum.Meth.A568:588-600,2006**.
e-Print: **physics/0605127**

15. **A large dynamic range integrated front-end for photomultiplier tubes.**
B. Genolini, L. Raux, C. de la Taille, J. Pouthas, V. Tocut (Orsay, IPN & Orsay, LAL) . 2006. 5pp.
Prepared for 4th International Conference on New Developments in Photodetection (BEAUNE 2005): From Infra Red to Gamma Rays, Beaune, France, 19-24 Jun 2005.
Published in **Nucl.Instrum.Meth.A567:209-213,2006**.

16. **Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout.**
S. Blin *et al.* LC-DET-2006-007, 2006. 12pp.

17. **Integrated electronic for SIPM and MPPC.**
Pierre Barrillon, Sylvie Blin, Frederic Dulucq, Julien Fleury, Gisele Martin, Ludovic Raux, Nathalie Seguin, Christophe de la Taille (Orsay, LAL) . 2006. 19pp. Published in **PoS PD07:025,2006**.

18. **The Upgraded D0 detector.**
By D0 Collaboration (V.M. Abazov *et al.*). FERMILAB-PUB-05-341-E, Jul 2005. 142pp.
Published in **Nucl.Instrum.Meth.A565:463-537,2006**.
e-Print: **physics/0507191**

19. **Construction, assembly and tests of the ATLAS electromagnetic barrel calorimeter.**
By ATLAS Electromagnetic Barrel Liquid Argon Calorimeter Group (B. Aubert *et al.*). CERN-PH-EP-2005-034, Jul 2005. 77pp.
Published in **Nucl.Instrum.Meth.A558:388-418,2006**.

20. **Position resolution and particle identification with the ATLAS EM calorimeter.** By ATLAS Liquid Argon Calorimeter Collaboration (J. Colas *et al.*). May 2005. 32pp.
Published in **Nucl.Instrum.Meth.A550:96-115,2005**.
e-Print: **physics/0505127**

21. **Front-end Electronic for the Calice ECAL Physics Prototype.**
Julien Fleury, Christophe de la Taille, Gisele Martin-Chassard (Orsay, LAL) . LCWS-2005-0902, Mar 2005.
In the Proceedings of 2005 International Linear Collider Workshop (LCWS 2005), Stanford, California, 18-22 Mar 2005.
In the Proceedings of 2005 International Linear Collider Workshop (LCWS 2005), Stanford, California, 18-22 Mar 2005, pp 0902.

22. **FLC_SIPM: Front-End Chip for SIPM Readout for ILC Analog HCAL.**
C. de la Taille, Gisele Martin-Chassard, L. Raux (Orsay, LAL) . LCWS-2005-0916, Mar 2005.

In the Proceedings of 2005 International Linear Collider Workshop (LCWS 2005), Stanford, California, 18-22 Mar 2005.
In the Proceedings of 2005 International Linear Collider Workshop (LCWS 2005), Stanford, California, 18-22 Mar 2005, pp 0916.

23. **Dedicated front-end electronics for the next generation of linear collider electromagnetic calorimeter.**
By the FLC Collaboration Proxy and FLC Collaboration (S. Manen *et al.*). Jan 2005. 3pp.
Contributed to 10th Workshop on Electronics for LHC and Future Experiments, Boston, Massachusetts, 13-17 Sep 2004.
e-Print: **physics/0501063**

24. **Development and construction of large size signal electrodes for the ATLAS electromagnetic calorimeter.**
B. Aubert *et al.* CERN-PH-EP-2004-019, May 2004. 43pp.
Published in **Nucl.Instrum.Meth.A539:558-594,2005**.

25. **Introducing FLC_PHY3 low noise front-end chip for FLC W-Si electromagnetic calorimeter physics prototype.**
Julien Fleury, Christophe de la Taille, Gisele Martin-Chassard (Orsay, LAL & Orsay) . Apr 2004. 9pp.
Prepared for International Conference on Linear Colliders (LCWS 04), Paris, France, 19-24 Apr 2004.
Published in *Paris 2004, Linear colliders* 819-827

26. **Extended joint ECFA/DESY study on physics and detector for a linear e+ e- collider. Proceedings, Summer Colloquium, Amsterdam, Netherlands, April 4, 2003.**
K. Ackermann *et al.* DESY-PROC-2004-01, DESY-04-123, DESY-04-123G, Mar 2004. 140pp.
Prepared for 4th ECFA / DESY Workshop on Physics and Detectors for a 90-GeV to 800-GeV Linear e+ e- Collider, Amsterdam, The Netherlands, 1-4 Apr 2003.

27. **Performance of the Liquid Argon final calibration board.**
C. de la Taille, N. Seguin-Moreau, L. Serin (Orsay, LAL) , N. Dumont-Dayot, I. Wingerter-Seez (Annecy, LAPP) . Mar 2004. 8pp.
Prepared for 11th International Conference on Calorimetry in High-Energy Physics (Calor 2004), Perugia, Italy, 28 Mar - 2 Apr 2004.
Published in *Perugia 2004, Calorimetry in particle physics* 143-150

28. **Performance of a low noise readout ASIC for the W-Si calorimeter physics prototype for the future linear collider.**
J. Fleury, C. de la Taille, G. Martin-Chassard (Orsay, LAL) . Mar 2004. 5pp.
Prepared for 11th International Conference on Calorimetry in High-Energy Physics (Calor 2004), Perugia, Italy, 28 Mar - 2 Apr 2004.
Published in *Perugia 2004, Calorimetry in particle physics* 191-195

29. **A front-end read out chip for the OPERA scintillator tracker.**
A. Lucotte, S. Bondil, K. Borer, J.E. Campagne, A. Cazes, M. Hess, C. de La Taille, G. Martin-Chassard, L. Raux, J.P. Repellin (Orsay, LAL & Bern U.) . 2004. 15pp.
Published in **Nucl.Instrum.Meth.A521:378-392,2004**.

30. **An adaptable fast and compact DAQ for the luminosity measurement at HERA II.**
V. Boudry, F. Moreau, A.E. Specka (Ecole Polytechnique) , R. Chiche, C. de la Taille (Orsay) , P. Bailly, E. Barrelet, H. Lebbolo, A. Vallereau (Paris U., VI-VII) , C. Renard (SUBATECH, Nantes) . 2004. 5pp.
Prepared for 13th IEEE - NPSS Real Time Conference (RT 2003), Montreal, Canada, 18-23 May 2003.
Published in **IEEE Trans.Nucl.Sci.51:425-429,2004**.

31. **Performance of the ATLAS electromagnetic calorimeter barrel module 0.**
By ATLAS Electromagnetic Liquid Argon Calorimeter Group (B. Aubert *et al.*). CERN-EP-2002-087, Nov 2002. 48pp.
Published in **Nucl.Instrum.Meth.A500:202-231,2003, Erratum-ibid.A517:399-402,2004**.

32. **Performance of the ATLAS electromagnetic calorimeter end-cap module 0.** By The ATLAS Electromagnetic Liquid Argon Calorimeter Group (B. Aubert *et al.*). CERN-EP-2002-104, Nov 2002. 31pp.
Published in **Nucl.Instrum.Meth.A500:178-201,2003**.

33. **Calibration boards for the ATLAS LAr calorimeters.**
N. Dumont-Dayot *et al.* Sep 2002.
Prepared for 8th Workshop on Electronics for LHC Experiments, Colmar, France, 9-13 Sep 2002.
Published in *Colmar 2002, Electronics for LHC experiments* 347-352

34. **Front end electronics for a silicon tungsten calorimeter.**
S. Manen, G. Bohner, J. Lecoq (Clermont-Ferrand U.) , J. Fleury, C. de la Taille, G. Martin (Orsay, LAL) . Aug 2002. 4pp.
Prepared for International Workshop on Linear Colliders (LCWS 2002), Jeju Island, Korea, 26-30 Aug 2002.
Published in *Seogwipo 2002, Linear colliders* 577-580

35. **The electronics of the new H1 luminosity system.**
V. Boudry, F. Moreau, A.E. Specka, C. Renard (Ecole Polytechnique) , E. Barrelet, P. Bailly, H. Lebbolo, A. Vallereau (Paris U., VI-VII) , R. Chiche, C. de la Taille (Orsay, LAL) . Mar 2002. 6pp.
Prepared for 10th International Conference on Calorimetry in High Energy Physics (CALOR 2002), Pasadena, California, 25-30 Mar 2002.
Published in *Pasadena 2002, Calorimetry in particle physics* 652-657

36. **Status of ATLAS LAr DMILL chips.**
C. de la Taille (Orsay, LAL) . Sep 2001.
Prepared for 7th Workshop on Electronics for LHC Experiments, Stockholm, Sweden, 10-14 Sep 2001.
Published in *Stockholm 2001, Electronics for LHC experiments* 289-294

37. **Hadron energy reconstruction for the ATLAS calorimetry in the framework of the nonparametrical method.**
By ATLAS Collaboration (S. Akhmadalev *et al.*). Apr 2001. 33pp.
Published in **Nucl.Instrum.Meth.A480:508-523,2002**.
e-Print: **hep-ex/0104002**

38. **Silicon diode, readout and front end electronics of the proposed w-si ecal.**
A. Karar, Ch. de la Taille . LC-DET-2001-059, Feb 2001.
In *2nd ECFA/DESY Study 1998-2001* 2286-2297.

39. **Overview of ATLAS LAr radiation tolerance.**
C. de la Taille (Orsay, LAL) . Sep 2000.
Prepared for 6th Workshop on Electronic for LHC Experiments, Cracow, Poland, 11-15 Sep 2000.
Published in *Cracow 2000, Electronics for LHC experiments* 265-269

40. **Results from a new combined test of an electromagnetic liquid argon calorimeter with a hadronic scintillating-tile calorimeter.**
By ATLAS Collaboration (S. Akhmadalev *et al.*). Jul 2000. 17pp.
Published in **Nucl.Instrum.Meth.A449:461-477,2000**.

41. **Front end electronics in fast calorimetry.** C. de la Taille (Orsay, LAL) . LAL-RT-00-03, May 2000. 11pp.
Hardcopy at DESY.
Prepared for 8th International Conference on Calorimetry in High-Energy Physics (CALOR 99), Lisbon, Portugal, 13-19 Jun 1999.
Published in *Lissabon 1999, Calorimetry in high energy physics* 557-569

42. **The NA48 LKr calorimeter readout electronics.**
By NA48 Collaboration (A. Gianoli *et al.*). 2000.
Prepared for 11th IEEE NPSS Real Time Conference (Santa Fe 99), Santa Fe, New Mexico, 14-18 Jun 1999.
Published in **IEEE Trans.Nucl.Sci.47:136-141,2000**.

43. **Radiation hard micro-coaxial cables for the ATLAS liquid argon calorimeters.**
W. Bonivento, E. Collet, P. Imbert, C. de la Taille (Orsay, LAL & Orsay) . 2000.
Published in **Nucl.Instrum.Meth.A451:492-505,2000**.

44. **The ATLAS calorimeter calibration board: Test of a first set of boards new developments.**
J. Colas, N. Dumont-Dayot, M. Moynot, P. Perrodo, G. Perrot, I. Wingerter-Seez (Annecy, LAPP) , C. de La Taille, G. Martin-Chassard, N. Seguin-Moreau, L. Serin (Orsay, LAL & Orsay) . 1999.
Prepared for 5th Workshop on Electronics for the LHC Experiments (LEB 99), Snowmass, Colorado, 20-24 Sep 1999.
In *Snowmass 1999, Electronics for LHC experiments* 265-269.

45. **An automated test bench for the ATLAS shapers and SCAs.**
J.P. Richer, C. de la Taille, R. Bernier, D. Breton (Orsay, LAL) , A. Patti, D. Dzahini, J. Collot (LPSC, Grenoble) , E. Delagnes (DAPNIA, Saclay) . 1999.
Prepared for 5th Workshop on Electronics for the LHC Experiments (LEB 99), Snowmass, Colorado, 20-24 Sep 1999.
In *Snowmass 1999, Electronics for LHC experiments* 561-563.

46. **Performance of the ATLAS LAr calibration board.**
J. Colas, M. Moynot, P. Perrodo, G. Perrot, I. Wingerter-Seez (Annecy, LAPP) , J.P. Coulon, C. de La Taille, G. Martin-Chassard, N. Seguin-Moreau, L. Serin (Orsay, LAL & Orsay) . 1998.
Given at 4th Workshop on Electronics for LHC Experiments (LEB 98), Rome, Italy, 21-25 Sep 1998.
In *Rome 1998, Electronics for LHC experiments* 213-217.

47. **A Low noise transceiver for the NA48 liquid krypton calorimeter.**
C. de la Taille, G. Martin-Chassard, N. Seguin-Moreau (Orsay, LAL) . LAL-RT-97-05, Dec 1997. 14pp.
Prepared for 6th International Conference on Calorimetry in High-energy Physics (ICCHEP 96), Rome, Italy, 8-14 Jun 1996.
Published in *Frascati 1996, Calorimetry in high energy physics* 799-805

48. **Test beam results of a stereo preshower integrated in the liquid argon accordion calorimeter.**By RD3 Collaboration (R.A. Davis *et al.*). CERN-PPE-97-133, Aug 1997. 35pp.
Published in **Nucl.Instrum.Meth.A411:313-329,1998**.

49. **Overview of the front end electronics for the ATLAS LAr calorimeter.**
By ATLAS LArG Collaboration (C. de la Taille *for the collaboration*). 1997.
Given at 3rd Workshop on Electronics for LHC Experiments, London, England, 22-26 Sep 1997.
In *London 1997, Electronics for LHC experiments* 186-191.

50. **ATLAS computing technical proposal.**
By ATLAS Collaboration (A. Airapetian *et al.*). CERN-LHCC-96-43, Dec 1996. 100pp.

51. **ATLAS calorimeter performance Technical Design Report.**
By ATLAS Collaboration (A. Airapetian *et al.*). CERN-LHCC-96-40, Dec 1996. 189pp.

52. **Results from a combined test of an electromagnetic liquid argon calorimeter with a hadronic scintillating tile calorimeter.**
By ATLAS Collaboration (Z. Ajaltouni *et al.*). CERN-PPE-96-178, Nov 1996. 28pp.
Published in **Nucl.Instrum.Meth.A387:333-351,1997**.

53. **Performance of an endcap prototype of the ATLAS accordion electromagnetic calorimeter.**
By RD3 Collaboration (D.M. Gingrich *et al.*). CERN-PPE-96-175, Oct 1996. 26pp.
Published in **Nucl.Instrum.Meth.A389:398-408,1997**.

54. **Construction and test of a fine grained liquid argon preshower prototype.**
By RD3 Collaboration (R.A. Davis *et al.*). CERN-PPE-96-123, Jul 1996. 19pp.
Published in **Nucl.Instrum.Meth.A385:47-57,1997**.

55. **A quad-gain monolithic shaper for fast LAr calorimetry.**
R.L. Chase, C. de La Taille, G. Martin-Chassard, J.P. Richer, N. Seguin-Moreau (Orsay, LAL & Orsay) . 1996.
Given at 2nd Workshop on Electronics for LHC Experiments, Balatonfured, Hungary, 23-27 Sep 1996.
In *Balatonfuered 1996, Electronics for LHC experiments* 66-69.

56. **Performance of a large scale prototype of the ATLAS accordion electromagnetic calorimeter.**
By RD3 Collaboration (D.M. Gingrich *et al.*). CERN-PPE-95-035, CERN-PPE-95-35, Mar 1995. 39pp.
Published in **Nucl.Instrum.Meth.A364:290-306,1995**.

57. 57) **A Fast monolithic shaper for the atlas E.M. calorimeter.**
R.L. Chase, C. de la Taille, J.P. Richer, N. Seguin-Moreau (Orsay, LAL) . LAL-RT-95-04, LARG-10-1995, Mar 1995. 28pp.
Presented at 5th International Conference on Calorimetry in High Energy Physics, Upton, NY, 25 Sep - 1 Oct 1994.
Published in Calorimetry in HEP 1994:0410-418 (QCD201:I38:1994)

58. **ATLAS: Technical proposal for a general-purpose p p experiment at the Large Hadron Collider at CERN.**
By ATLAS Collaboration (W.W. Armstrong *et al.*). CERN-LHCC-94-43, Dec 1994. 289pp.

59. **Performance of a liquid argon accordion hadronic calorimeter prototype.**
By RD3 Collaboration (D.M. Gingrich *et al.*). CERN-PPE-94-127, Aug 1994. 43pp.
Published in **Nucl.Instrum.Meth.A355:295-307,1995**.

60. 60) **RD-3: Status report.**
D.M. Gingrich *et al.* CERN-DRDC-94-18, May 1994. 31pp.

61. **Performance of the liquid argon electromagnetic and hadronic accordion calorimeter for the LHC.**
A. Cravero *et al.* 1994.
Published in **Nucl.Instrum.Meth.A344:39-46,1994**.

62. **Transmission line connections between detector and front end electronics in liquid argon calorimetry.**
R.L. Chase, C. de La Taille, N. Seguin (Orsay, LAL) , S. Rescia (Brookhaven) . 1993.
Published in **Nucl.Instrum.Meth.A330:228-242,1993**.

63. **Performance of cable-coupled preamplifiers (0T).**
R.L. Chase, C. de la Taille, N. Seguin-Moreau (Orsay, LAL & Orsay) . 1993.
Given at 4th International Conference on Calorimetry in High-energy Physics, La Biodola, Italy, 19-25 Sep 1993.
In *La Biodola 1993, Calorimetry in high energy physics* 148-153.

64. **Performance of a liquid argon preshower detector integrated with an accordion calorimeter.**
By RD3 Collaboration (B. Aubert *et al.*). CERN-PPE-92-206, Nov 1992. 28pp.
Published in **Nucl.Instrum.Meth.A330:405-415,1993**.

65. **Automated system for equivalent noise charge measurements from 10-ns to 10-microseconds.**
C. de La Taille (Orsay, LAL) . LAL-RT-92-10, Jul 1992. 11pp.
Presented at 3rd Int. Conf. on Advanced Technology and Particle Physics, Como, Italy, Jun 22-26, 1992.
Published in **Nucl.Phys.Proc.Suppl.32:449-459,1993**.

66. **Performance of a liquid argon electromagnetic calorimeter with a cylindrical accordion geometry.**
B. Aubert *et al.* CERN-PPE-92-129, Jul 1992. 29pp.
Published in **Nucl.Instrum.Meth.A325:116-128,1993**.

67. **Performance of a liquid argon accordion calorimeter with fast readout.**
B. Aubert *et al.* CERN-PPE-92-046, Feb 1992. 29pp.
Published in **Nucl.Instrum.Meth.A321:467-478,1992**.

68. **Liquid argon calorimetry with LHC performance specifications.**
F. Gianotti *et al.* 1992.
Published in **Nucl.Instrum.Meth.A315:285-293,1992**.

69. **Low-energy calorimetry in a multiwire chamber filled with tetramethylsilane.**
B. Degrange, J. Guillon, F. Moreau, U. Nguyen-Khac, C. de la Taille, S. Tisserant, M. Verderi (Ecole Polytechnique) . 1991.
Published in **Nucl.Instrum.Meth.A311:539-547,1992**.

70. **Calibration of liquid argon calorimeters at high luminosity.**
R.L. Chase, C. de la Taille, N. Seguin (Orsay, LAL) , L. Rogers (Brookhaven) . 1991.
Prepared for 2nd International Conference on Calorimetry in High-energy Physics, Capri, Italy, 14-18 Oct 1991.
In *Capri 1991, Calorimetry in high energy physics* 442-444.

71. **Liquid argon calorimetry with LHC performance specifications. R & D proposal.**
D. Fournier *et al.* Oct 1990.
Prepared for ECFA Large Hadron Collider (LHC) Workshop: Physics and Instrumentation, Aachen, Germany, 4-9 Oct 1990.
Published in *Aachen 1990, Large Hadron Collider, vol. 3* 368-369

ANNEX2

OMEGA CONSTITUTION

Convention pôle microélectronique. Version 4 1/3/2007

Création d'un pôle de micro-électronique pour la région parisienne, basé au LAL Orsay

1. **Préambule**

   La complexité croissante des circuits intégrés utilisés dans les expériences de physique de l'IN2P3 et les moyens nécessaires à leur développement nécessitent désormais des groupes dont **la taille critique d'une dizaine de personnes** permet de mener à bien ces développements. Par ailleurs, de nombreux sous-circuits sont régulièrement réutilisés d'une expérience à l'autre, rendant essentielle une communication fluide entre les concepteurs qui est assurée par une **proximité géographique** et les contacts quotidiens. Ceci permet le partage d'expérience, les « réunions de design » et les revues internes, nécessaires au succès de circuits coûteux. Au niveau national, plusieurs pôles (typiquement 4) pourraient être créés autour de laboratoires possédant déjà des équipes nombreuses, les laboratoires disposant d'équipes plus réduites étant alors **associés** à ces pôles.

2. **Définition d'un pôle de microélectronique**

   2.1. **Eléments consititutifs :** un pôle de microélectronique est un ensemble d'ingénieurs électroniciens affectés fonctionnellement à ce pôle et hébergés dans un laboratoire hôte.

   2.2. **Mission :** le pôle conçoit et réalise des circuits de microélectronique nécessaires aux expériences de physique des laboratoires utilisateurs.

   2.3. **Direction** : le pôle est dirigé par un directeur de pôle. Une structure de gouvernance permet de s'assurer du bon fonctionnement du pôle.

   2.4. **Moyens :** le pôle reçoit de la part de l'IN2P3 ses moyens humains et financiers sur une ligne (indépendante) identifiée. Ceux-ci s'inscrivent dans un plan d'objectifs pluriannuel

glissant couvrant les moyens du pôle, ceux du laboratoire hôte et les moyens d'interface répartis dans les laboratoires utilisateurs.

2.5. **Durée** : le pôle est créé pour une durée de 5ans renouvelable

2.6. **Valorisation** : la valorisation ne rentre pas dans les attributions du pôle car les logiciels ne sont pas utilisables contractuellement, elle doit donc être traitée par le C4I. Les ingénieurs du pôle ont la liberté de valoriser leurs designs avec le C4I, après accord du labo ou du pôle.

3. Laboratoires associés (ou partenaires)

3.1. **définition** : les laboratoires associés sont définis par notion de proximité géographique et/ou par leur investissement de ressources dans le pôle.

3.2. **mise en oeuvre** : les laboratoires associés sont définis et révisables par le conseil d'administration.

4. Laboratoires hôte

4.1. **Infrastructure** : le laboratoire hôte doit assurer au pôle l'infrastructure nécessaire à son bon fonctionnement : bureaux, matériel électronique et informatique, licences, etc.. avec une identification précise, permettant l'évaluation des coûts consolidés

4.2. **Services** : le laboratoire hôte doit assurer au pôle l'accès aux différents services dont le pôle a besoin : achats, administration etc.. Ces accès seront arbitrés en toute transparence dans les instances du laboratoire hôte, dont le directeur du pôle sera membre ou pourra se faire représenter par une personne de son choix.

4.3. **Personnel affecté** : le personnel recruté pour le compte du pôle est rattaché administrativement au laboratoire hôte. Le laboratoire hôte est responsable de la gestion [et la promotion de ces personnels et s'engage à veiller à l'équité de leur traitement].

4.4. **Accueil de personnel extérieur** : le laboratoire hôte accueillera aussi des ingénieurs d'autres laboratoires qui seront missionnés au pôle pour une durée déterminée et seront alors placés sous l'autorité fonctionnelle du directeur du pôle.

4.5. **Budget** : le laboratoire hôte recevra de la part de l'IN2P3 (ou du budget du pôle) une dotation spécifique pour l'hébergement du pôle.

4.6. **Prérogatives** : lorsque le laboratoire hôte est aussi un laboratoire utilisateur, ses droits et devoirs en tant que laboratoire utilisateur sont identiques à ceux des autres laboratoires.

5. Laboratoires (ou projets) utilisateurs et fonctionnement

5.1. **Soumission des demandes** : les laboratoires utilisateurs soumettent pour le compte de leurs projets des circuits microélectroniques pour études ou réalisations au pôle. Ces demandes seront recueillies et classées par le comité des projets, chargé de définir le programme de travail du pôle.

5.2. **Interface** : le laboratoire utilisateur doit identifier un ingénieur électronicien (mais absolument pas nécessairement microélectronicien) chargé de l'interface avec le pôle, pour les différentes phases du projet (spécifications, tests, mesures). Réciproquement, au moins un ingénieur du pôle est affecté au projet et participe pleinement à la collaboration scientifique ou au projet, dont il est est alors signataire.

5.3. **Responsabilité** : le laboratoire utilisateur est responsable de la mesure des circuits fournis et de leur intégration dans le reste de l'électronique.

5.4. **Représentations :** les laboratoires utilisateurs sont représentés dans l'assemblée annuelle des utilisateurs du pôle.

5.5. **Propriété intellectuelle :** les circuits développés par le pôle restent la propriété intellectuelle du pôle et peuvent resservir à d'autres expériences de physique de l'IN2P3. Par contre, leur utilisation à des fins de valorisation ne pourra se faire sans l'accord du physicien responsable du projet. Réciproquement, l'utilisation des circuits par le laboratoire utilisateur pour d'autres expériences ou pour la valorisation ne pourra se faire sans l'accord du directeur du pôle.

5.6. **Publications :** les publications présentant le design et les performances des circuits seront impérativement visées et co-signées par les ingénieurs du pôle ayant participé au design.

6. Gouvernance

6.1. **Direction du pôle :** le pôle est dirigé par un directeur du pôle nommé pour 5 ans par le conseil d'administration du pôle. Il peut être assisté d'un directeur adjoint. Le directeur transmet à l'IN2P3, via le laboratoire hôte, les demandes en ressources humaines et financières du pôle. Il est responsable à ce titre de la politique de recrutement du pôle.

6.2. **Conseil d'administration :** ce comité est formé par les représentants des différentes entités fournissant des ressources au pôle : IN2P3, laboratoire hôte, laboratoires associés. Le directeur de l'IN2P3 est président de droit du conseil d'administration; il peut déléguer ce rôle. Le directeur du pôle est invité permanent. Le conseil d'administration se réunit au moins une fois par an.

- il nomme le directeur du pôle
- il reçoit le rapport d'activité du directeur du pôle
- il fixe les règles de travail et nomme les membres extérieurs du comité des projets
- il organise autant que de besoin des revues extérieures du pôle
- il reçoit le rapport de l'assemblée des utilisateurs
- il approuve et contrôle le budget annuel du pôle

6.3. Assemblée des utilisateurs : une fois par an, les utilisateurs et utilisateurs potentiels du pôle sont réunis pour recevoir le rapport d'activité du directeur du pôle. Elle inclut une session de discussion et questions ouvertes.

6.4. Constitution du conseil d'administration du pole d'Orsay (previsionnel)

- M. Spiro : Directeur de l'in2p3 (ex officio)
- P. Dargent : directeur technique de l'in2p3 (ex officio)
- G. Wormser : Directeur du laboratoire hôte (ex officio)
- D. Guillemaud-Muller : directrice de l'IPNO
- H. Videau : directeur du LLR
- G. Chardin : directeur du CSNSM
- L. Serin : physicien coordinateur de l'electronique LAL
- M. Winter : representant du pole de Strasbourg
- D. Linglin : directeur du C4I
- P. Rebourgeard representant du CEA

Résumé : ce rapport résume les développements réalisés en électronique pour lire le calorimètre à Argon Liquide (LAr) d'ATLAS au LHC puis le R&D effectué dans CALICE pour lire ceux de l'ILC en passant par les circuits développés pour lire les photomultiplicateurs multi-anode (MaPMT) pour OPERA ou pour la luminosité d'ATLAS et qui ont aussi des applications en imagerie médicale. Commencée au début des années 90, le R&D pour la calorimétrie d'ATLAS était extrêmement challenging en termes de vitesse de lecture, tenue aux radiations et précision de mesure. La vitesse élevée a nécessité une nouvelle approche de préamplificateurs de courant plutôt que de charge et la définition du bruit en ENI. Les préamplificateurs ont été développés a Orsay ainsi que les shapers monolithiques, ils sont détaillés dans le chapitre 1 ainsi que les considérations sur le filtrage numérique, qui constituait une nouveauté pour la communauté et qui ne donnait pas les résultas escomptés au début. Le chapitre 2 est consacré au système de calibration, développé et produit par Orsay et dont la performance poussée a nécessité des études approfondies. Le chapitre 3 clôt les études pour ATLAS avec un résumé des mesures qui ont dû être faites sur les 200 000 voies du détecteur pour le comprendre et le modéliser afin d'atteindre partout la précision et l'uniformité meilleures que le pourcent. Ces travaux pour ATLAS se sont achevés en 2004, même si des développements ont été réalisés pour les calorimètres de NA48 et D0 durant cette même période et sur des sujets connexes qui ne sont pas détaillés ici. La prochaine génération de collisionneurs après le LHC nécessitera une nouvelle génération de calorimètres, beaucoup plus granulaires (on parle d' « imaging calorimetry », avec des centaines de millions de canaux) et d'électronique de lecture intégrée dans le détecteur. Les ASICs développés pour cette application dans le cadre de la collaboration « CALICE » sont décrits au chapitre 4. Ils intègrent toutes les fonctions d'amplification, digitisation et lecture intégrée qui ont font de véritables « Systems On Chip » (SoC). Une famille de 3 circuits permet de lire le calorimètre électromagnétique Silicium-Tungstène, les RPCs du calorimètre hadronique digital ou les SiPM du calorimètre hadronique analogique ; très performants et versatiles, ils trouvent de nombreuses applications extérieures Ces circuits ont repris de précédents blocs de chips mis au point dans les années 2000 pour lire les photomultiplicateurs multi-anodes du Target Tracker de l'expérience OPERA puis du luminomètre de l'expérience ATLAS et qui sont décrits au chapitre 5 Ces circuits trouvent une continuation actuelle dans les photodétecteurs intégrés de grandes dimensions, développés pour de futures expériences Neutrino.

Abstract : this report summarizes the electronics developments for liquid argon calorimeter read-out at LHC and the R&D carried out in the framework of the CALICE collaboration for those of the future linear collider (ILC). It also includes chips designed for multi-anode photomultipliers (MaPMT) used in the OPERA experiment or on ATLAS luminometer, which also find applications in medical imaging. Started in the early 90's, the R&D for ATLAS calorimetry was extremely challenging in terms of readout speed, radiation tolerance and measurement accuracy. The high speed has required a new approach using current-sensitive preamplifiers instead of charge sensitive ones and the redefinition of noise performance in terms of ENI. The preamplifiers developed at Orsay and the monolithic shapers are described in Chapter 1, including considerations of digital filtering, which was a new technique in our field. Chapter 2 is dedicated to the calibration system, designed and built by Orsay, for which the high performance and accuracy necessitated in-depth studies. The 3rd chapter closes the studies for ATLAS with a summary of the detector measurements which had to be carried out on the 200 000 channels in order to understand and modelize the detector and achieve everywhere the accuracy and uniformity at per-cent level. These developments for ATLAS ended in 2004, although parallel work was also carried out for the NA48 and D0 calorimeters which are not detailed here. The next generation of collider will require a new generation of calorimeters, much more granular, referred to as "imaging calorimetry" with embedded read-out electronics. The ASICs developed for this purpose in the framework of the CALICE collaboration are described in Chapter 4. They integrate all the functionalities of amplification, digitization and read-out making them complex "System-On-Chip" circuits extremely performant that find many other applications. A family of 3 chips reads out the Si-W electromagnetic calorimeter, the gas chambers of the digital hadronic calorimeter or the SiPMs of the analog hadronic calorimeter. These circuits have re-used several blocks developed for the multi-anode photomultipliers readout, developed in the early 2000's for the target tracker of the OPERA experiment and continued for the ATLAS luminometer, which are described in Chapter 5. These chips find a continuation in the future Water Cerenkov detectors, with large "smart" photodetector arrays.