A High Speed, Low Noise ASIC Preamplifier for Silicon Strip Detectors

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Abstract

A first version Tektronix Quickchip semicustom ASIC preamplifier for silicon strip detectors was reported in Oct., 1988[1]. An improved version, QPA02, has been designed which incorporates laser trimming of nichrome resistors as a means of compensating for chip resistance process variations, which affected the response of the first version. This allows chips with randomly varying resistance values to be trimmed to have a standard output pulse shape. The QPA02 also has improved performance specifications. This paper describes the design philosophy and specifications of the QPA02, and the test results.

Introduction

The QPA02 is a high speed bipolar transimpedance amplifier built using a Tektronix "Quickchip 2S" semicustom linear array. It converts an impulse of charge to a fast voltage pulse. It was designed for use as a silicon strip amplifier for Fermilab E-771[2], but will be used in E-789 and may have other applications as well. E-771 requires an amplifier with a fast response to a charge impulse input, since the time between beam buckets is about 19 ns. The QPA02 has an impulse response that returns to baseline in less than 38 ns, or two beam buckets, for a detector capacitance of 20 pf. A high gain amplifier was designed (of order 15 mv/fc) so that output signals traveling over long cables could directly drive discriminators. This also reduces sensitivity to external noise pickup. A buffered differential output was necessary to drive flat cable with maximum noise immunity. E-771 space constraints forced a high channel density, which motivated an integrated circuit design.

The Tektronix Quickchip linear array was chosen for this design over other available high performance bipolar linear arrays because Tektronix markets its own design tools which facilitate accurate simulation and layout, and because custom laser trimmable nichrome resistors are available on Quickchip. A first prototype amplifier, QPA01, was designed, produced, and tested[1]. The response of the amplifier differed somewhat from the nominal simulations due to process variations in on-chip resistor values. This emphasizes one of the major challenges in analog integrated circuit design. Chip resistor values can vary widely from run to run and are unpredictable. However, the designer can make use of the fact that on any given chip the resistors are matched to within 1%. The second version amplifier, QPA02, is designed to use a nichrome resistor laser trimming scheme to partially compensate for these resistance variations, resulting in a more standardized output pulse response.

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The Quickchip Design Process

Designing with Quickchips is a well defined process. Normally a design is simulated and its performance understood by using TSPICE (a Tektronix proprietary enhanced version of SPICE 2G) before commencing layout. This is done using Tektronix supplied component libraries. Then a die selection is made from several available types. This is usually based on the number of components and I/O pads needed per chip. Layout is then performed using the QUICKIC (Tektronix version of KIC) layout editor. Two levels of metal are available to interconnect components. Sometimes layout constraints force component changes. This necessitates a return to TSPICE to verify any design changes. A design review at Tektronix checks the integrity of the design. Normally a prototype run of chips is made and performance checked before ordering production quantities.

Amplifier Design

The QPA02 is a two stage amplifer. A schematic is shown in Fig. 1. The first stage, or preamp, is a transimpedance feedback amplifier in the common emitter configuration to convert a charge input to a voltage output. The second stage is a differential voltage amplifier. Its function is to boost the gain, shape the preamp output, and provide differential outputs to drive a transmission line. A "reference" preamp stage, similar to the input stage, is used to provide DC tracking to the second stage. This is necessary since DC bias levels are somewhat uncertain due to process variations and temperature effects. This reference stage has no input capacitance and is bandwidth limited with a relatively large on-chip capacitor. Therefore it does not contribute significantly to the output noise.

Preamp

The preamp input transistor Q1 is a large area transistor to minimize noise due to base resistance. A cascode transistor, Q2, limits Miller capacitance at the input. The cascode base

bias voltage is supplied by a simple diode string. An emitter follower, Q3, buffers the cascode collector to the second stage. A feedback resistor is connected from a variable attenuator (driven by the follower) back to the input.

This stage has two important open loop poles, one significantly higher than the other. The feedback resistor value is selected to give a slight overshoot in the impulse response. (This overshoot is smoothed out by the second stage shaper and causes the output to have a quicker return to baseline). The dominant open loop pole is formed by the capacitance at the input node (dominated by the detector capacitance C_d) and the input resistance R_π. This can be written as

$$f_1 = 1/2\pi R_\pi C_d = g_m/2\pi\beta C_d.$$

Since g_m is inversely proportional to I_c, and I_c is nearly proportional to the collector resistance R_c, f_1 is then proportional to $1/R_cC_d$, and is nominally around 2.5 MHz. The second pole is formed by the cascode collector node capacitance, C_c, and the collector resistor, and can be written as $f_2 = 1/2\pi R_cC_c$. Its nominal value is 65 MHz. The DC open loop transresistance is approximately βR_c. Without the cascode transistor, the amplifier would have only one important pole, formed by C_d added to the Miller capacitance of Q1. Such a configuration would be more sensitive to process variations in input transistor parasitic capacitance, and would have a longer impulse response fall time. By using the cascode, however, the response becomes more sensitive to variations in input capacitance. Since detector capacitances should be relatively uniform channel to channel compromise is acceptable. The nominal design assumes ... pf input capacitance, but other capacitances can be used. Supply voltage can then be used to adjust the impulse response if desired.

Since the two poles are widely separated, and the feedback is set such that the loop gain falls to one at about 25 MHz, the preamp closed loop bandwidth and phase margin are determined mainly by f_2 and R_{fb}. Thus process variations in resistance will affect the amplifier's response. Assuming fixed C_d, the value of R_c has little effect on the open loop gain at f_2, since a change in R_c moves f_1 and the DC open loop gain in opposite directions, preserving gain bandwidth. In order to stabilize the response in the presence of process variations, the second pole frequency and the amount of feedback must be held constant. A scheme in which R_c and R_{fb} were formed from nichrome and then laser trimmed was considered. However, the values required were too large to be practically designed as nichrome trims. Also, there is no easy way of monitoring the resistance values while trimming to know when the correct value has been reached. Therefore, a method was developed which uses small value nichrome resistors as "fuses" which can be left in or cut out by laser. There are five different discrete configurations to which the amplifier can be "trimmed" by cutting different combinations of fuses. These configurations are assigned to evenly spaced portions range of possible chip resistance variation. A test re...or

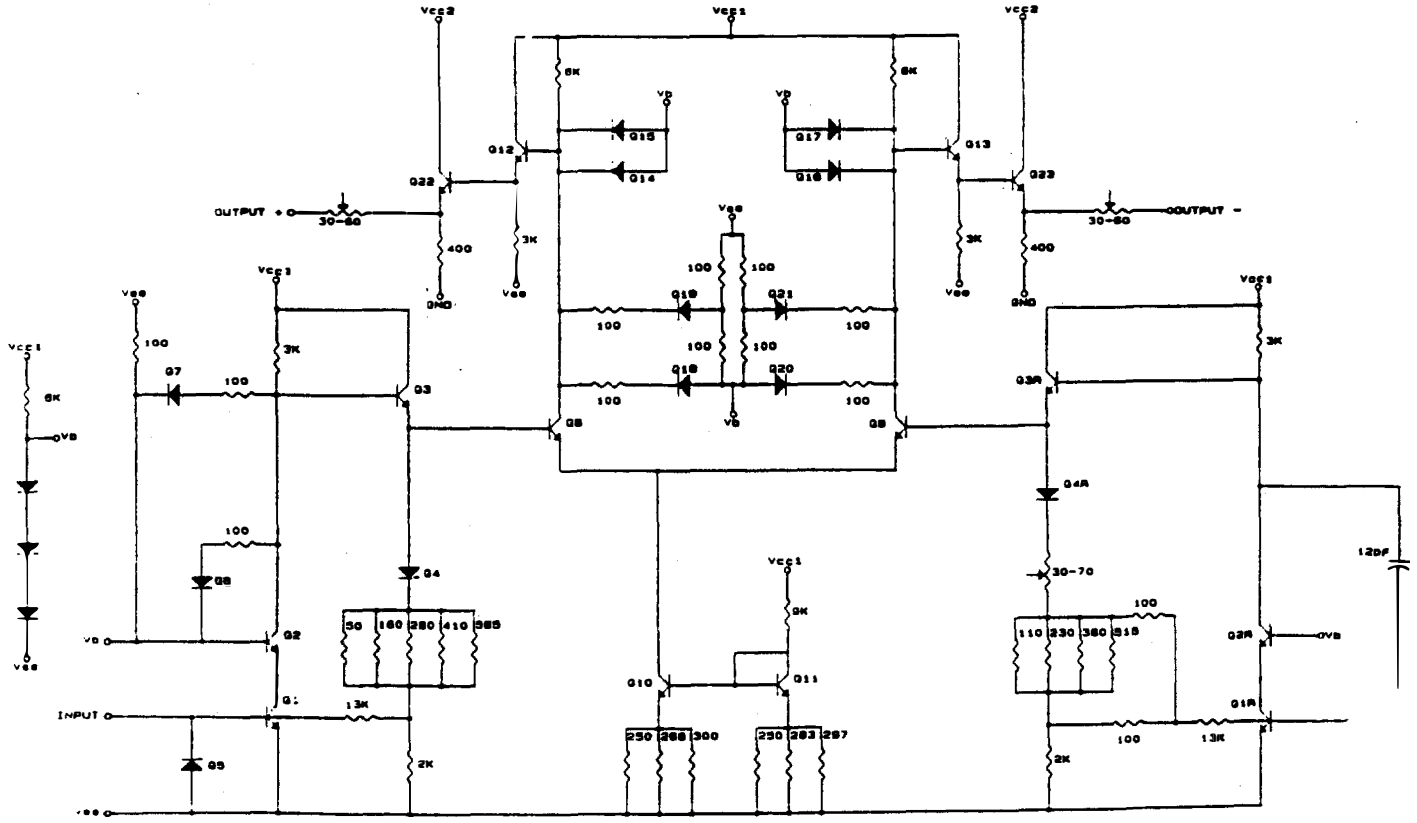

Fig. 1 - QPA02 Schematic

measurement determines which configuration is appropriate for any given chip. Nichrome laser cuts can then be made before the chip is powered up.

The frequency of the second pole is held at 65 MHz by changing the capacitance on the cascode collector node, based on the test resistor measurement. Two small capacitors in the form of back biased junctions are connected to this node through nichrome fuses. The value of one of these junction capacitors can be set to one of two levels by changing the value of back bias voltage via nichrome fuses. Thus a total of five different values of capacitance are available at this node. The amount of feedback is held at a constant value by trimming an attenuator which drives the feedback resistor (again, in discrete steps). This is done by cutting out four of five parallel nichrome resistors, based on the test resistor measurement. The response and phase margin of the preamp have been stabilized against chip resistance variation by using this technique.

The reference stage used for DC balance contains similar feedback attenuator trims, but the other trims are not necessary. A continuously trimmable nichrome resistor is added in order to remove any remaining DC imbalance due to transistor Vbe or Beta mismatch. This is an active trim done by monitoring the DC output voltage while the device is powered.

Amplifier/Shaper

The second stage is a differential pair, Q8 and Q9, which is biased by a degenerated current mirror, Q10 and Q11. This stage provides an amplified differential signal at the collectors of the differential pair. Each collector is buffered in order to drive a transmission line. The output is bandwidth limited by adding capacitance to the collector nodes in the form of back biased junctions. This shapes the signal and limits the noise. The nominal shaped signal peaks at about 10 ns and is less than 35 ns base to base. The first stage overshoot helps speed up the fall time at the output. Since the shaping depends on the RC time constant at the collector, the chip resistance value affects this. Therefore, a nichrome trim scheme similar to that used in the first stage is implemented here to trim the capacitance to one of five discrete values. Thus the shaping time constant will remain relatively constant.

The preceding scheme allows a standard output pulse shape over a range of chip resistance values. However, amplitude differences exist for the different cases since the resistance affects the gain. Therefore, the current mirror degeneration resistance in the second stage is formed from parallel nichromes of different values that were determined empirically using TSPICE. By cutting out two of the three resistors in each leg, the gain can be set such that the pulse height will be at a fixed value.

The output section of the second stage consists of small area emitter followers, Q12 and Q13, to buffer the collectors and drive larger output transistors, Q22 and Q23. An internal pulldown resistor is used to bias each output transistor at about 4 ma. An external pulldown may be added to increase the dynamic range if desired. A laser trimmable back termination is provided in series with each output.

QPA02 Layout

The Quickchip 2S die, the smallest available, was chosen for the layout since it contained the correct number of pads for four channels, and because the component layout was fortuitous. The pad assignments are shown in Fig. 2. The channels are laid out in columns, with input pads on the bottom and output pads on the top. Power supply pads are on either side. The preamplifier stages are on the bottom half of the chip, and the amplifier/shaper stages are on the top half. This arrangement maximizes isolation between inputs and outputs. Fig. 3 shows two chips bonded into a custom chip

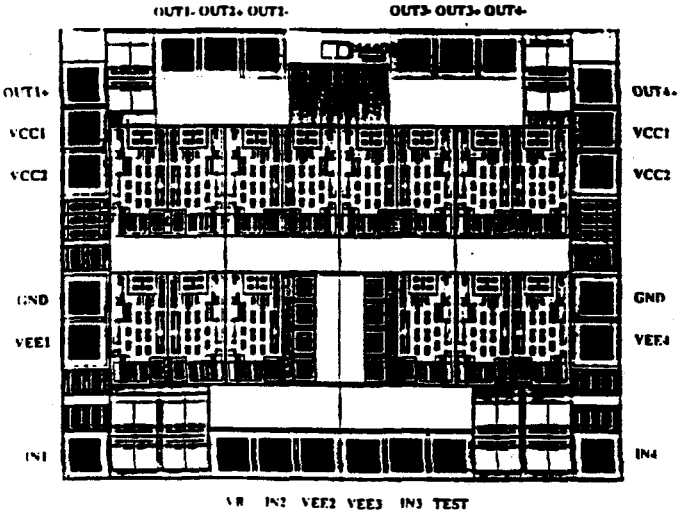

Fig. 2 - Quickchip 2S die with pad assignments

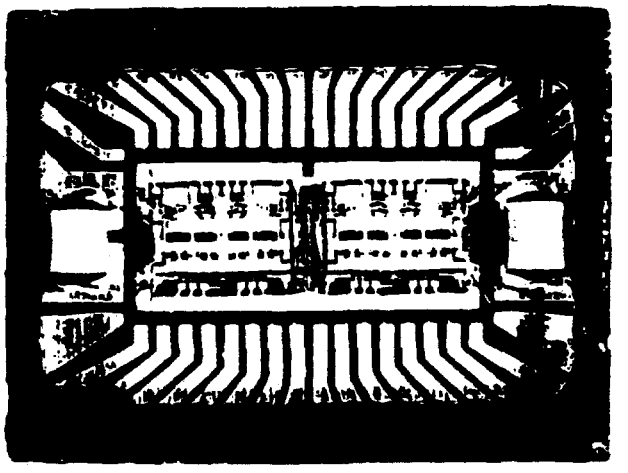

Fig. 3 - Two QPA02's in custom chip carrier

carrier. Small bypass capacitors for the output driver supply are also mounted inside the carrier.

A separate reference (VEE) pad is necessary for each channel to avoid common impedance crosstalk. Output driver pulldown resistors are included on the chip to avoid DC currents in output cables. These are all connected to a common point (GND). When using QPA02, GND and VEE pads should all be referenced to the same low impedance ground plane.

The output driver transistors are connected to a separate power pad, VCC2. This avoids the problem of high output currents coupling to the input circuitry. Also, this allows VCC2 to be independently adjusted. VCC2 should not be more than 2.0 volts lower than VCC1. For ease of use, VCC2 may be run at the same supply voltage as VCC1. However, this will result in increased power dissipation.

The cascode bias, VB, is shared between all channels on a chip. It is connected to a pad so that it can be externally bypassed. This is necessary to reduce crosstalk and to limit random noise components.

Since this amplifier has a large gain-bandwidth, it requires special care in grounding and shielding for practical use. This is the subject of another paper presented at these proceedings[3].

Performance and Test Results

Prototype chips were supplied by Tektronix for evaluation. Fig. 4 is a diagram of the test board used. For all tests, VCC1 was set at 4.5 volts and VCC2 at 2.5 volts. Response and noise measurements were made for a variety of input capacitances and compared to TSPICE predicted values. In all cases, the measured results closely matched the TSPICE values, proving the value of design simulation.

Fig. 5 is the measured impulse response for a charge input of 4 fc, taken at one output. This translates to a differential impulse gain of 17 mv/fc for Cin=20 pf. Fig. 6 illustrates how VCC1 can be varied to adjust the impulse response. In this case, VCC1 is used to keep the same pulse width for a variety of input capacitances. The QPA02 has a dynamic range of approximately 30 fc at the input before the

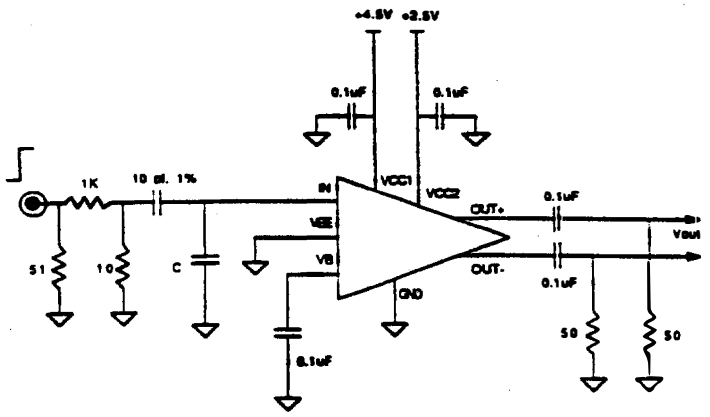

Fig. 4 - QPA02 test circuit diagram

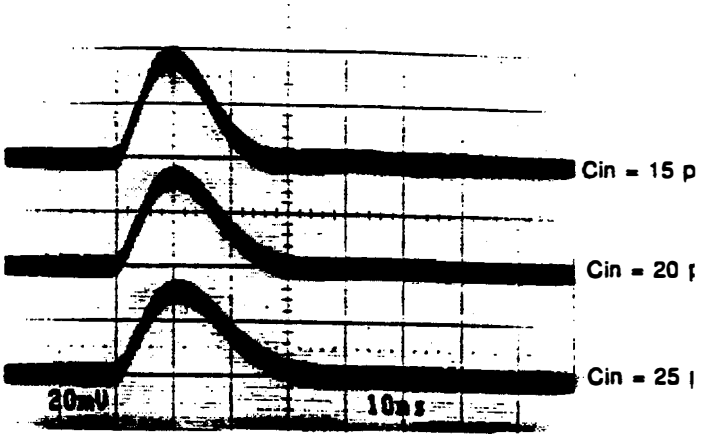

Fig. 5 - Impulse response

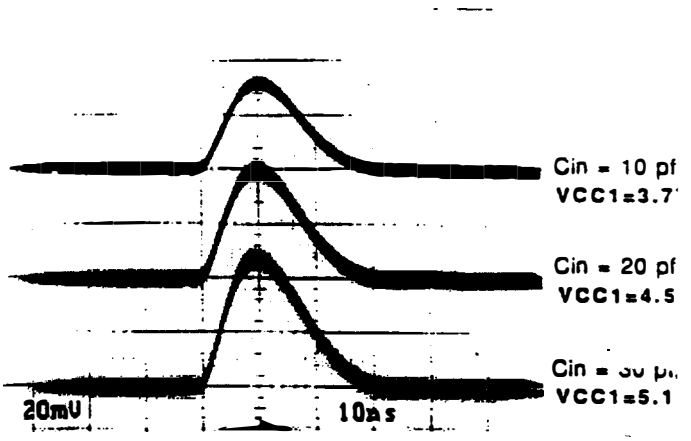

Fig. 6 - Impulse response adjusted with VCC1

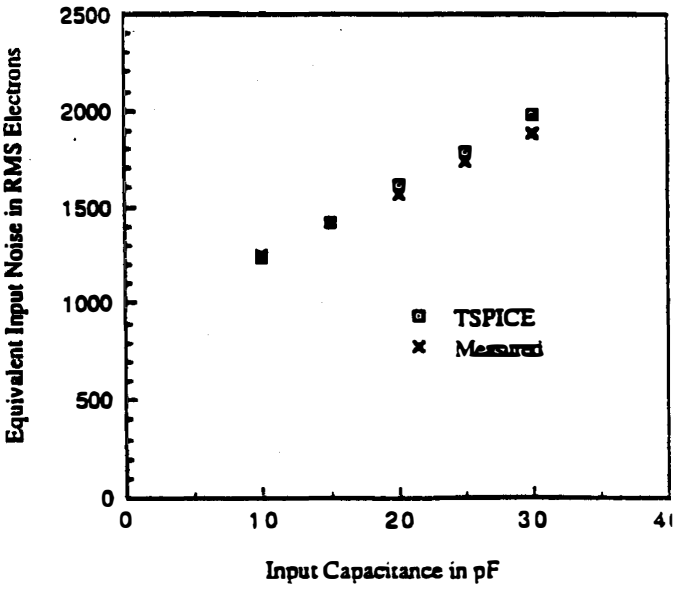

Fig. 7

outputs begin saturating. However, linearity is degraded above 10 fc.

The noise performance was measured using a LeCroy 620AL discriminator[4] and is shown in Fig. 7. The input noise is approximately 1570 electrons for Cin=20 pf.

The power consumption of the QPA02 is approximately 45 mw per channel. Channel to channel crosstalk is measured at typically 0.5%. The input impedance is approximately 200 ohms.

Conclusions

Semicustom linear arrays can be a fast and reliable way to produce integrated amplifiers for high energy physics. The QPA02 has been tested and demonstrated to be an effective silicon strip amplifier for high rate applications, performing as modeled. Other applications may exist which can use this amplifier or a modified version of this amplifier.

Acknowledgements

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References

[1] D. Christian, et. al., "The Development of Two ASIC's for a Fast Silicon Strip Detector Readout System", IEEE Trans. on Nucl. Sci. NS-36 (1988) 507-511

[2] C. Swoboda, et al., "A High-Rate FASTBUS Silicon Strip Readout System", presented at the 1989 Nuclear Science Symposium.

[3] R.J. Yarema, T. Zimmerman, "A High Speed, High Gain Preamplifier System for Silicon Strip Detectors", presented at the 1989 Nuclear Science Symposium.

[4] This method is described by P. Jarron and M. Goyot, NIM 226 (1984) 156-162