TEST RESULTS OF TWO LBL SVX SILICON STRIP DETECTOR READOUT CHIPS AND THE LBL RADTEST CHIP

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I. INTRODUCTION

Two versions of a silicon strip detector readout chip built by S. Kleinfelder and others at LBL have been received at Fermilab. Version SVXC, the latest revision, containing significant modifications from SVXB, was received October 1987. This chip, aside from several minor problems, is functional and has been tested at LBL and at Fermilab. SVXB', received Dec. 1987, is a modified version of the SVXB chip, with larger input transistors, and has been tested at Fermilab. Also tested at Fermilab was a RADTEST chip received from LBL. This chip is a test chip designed by S. Kleinfelder and H. Spieler containing SVX front end amplifier structures of different sizes so that gain and noise can be easily measured and compared to theory. Results of measurements made on these chips at Fermilab are presented in the following pages. For reference and comparison, extensive test results of the previous version readout chip, SVXB, have been presented in a previous report (2). These tests were performed in collaboration with S. Kleinfelder, R. Ely, C. Haber, and H. Spieler of LBL.

II. RADTEST MEASUREMENTS.

Figure 1 is a diagram of the SVXC front end cascode integrator and first amplifier-comparator (called the "B" amplifier). The RADTEST chip contains several cascode amplifiers (output at the source follower) of similar configuration but without the feedback capacitor, so that open loop measurements can be made. The B amplifiers are not present. There are two different size structures. The RADTEST "small amplifier" is sized identically to SVXB (input transistor W/L = 250/3). The "big amplifier" is ten times larger (input transistor W/L = 2500/3). For all measurements, V_{DD}=6V, and V_N=V_P=3V. The cascode amplifier current was set to the design current of 65 μa in the small amplifier and 650 μa in the big amplifier.

OPEN LOOP RESPONSE

Figures 2 and 3 show the open loop gain and phase response for the small and big amplifiers, respectively. These plots were done with an H.P. 3577 Network Analyzer. The amplifier was put into the active region with a 20 MΩ feedback resistor. A BUF03 unity gain buffer was driven by the amplifier output. For the open loop measurement, the network analyzer source drove the amplifier input through a 0.1 μf capacitor. The test circuit used is shown in Fig. 4a.

The small amplifier has an open loop gain of about 2600 and a pole at around 90 KHz, for a gain bandwidth product of 230 MHz. SPICE predicts an open loop gain of 1900 and the first pole at 125 KHz for a very similar GBW product of 240 MHz. The measured open loop gain is much higher than the gain of 700 previously reported for SVXB (2). In fact, a design change was made in the amplifiers to increase the open loop gain. The second pole introduced by the source follower is predicted at above 10 MHz by SPICE, but is observed at 4 MHz here because of the external capacitive load.

The big amplifier response, shown in Fig. 3, is very similar to the small amplifier response. The second pole is higher in frequency, but this may be due to external loading effects.

NOISE DENSITY

It was desired to measure the noise density of the RADTEST amplifiers so that 1) the small amplifier thermal noise could be compared to the SPICE prediction for SVXB, 2) the scaling of thermal noise vs. transistor size could be checked, and 3) the 1/f noise could be found. In order to measure this, the amplifier was run with resistive feedback (through large value capacitors to preserve the DC operating point) so that the gain could be set to a known value and would remain stable. The output point of the amplifier was taken as the BUF03 output. Fig. 4b shows the test circuit used. The output noise density was measured with an H.P. 8568 Spectrum Analyzer, using the noise marker function. The input noise density was then calculated using the closed loop gain curve from the network analyzer. In most cases the BUF03 noise was negligible. If not negligible, it was subtracted out.

Fig. 5 shows the resultant noise densities as a function of frequency for the small and the big amplifiers. The curves plotted obey the following equations:

SMALL AMPLIFIER: $e_n^2 = (6.8 \times 10^{-12}/f^{0.87}) + (7.0 \times 10^{-9})^2 \ V^2/Hz$

BIG AMPLIFIER: $e_n^2 = (4.3 \times 10^{-13}/f^{0.84}) + (2.1 \times 10^{-9})^2 \ V^2/Hz$

The thermal noise of the small (SVXB sized) amplifier is 7 nv/$\sqrt{Hz}$, whereas SPICE predicts about 5 nv/$\sqrt{Hz}$. This difference is not understood. The measured big amplifier noise should be smaller than that of the small amplifier by a factor of $\sqrt{10}$, or 3.2, in theory. The measured result of 2.1 nv/$\sqrt{Hz}$ is smaller by a factor of 3.3. Therefore the scaling of the noise agrees with theory. Thus we can project the thermal noise of SVXC (500/3 input transistor) at about 5 nv/$\sqrt{Hz}$, a factor of $\sqrt{2}$ smaller than the small amplifier.

The 1/f noise is really not strictly 1/f, but falls at a somewhat slower rate with frequency. This puts the noise corner at 800 KHZ. Thus for a double correlated sample with t_s (time between samples) in the range of 1 μs, the "1/f" noise can have a contribution to the total noise.

III. SVXC MEASUREMENTS

SVXC has been modified substantially from SVXB in order to reduce the number of I/O pads and reduce the noise. Analog section control input lines and digital address output lines now share an 8-bit bidirectional bus. The SVXC input transistor size (500/3) is twice that of the SVXB input transistor (250/3), and the B amplifier following the input integrator stage has been bandwidth limited to improve the noise. Also, the feedback capacitor has been moved from the integrator source follower output to the cascode output, which removes a pole from the feedback loop and substantially reduces the ringing when the integrator is reset.

If a normal acquisition pattern is run on SVXC, the analog output appears to be saturated. To correct this and put the amplifier in its active region, a calibration pulse of several hundred millivolts must be injected after the amplifiers are reset. This behavior was not observed with SVXB. One possible explanation is that the modified reset switches are now injecting more charge when opened, saturating the amplifier. A large calibration pulse then brings the amplifier back out of saturation. This effect is being investigated and is not yet fully understood. Running the chip like this makes it difficult to check all the parameters that were checked on SVXB, but it is believed that the important measurements of gain and noise can be made accurately by double correlated sampling.

Also, there is a minor error in the latch-all circuit. If it is desired to read out all channels, then the calibration pulse injected to bring the amplifiers out of saturation must be large enough to make all the channels look hit, after which the output latch is clocked.

Fig. 6 shows the pattern used for these tests. A high level indicates a switch closure. The WE', RE', and H/L lines control the bidirectional bus. First a chip ID address is written to the chip when WE' is low and H/L is high. WE' low and H/L low then allows the analog section to be clocked. The amplifiers are reset, a large calibration is injected to bring the amplifiers into the active region, the output latch is clocked to force all

channels to read out, and a double correlated sample is then performed with R_C and R_S. To perform a digital readout, RE' is brought low. Toggling H/L then alternately clocks out the hit address and the chip ID address.

GAIN

The charge gain was measured by applying a voltage step to a 10 pf, 1% surface mount capacitor connected to a bonded input channel. This yielded a charge gain of 39 mv/fc. The gain of SVXB was about 29 mv/fc. This probably indicates an increase in the gain of the B amplifier following the integrator (it was modified to reduce the bandwidth). LBL has measured the B stage gain on the probe station to be around 18-20. Thus the integrator gain would be 2 mv/fc, which indicates a 0.5 pf feedback capacitor instead of 0.3 pf. The cause of this discrepancy is not known.

TRANSFER CHARACTERISTIC

It is difficult to measure a transfer characteristic because the large charge injection used causes an unknown offset in the amplifier. However, by varying the input injection through a 10 pf capacitor to one channel, a ΔVout of $\approx$1V was observed before saturation. This is less than the 1.8V observed for SVXB, but there is some uncertainty with this result due to the method.

RISETIME

The risetime of the analog stage (in this case limited by the B amplifier) was measured in two different ways: 1)The sample and hold switch was left closed while performing a readout, and a charge was injected into a channel while that channel was connected to the analog readout line. 2)A "sampling" technique was used in which the sample and hold switch was opened at progressively longer times after charge injection. Method 1 gives an output risetime (10%-90%) of $\approx$1 μs. The analog output buffer risetime is $\approx$400 ns, therefore the B amplifier risetime would be $\approx$900 ns. The 3 db bandwidth would then be 400 KHz. Method 2 gives a waveform which is of the form $V = V_{max}(1-e^{-t/RC})$. This is in fact predicted by SPICE but not observed with Method 1. The RC time constant was measured at 260 ns, giving a 3 db bandwidth of $\approx$600 KHz. The risetime does not change with input capacitance, since the B amplifier is the bandwidth limiter, not the integrator. In contrast, the SVXB measured RC time constant (using the sampling technique) is 65 ns for C_{in} = 0 pf, for a bandwidth of 2.5 MHz. Also, the risetime increases somewhat for larger C_{in} since the B amplifier is not necessarily the bandwidth limiter.

Method 2 is considered the more accurate method, and this is in fact how the chip will be used. More information about signal height vs. window time is given in a following section of this report.

NOISE

In an attempt to lower the noise of SVXC from that of SVXB, the input transistor was doubled to 500/3, and the B amplifier was bandwidth limited. Doubling the transistor should result in a factor of $\sqrt{2}$ lower noise. Similarly, the noise should be reduced by a factor of the square root of the ratio of the bandwidths. However, this comparison is more complicated because the SVXB bandwidth varies somewhat with input capacitance.

Figure 7 is a plot of the measured noise referred to rms electrons at the input for double correlated sampling. The noise was measured by taking a histogram of the output voltage of one channel with a QVT in V mode. For a double correlated sample on SVXB (t_s = 5 μs), the noise slope is 160 e/pf (this is the initial slope of the curve). Extrapolating back to the x-intercept gives an unbonded channel input capacitance of ≈3 pf. This is due to input transistor gate capacitance (SPICE predicts 1.1 pf), input pad capacitance of about 1 pf, and stray.

The measured noise of SVXC (double correlated sample, t_s = 6 μs) is also plotted. It is linear, as expected. The SVXC noise slope of 38 e/pf is a factor of 4.2 lower than the SVXB noise slope, which is quite dramatic. If we assume that a factor of $\sqrt{2}$ is due to transistor size, then the bandwidth limiting is responsible for a factor of 3 in noise improvement. (The bandwidths calculated from the measured risetimes predict a factor of $\sqrt{2.5M/0.6M}$ = 2). Thus it seems very useful to keep the bandwidth as low as possible, or in other words, to keep the risetime as high as can be tolerated.

If we extrapolate the SVXC measured curve back to the x-axis, we obtain an unbonded amplifier input capacitance of 6.5 pf, which is 3.5 pf larger than for SVXB. This is somewhat more than expected, since SPICE predicts an input transistor gate capacitance of 2.7 pf for SVXC, giving an increase of only 1.6 pf over SVXB. More reasonable results are given if the intercepts are taken at the y = 150 electrons line instead of the y = 0 line. This may indicate that there is an additional noise source of ≈150 electrons present.

If a double window pattern (for leakage current subtraction) is used, this results in quadruple sampling, and the noise should be a factor of $\sqrt{2}$ higher than for double correlated sampling. The results of this measurement are in Fig. 8. In fact, the slope is measured at 230 e/pf as expected on SVXB. However, the intercept is about 400 electrons higher than expected. This is not understood. It seems as if the extra B amplifier reset performed for the double window is injecting some extra noise.

The noise for a quadruple sample on SVXC was measured and found to have a slope and intercept much higher than expected. It is suspected that this measurement is invalid since the amplifier must be twice brought out of saturation with a large charge injection, with unknown effects. Therefore the theoretically expected noise is plotted in Fig. 8, with the hope that this can be measured on a later version of the chip. This curve ignores the unexplained effect of the higher-than-expected intercept encountered on SVXB, so it may be somewhat optimistic.

NOISE VS. WINDOW TIME

The noise and signal were measured vs. t_s (time between samples) for a double correlated sample. A relative figure of merit for signal to noise is then calculated. The following table presents the results. The charge input was 1.6 fc.

ts (ns)	noise (mv FWHM)	ΔVout (mv)	S/N Merit
50	2.9	2	.69
100	4.1	10	2.4
150	5.1	18	3.5
200	5.6	26	4.6
250	6.2	32	5.2
300	6.4	37	5.8
350	6.7	41	6.1
400	7.2	45	6.3
450	7.5	48	6.4
500	7.8	51	6.5
600	7.8	55	7.1
700	8.0	58	7.3
800	8.2	60	7.3
900	8.3	61	7.4
1000	8.5	62	7.3
2000	8.5	63	7.4
4000	9.0	64	7.1
6000	10.0	64	6.4
8000	11.5	64	5.6

Presumably the increase in noise at large t_s is due to a higher weighting of the 1/f noise. The table shows that the optimum window time is ≈1 μs, which allows for an almost complete rise of the signal. Since the noise curve measured and plotted in Fig. 7 was for t_s = 6 μs, a slightly better noise performance than this might be obtained with an optimum window time.

POWER DISSIPATION

The power dissipation of SVXB was measured at 48 mw in the +6V section, and 145 mw in the +5V section, for a total of 193 mw. In SVXC, the input transistor is doubled, which should double the power required in the analog section. (The cascode current was set at 118 μa, close to the design current and about twice that of SVXB). However, this should be offset by a reduction in the digital section due to band limiting the B amplifier. The following measurements were taken on SVXC:

+6V section: 6V (20.2 ma) = 121 mw
+5V section: 5V (16.0 ma) = 80 mw
Total = 201 mw

Thus the noise performance has been improved with no expense in power consumption.

If desired, the power consumption may be lowered with some penalty in noise performance. Measurements show that if the cascode current is lowered from 118 μa to 38 μa, the noise slope increases from 38 e/pf to 50 e/pf and the +6V supply current = 8.9 ma. This agrees with theory, which states that the noise should vary as the inverse of the fourth root of the current ratio. Thus the total power dissipation changes from 201 mw to 133 mw with a 30% increase in the noise slope.

MISC.

A "readout slope" of about 50 mv for 128 channels was measured for SVXB (2). This was suspected to be due to IR drop in the power bus on the chip. The power busses on SVXC have been widened, and the slope seems to have disappeared.

The digital address lines of SVXC should increment from 0 to 127 when doing a readout. Short glitches were observed instead of levels, however. This is probably only a minor error.

IV. SVXB' MEASUREMENTS

SVXB' is quite similar to SVXB, except that the input transistor W/L has been increased from 250/3 to 1500/3, a factor of 6. Thus the noise should be down by a factor of $\sqrt{6}$, given an identical bandwidth and a cascode current that scales with the transistor size.

The cascode current is set by varying the "top bias" voltage, as on SVXB. For an SVXB' top bias voltage identical to that used for SVXB, it was found that the cascode current did not scale with transistor size. In other words, the SVXB' current was not 6 times the SVXB current. To obtain 6

times the SVXB current, the top bias had to be changed by a fairly large amount, accompanied by a drop in the charge gain. Therefore, for these tests, SVXB' was run at the same top bias as SVXB. This gave a cascode current 2.5 times larger than that of SVXB instead of 6 times larger. Theoretically, this should produce a noise level 25% higher than that which would be observed with the design current.

GAIN

The charge gain was measured at 26.7 mv/fc. This remained relatively constant for input capacitances from 10 pf to 40 pf. This indicates a high open loop gain.

RISETIME

The "sampling" method used for SVXC and SVXB was used here. A similar exponential output waveform was obtained. The RC time constant obtained from the data is ≈95 ns, which gives a 3 dB bandwidth of 1.7 MHz (C_{in} = 0 pf). The signal rises to 90% of its final value in 250 ns. The bandwidth of SVXB was measured at 2.5 MHz, so we can expect some noise reduction in SVXB' due to its lower bandwidth.

NOISE

Figures 7 and 8 show the SVXB' noise for a double sample and quad sample, respectively. In both cases, the initial slope of the curve shows a factor of 2.1 improvement compared to SVXB. If we consider the differences in transistor size, cascode current, and bandwidth, the predicted factor is 2.4. The x-intercept of the curve in Fig. 7 is 5.5 pf, which gives an input capacitance that is actually smaller than SVXC. The input capacitance should be larger than SVXB or SVXC because of the larger input transistors. However, if we assume as before that there is an additional noise in the system of 150 electrons and take the intercept at y = 150 electrons, the result is somewhat more reasonable.

POWER DISSIPATION

The power consumed in the +5V digital section was measured at 22 ma, giving a dissipation of 110 mw. The +6V analog section, running at below the design current, drew 22 ma, dissipating 132 mw. This is slightly higher than the dissipation of SVXB and of SVXC.

V. CONCLUSIONS

A substantial noise improvement over SVXB can be realized by widening the input transistors as in SVXB', even when run below the design current. (Power dissipation would probably be too high if run at the design current). However, the best approach involves limiting the bandwidth as much as is acceptable, as in SVXC.

SVXC incorporates significant design changes over SVXB to improve performance and functionality. The most important design changes found in SVXC have been measured and perform as expected. Several effects, however, must still be investigated. The most important of these is the output saturation which requires a large calibration pulse to correct. The noise performance has improved dramatically over SVXB due to larger transistors and bandwidth limiting. For double correlated sampling with a signal of 25000 electons, the S/N ratio at 30 pf is 18. The expected S/N for a double window leakage subtraction cycle is then 13, although this measurement could not be made on the present SVXC device.

References

1) Stuart A. Kleinfelder, et al., "A Flexible 128 Channel Silicon Strip Detector Instrumentation Integrated Circuit With Sparse Data Readout," submitted to Nuclear Science Symposium, San Francisco, October 1987.

2) R. J. Yarema and T. Zimmerman, "Test Results of the LBL SSD Readout Chip," Fermilab, June 1987.

SVXC FRONT END

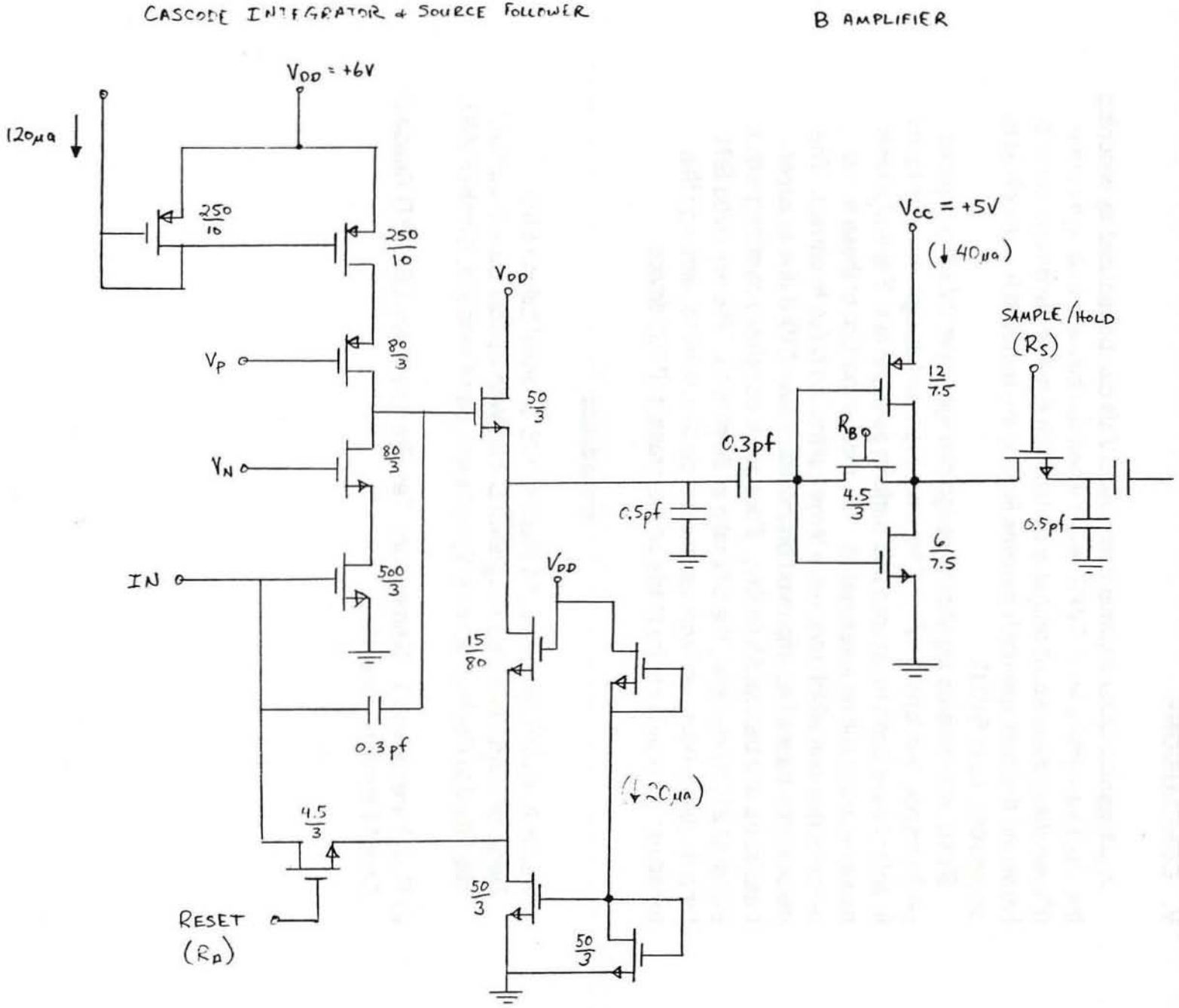


FIG. 1

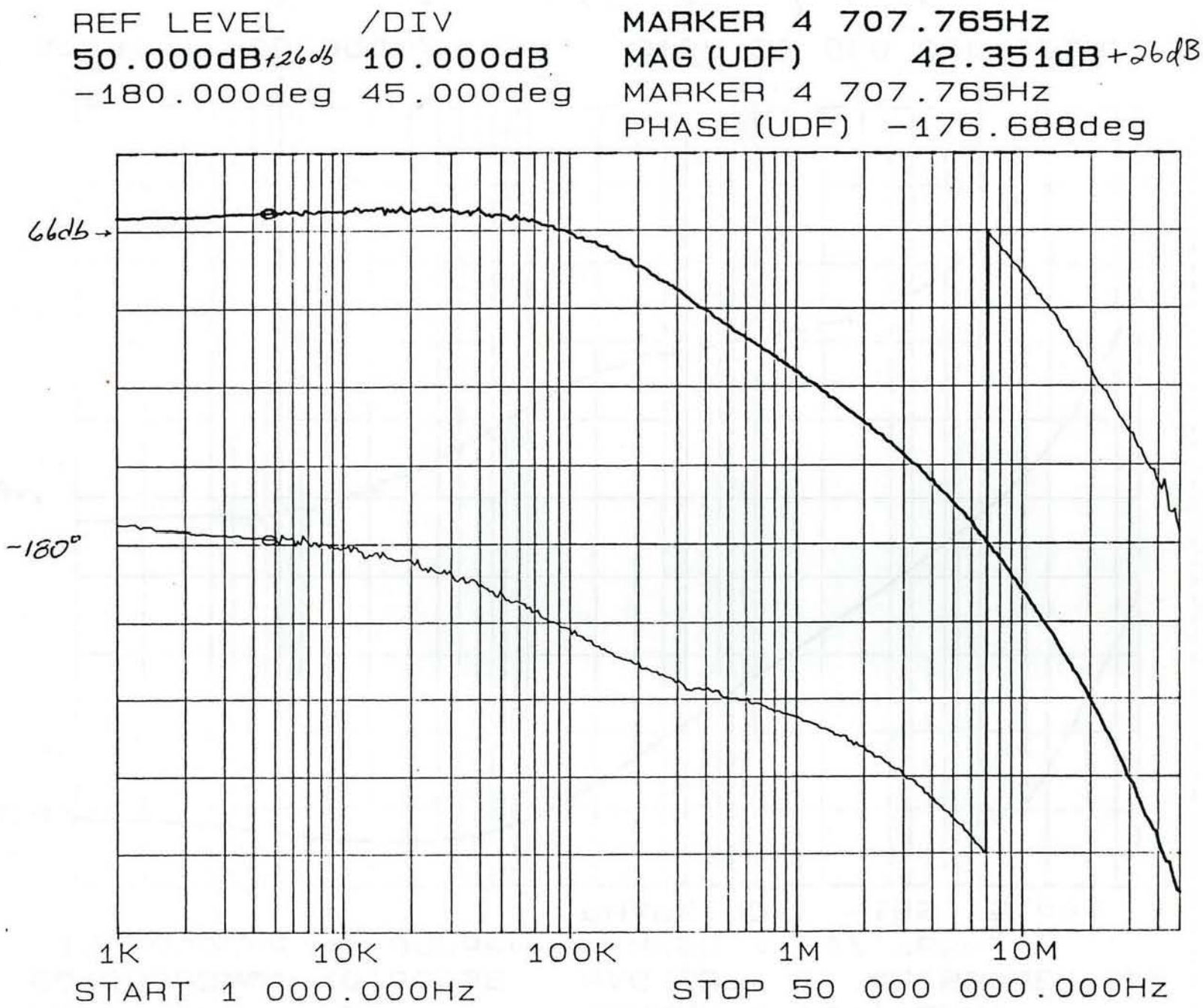


Fig. 2

Open Loop Small Transistor Amplifier + BUF03 Response.

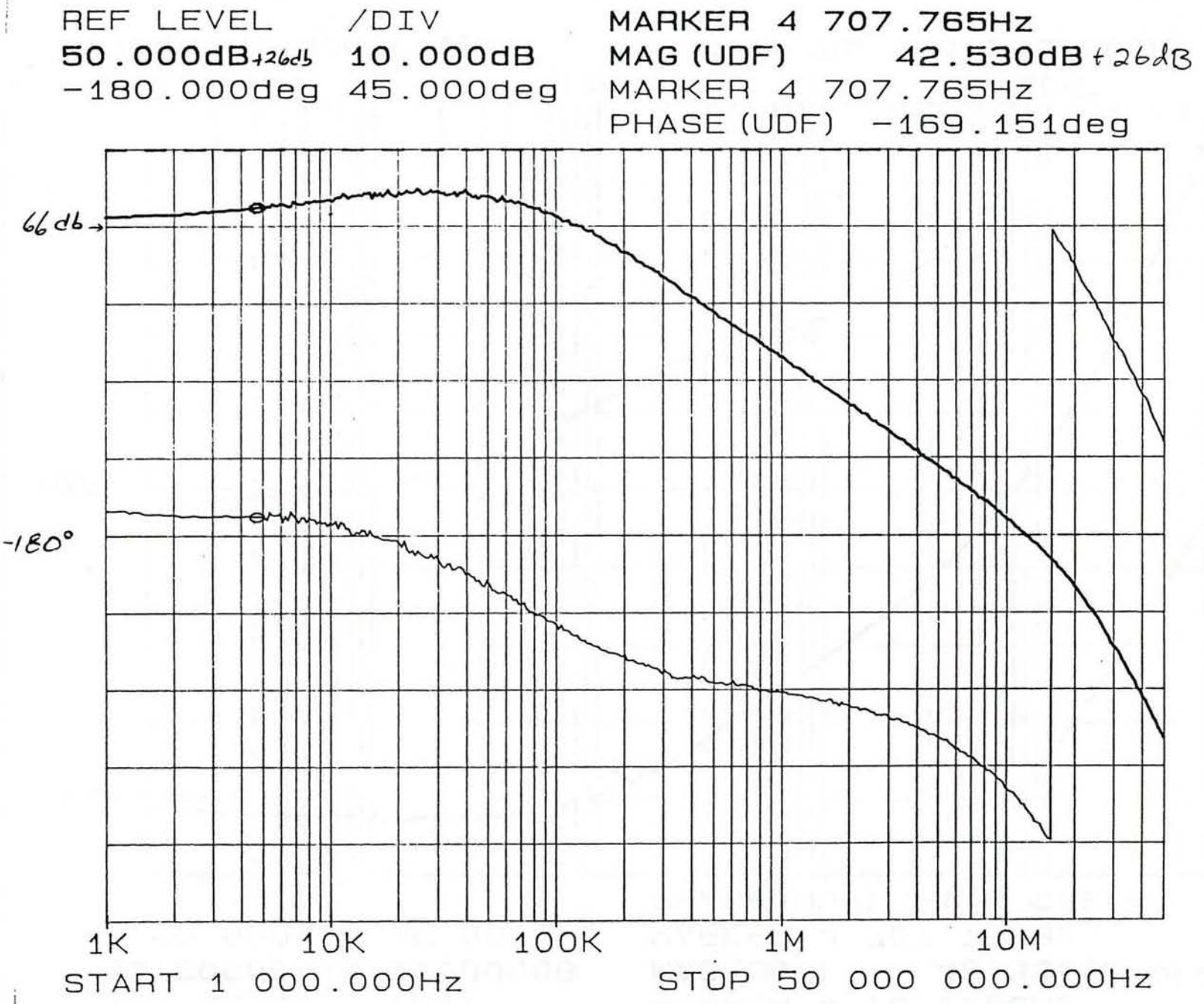
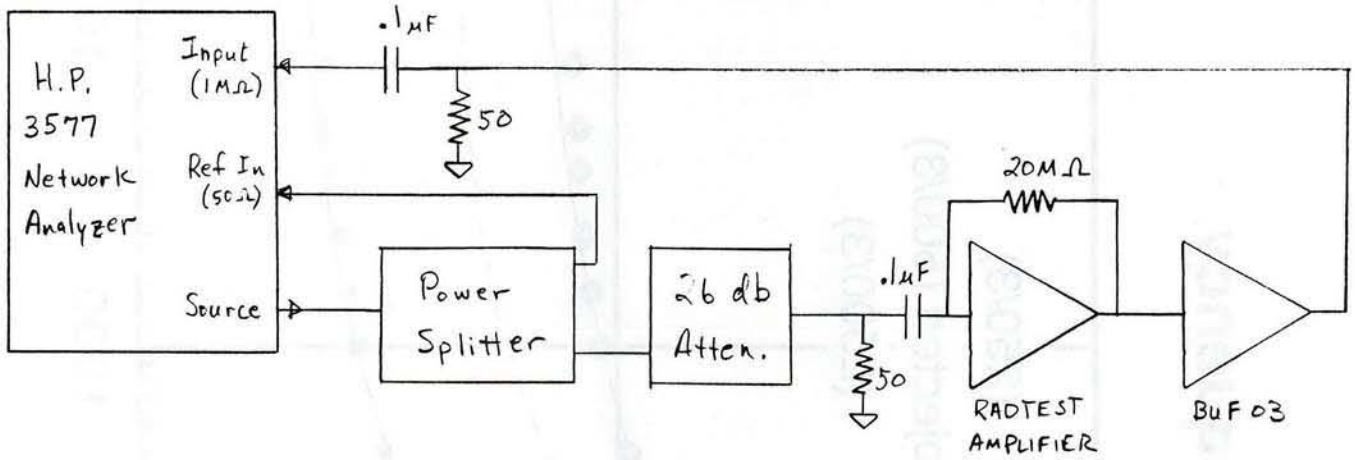
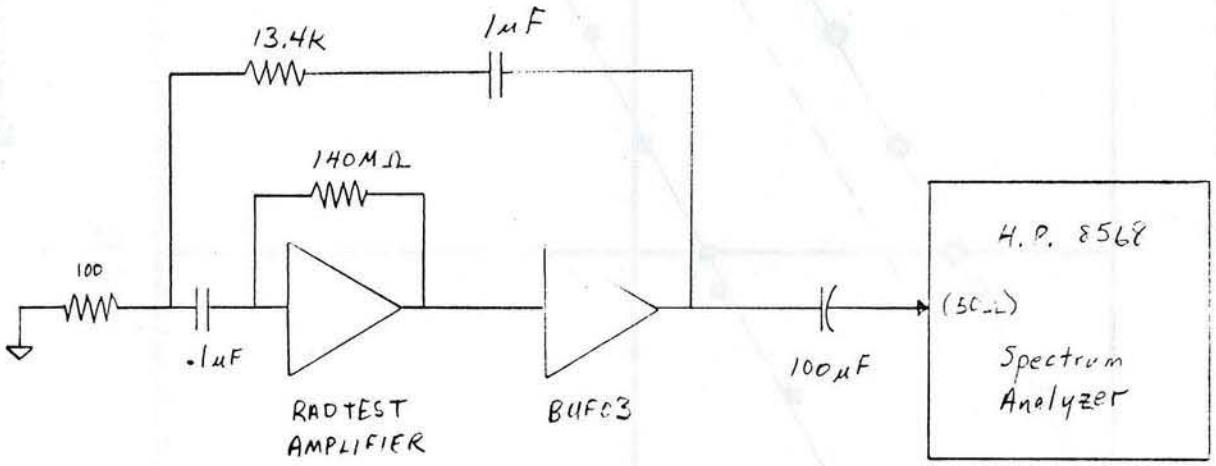


FIG. 3

Open Loop Response of Large Transistor Amplifier + BUF03



a. Open loop gain test circuit



b. Noise density test circuit

FIG. 4

SVX Amplifier Noise vs Frequency

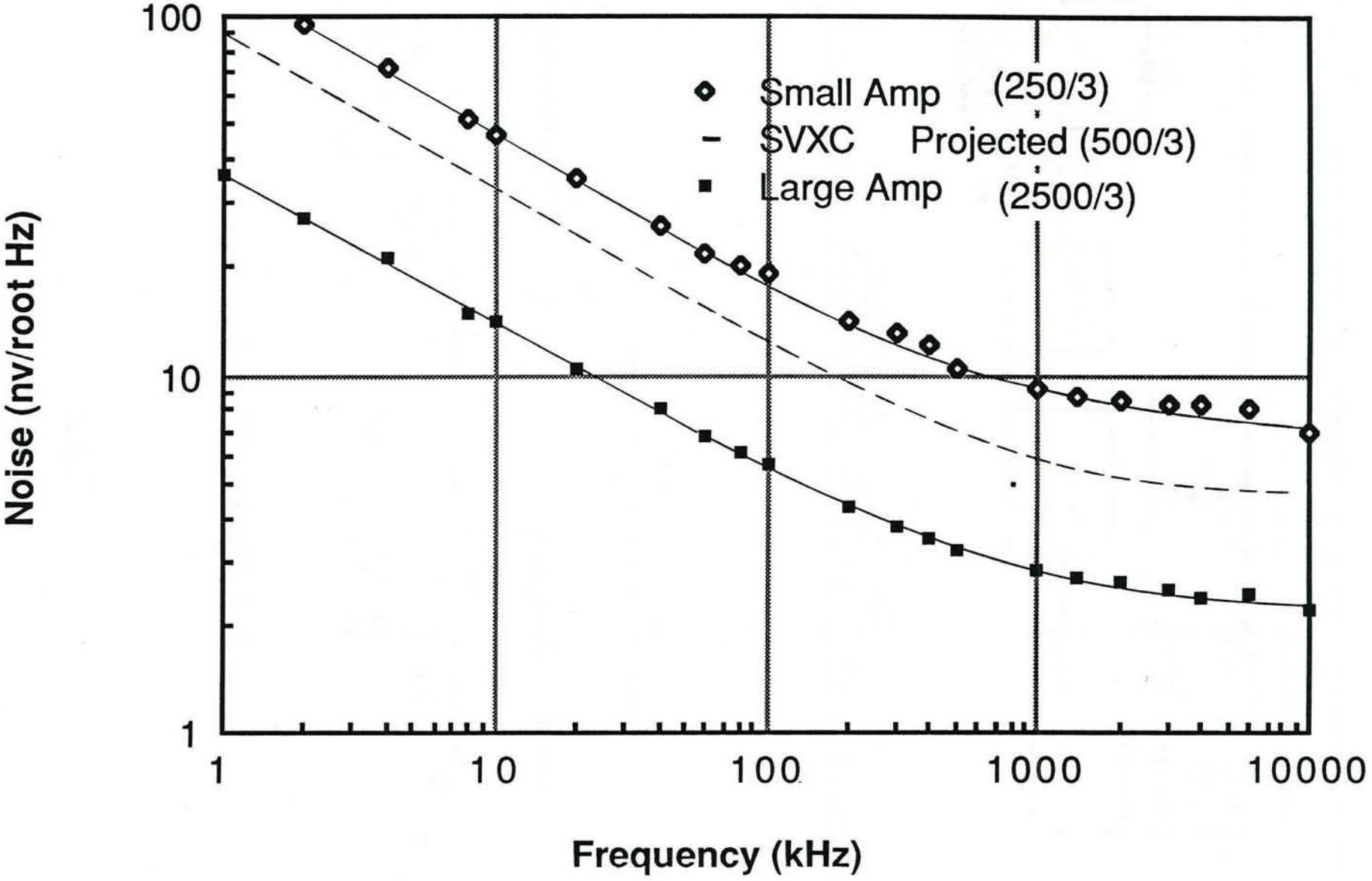
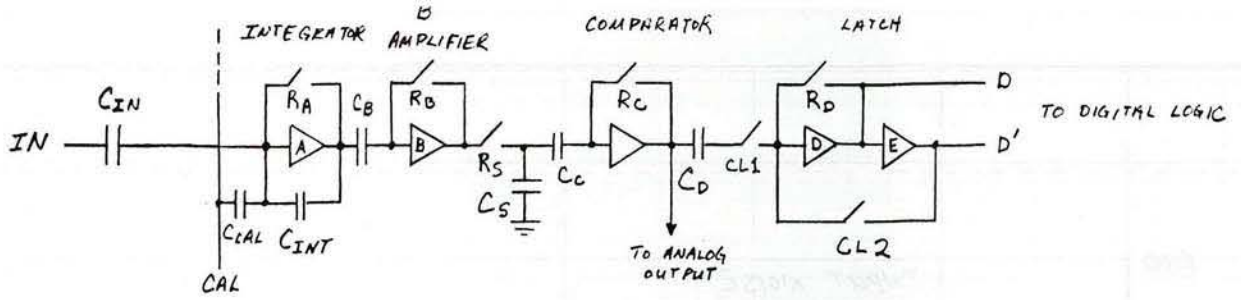


Fig. 5



Page 1 Nov 30, 1987 - 12:16 svxc3.def ADTRON Pulse Editor

OUTPUT 1: A	OUTPUT 2: B	OUTPUT 3: FIRST BIT
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CLOCK: INTERNAL	BIT CELL: 2 US	CHAN: 18 0 15K
BOARD1#: 1	BOARD2#: 2	

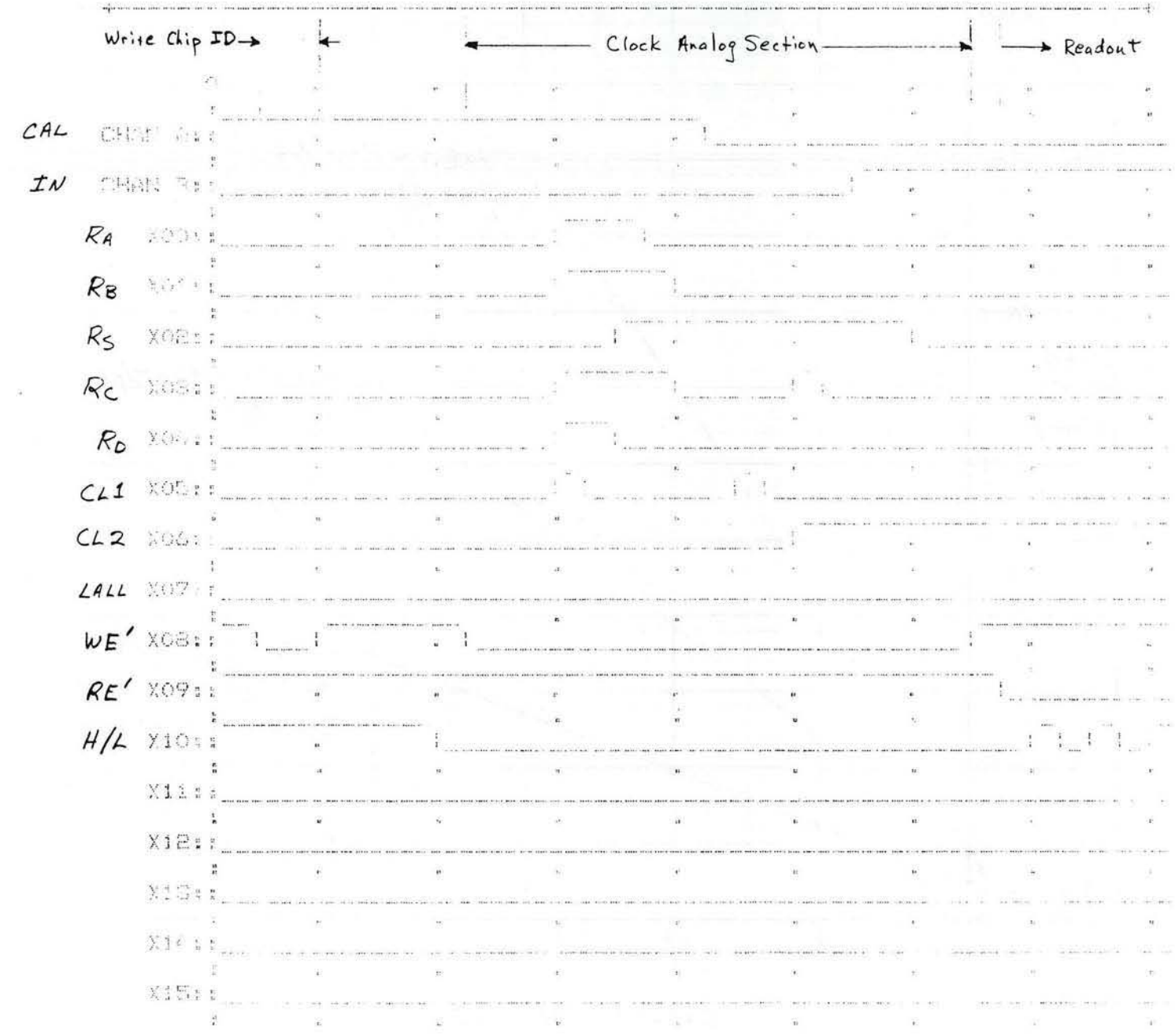

FIG. 6

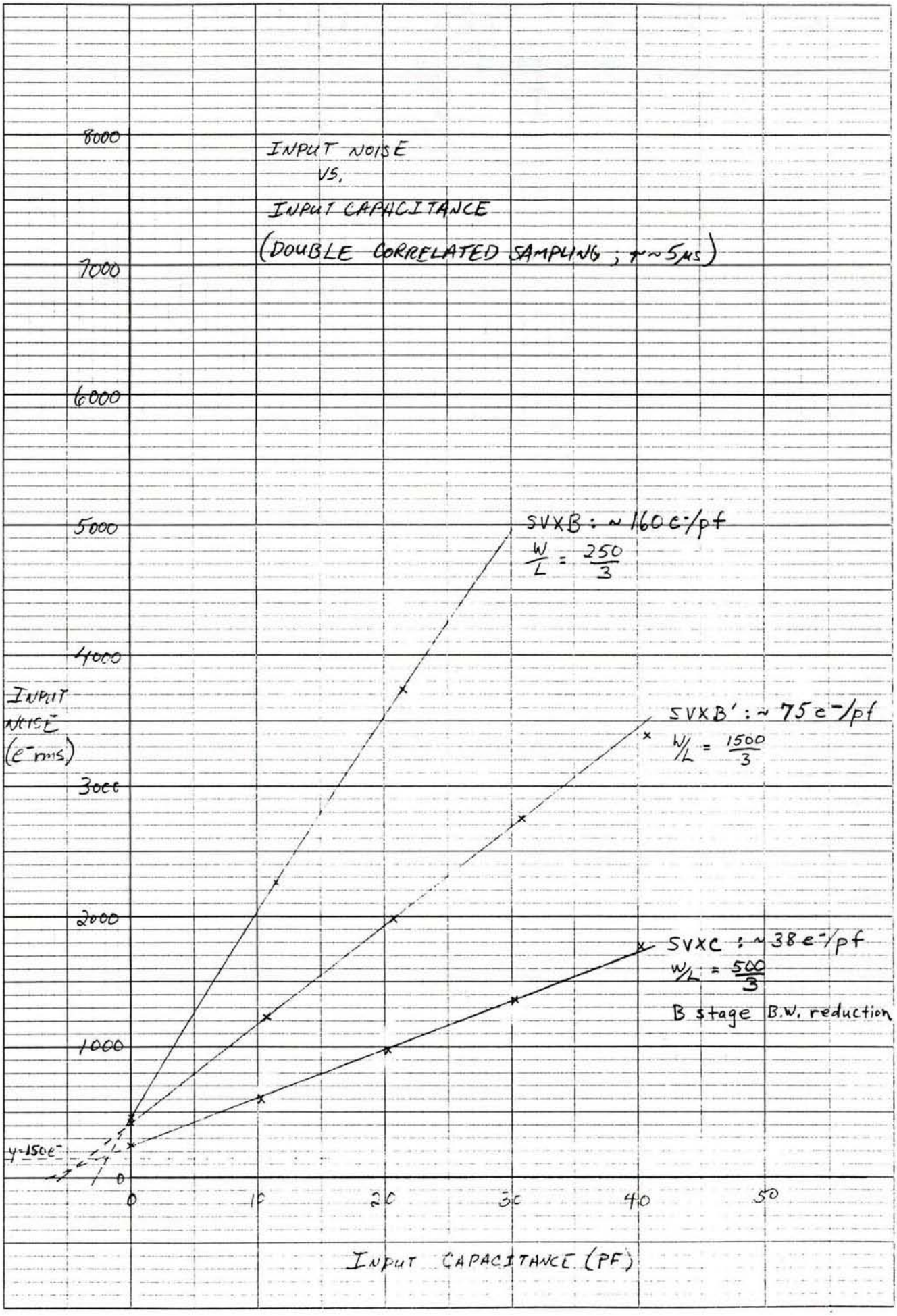

FIG. 7

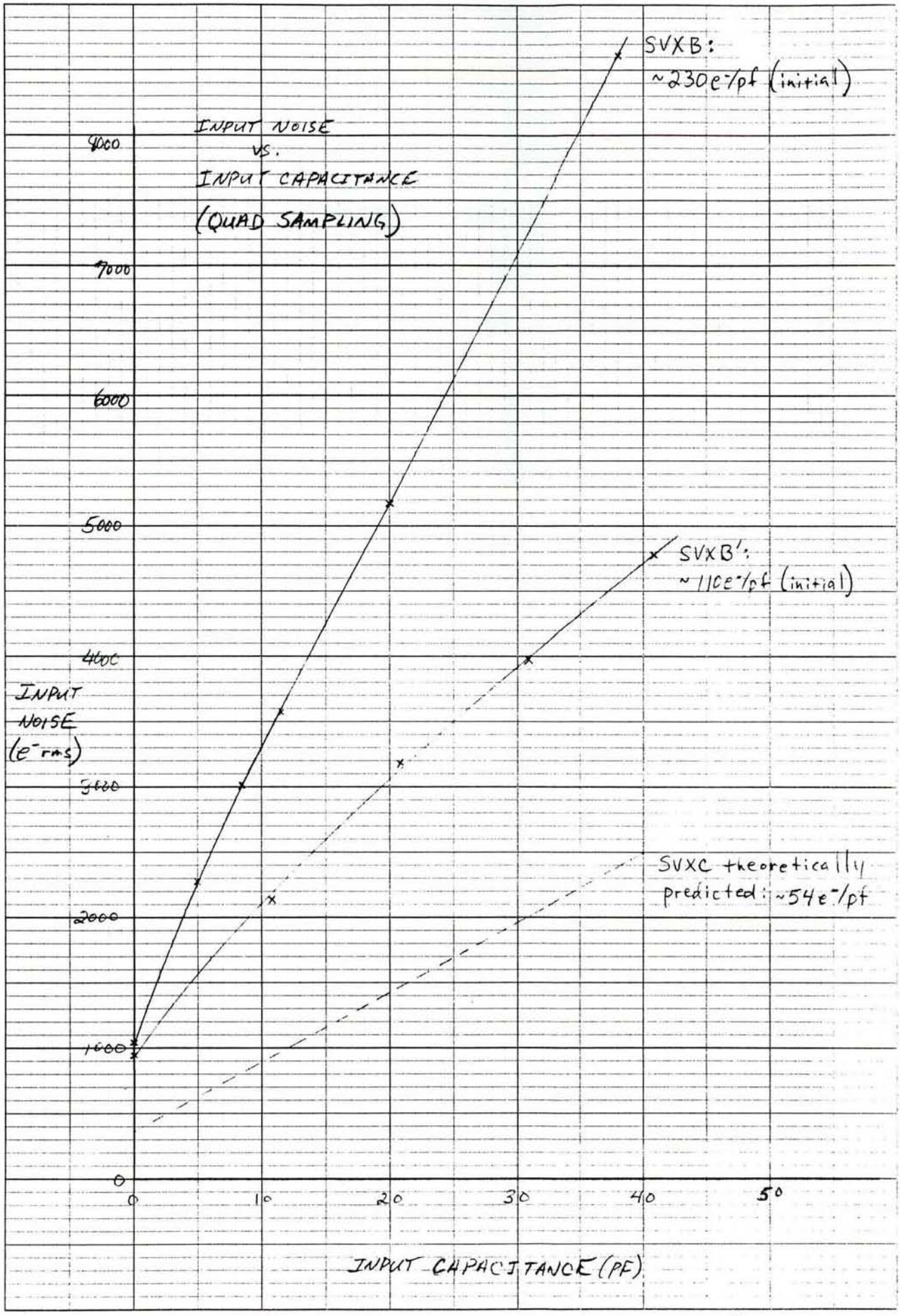

FIG. 8