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A 65 nm CMOS four-channel readout ASIC for ATLAS Muon Drift Tubes: 5–100 fC detection, 15 ns peaking time, and 8 mV/fC sensitivity

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Abstract: This paper presents the design and performance of a four-channel readout electronics system for the ATLAS muon chamber (MDT) to detect and measure charges resulting from proton-proton collisions. The design emphasizes speed, robustness, and efficiency in both area and power. Each channel comprises a charge-sensitive preamplifier (CSP), a shaper, a discriminator, and differential low-voltage signaling drivers. The analog channel exhibits a peaking time of 15 ns with a 60 pF detector capacitance and 4 ns without the detector capacitor. The circuit demonstrates linear sensitivity of 1 mV/fC at the CSP output and 8 mV/fC at the shaper output. Charge information in the range of 5–100 fC is extracted via time-over-threshold (ToT) decoding. Implemented in 65 nm CMOS technology, the design operates at a 1.2 V supply voltage.

Keywords: Analogue electronic circuits; CMOS readout of gaseous detectors

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1 Introduction

The ATLAS detector at the Large Hadron Collider (LHC) employs Monitored Drift Tube (MDT) chambers as the precision tracking subsystem in its Muon Spectrometer, enabling high-accuracy muon momentum reconstruction via track curvature in a magnetic field [1]. The upcoming High-Luminosity LHC (HL-LHC) Phase-II upgrade will increase luminosity by an order of magnitude, elevating event rates, pile-up, and radiation levels [1], thereby challenging the existing MDT readout electronics [2, 3], which are based on a bipolar Amplifier-Shaper-Discriminator (ASD) architecture with dual operation modes. This design imposes dead times of up to 750 ns due to bipolar undershoot, causing baseline shifts and limiting charge-processing rates.

To mitigate these issues under HL-LHC conditions, a new architecture is proposed, featuring a single operational mode with Time-Over-Threshold (ToT) for simultaneous extraction of timing information (from the leading edge) and charge information (from the pulse width). This approach minimizes dead time, enhances pile-up rejection, and improves rate capability. The circuitry is implemented in 65 nm TSMC CMOS technology with a 1.2 V supply, offering a compact layout, low power consumption, radiation tolerance, and scalability for sustained HL-LHC performance.

Section 2 describes the CMOS readout architecture in detail, and section 3 presents the measurement results of the prototype implementation.

2 Read-out electronics circuit implementation

The readout ASIC is a four-channel device. Each channel, as shown in figure 1, comprises an analog and a digital section. The analog front end includes a charge-sensitive preamplifier (CSP) followed by a two-stage differential shaper operating in a bipolar scheme to minimize baseline shift at high rates. The CSP converts input current pulses into voltage signals, which are amplified and shaped before being sent to a discriminator. The discriminator compares the signal to a threshold (typically 3–5σ above the noise level) and generates a digital output carrying timing information. A key enhancement in this design as compared to [4] is a dedicated buffer at the CSP output, enabling real-time monitoring of the internal analog signal without affecting front-end operation. This feature allows direct evaluation of CSP performance, including gain, timing, linearity, noise, and baseline behavior.

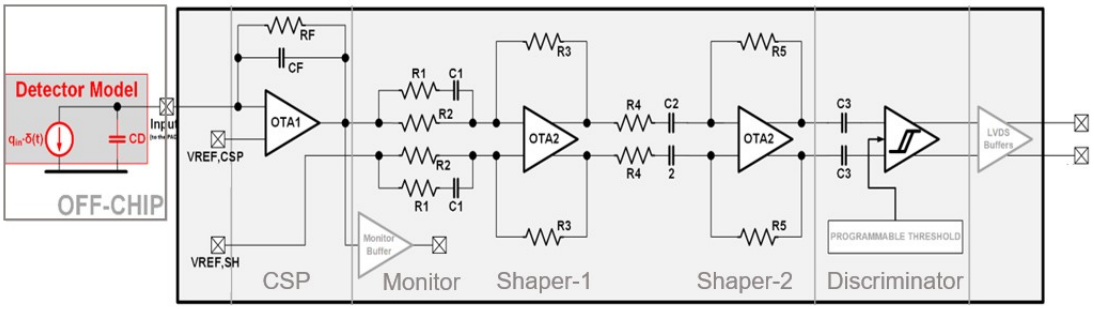

Figure 1. Read-out electronics generic block scheme.

2.1 Charge sensitive preamplifier

The charge-sensitive preamplifier (CSP) in the readout ASIC represents a cornerstone of the analog signal-processing chain, engineered to deliver an exceptional signal-to-noise ratio (SNR) and a rapid response to input charge pulses while maintaining ultra-low noise and minimal power dissipation, which are critical requirements for high-rate muon detection in the HL-LHC environment.

Implemented as a two-stage, single-ended amplifier topology, the CSP prioritizes power efficiency over fully differential alternatives, which incur higher current consumption without commensurate benefits in this application. Noise performance is optimized through careful sizing of the input transistor pair, featuring large channel dimensions ($W/L = 580\,\mu m/330\,nm$) and a nominal bias current of 1.475 mA, deliberately placing the devices in the subthreshold regime to achieve a high transconductance of $g_m = 25\,mA/V$. This strategy, widely adopted in low-noise CSP design, maximizes the g_m/I_D efficiency and reduces thermal noise [5] at the expense of modestly increased power consumption, a trade-off validated for the demanding MDT readout specifications.

Further power reduction is achieved by minimizing the number of stages in the channel and scaling the supply voltage to 1.2 V from earlier 3.3 V designs, enabling compact integration in 65 nm CMOS technology while ensuring radiation tolerance and sustained high-rate operation.

The CSP transfer function can be approximated by the following equation:

$$T(s) \approx \left(\frac{-R_F(s \cdot \tau_z - 1)}{(s \cdot \tau_0 + 1)(s \cdot \tau_1 + 1)} \right) \tag{2.1}$$

where $\tau_z = \frac{C_F}{g_m}$ and $\tau_0 = \frac{C_D}{g_m}$

2.2 Two stage bipolar shaper

The CSP output is filtered by a two-stage shaper, converting the CSP output pulse into a bipolar signal. Each stage uses a two-stage differential amplifier, transitioning from single-ended at the CSP output to differential in the shaper for high power-supply rejection [6]. The transistors of the input differential pair operate in the subthreshold region and exhibit a transconductance of $g_m = 2.5\,mA/V$. The choice of a two-stage amplifier topology, in addition to improved robustness to load, enables a large output voltage swing. The transistors in the second stage of each amplifier are designed with an overdrive voltage of less than 100 mV, providing a linear response up to 1 V.

Each shaper block incorporates an input impedance network and a resistive feedback network, as shown in figure 1, to implement the required poles and zeros for bipolar pulse shaping. Equations (2.2)

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and (2.3) present the transfer functions of Shaper 1 and Shaper 2, respectively.

$$T(s) = \frac{R3}{R1}\left(\frac{1 + sC_1(R_1 + R_2)}{1 + sC_1R_2}\right) \tag{2.2}$$

$$T(s) = \left(\frac{sC_2R_5}{1 + sC_2R_4}\right) \tag{2.3}$$

The four-stage shaper in design [2, 3] utilized large capacitors, which occupy large area on the chip. For area efficiency, along with minimizing the number of stages, sizing of the shaper passive elements are revised in this design and are reduced by a 4× ratio.

2.3 Time-Over-Threshold discriminator with progrmable threshold

The output of the analog signal processing chain is AC-coupled to the discriminator through coupling capacitors, where it is compared against a programmable threshold level to generate the corresponding digital ToT output pulse. The discriminator employs a comparator implemented using a two-stage single-ended amplifier topology without compensation. The architecture consists of a high-gain amplification stage followed by a chain of digital inverters, which converts the amplified analog signal into a rail-to-rail digital output depending on the relative levels of the input signal and the applied threshold.

The comparator threshold is set differentially using two independent 8-bit string digital-to-analog converters (DACs) in combination with 3-to-8-bit decoders. This configuration allows the threshold to be programmed up to 256 mV around the common-mode voltage, with a resolution of 2 mV per LSB. Each DAC is implemented using a main-string and sub-string structure, enabling finer voltage division and achieving an effective resolution of 1 mV per step. Complementary CMOS switches are employed to select the desired DAC output voltage and apply it to the comparator input.

3 Measurement results

The design performance is validated by extensive post-layout simulation followed by lab measurements with input charge (QIN) in the full range 5 fC÷100 fC. To realize the real experiment environment, a 60 pF detector capacitor has been assumed as part of design.

The input charge is swept from 5 fC to 100 fC, and the corresponding output of the CSP are measured, as shown in figure 2(a). The CSP demonstrates a peaking time of 15 ns and a sensitivity of 1 mV/fC, exhibiting linear behaviour up to the maximum tested input charge of 100 fC (i.e. 100 mV0-PEAK pulse). The CSP has a 5/100 fC input charge range at 0.89 fC Equivalent Noise Charge (resulting in 15 dB SNR at 5 fC Input charge).

The CSP is followed by a shaper implementing bipolar waveform shaping. Post-layout simulations in figure 2(b) show the bipolar response, with a baseline recovery time of <350 ns, shorter than in [2, 3], enabling prompt recording of subsequent charge pulses. The sensitivity of Shaper 1–2 is 8 mV/fC, and the maximum output swing reaches up to 800 mV for an input charge of 100 fC.

As the input charge increases, the corresponding Time-over-Threshold (ToT) pulse width varies from 13 ns to 25 ns, corresponding to a time-domain dynamic range of 12 ns. The discriminator output pulse width as a function of input charge is plotted in figure 3. The ToT pulse encodes two pieces of information: the leading edge indicates the charge arrival time, while the pulse width represents the amount of detected charge.

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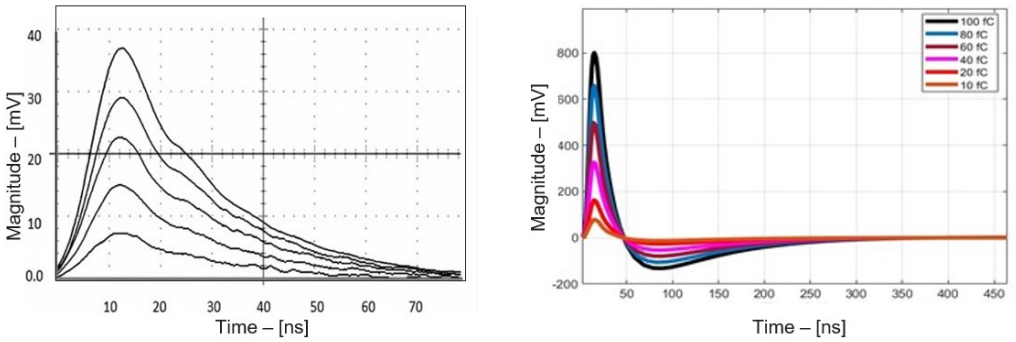

Figure 2. (a) CSP transient response for 10–50 fC charge (b) transient response of shaper.

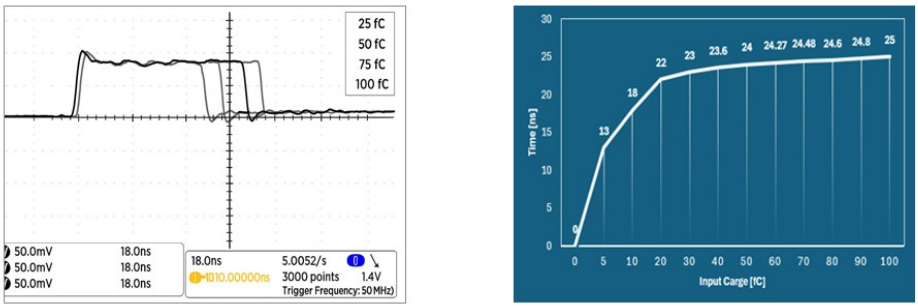

Figure 3. (a) ToT pulse for 25–100 fC charge (b) ToT pulse width VS input charge.

Figure 4(a) illustrates the output rate, defined as the number of pulses per second at the discriminator output, when the channel is periodically stimulated with a an input pulse every 1 µs. The output rate reaches its maximum when the threshold is set to a code value of 127, corresponding to a threshold voltage of 25 mV. This level is approximately five times higher than the shaper output noise (5 mV_{RMS}), ensuring reliable discrimination. Under these conditions, the measured output rate closely matches the input pulse rate at a threshold of $5\sigma_{noise}$, where σ_{noise} denotes the standard deviation of the shaper output noise.

As shown in figure 5, the readout ASIC comprises four channels, making the evaluation of inter-channel mismatches essential. This is performed using threshold scanning, in which the discriminator threshold is swept while a fixed input charge is injected and the corresponding output response is recorded. Figure 4(b) shows small channel-to-channel variations at low input charge levels, which progressively decrease as the injected charge increases.

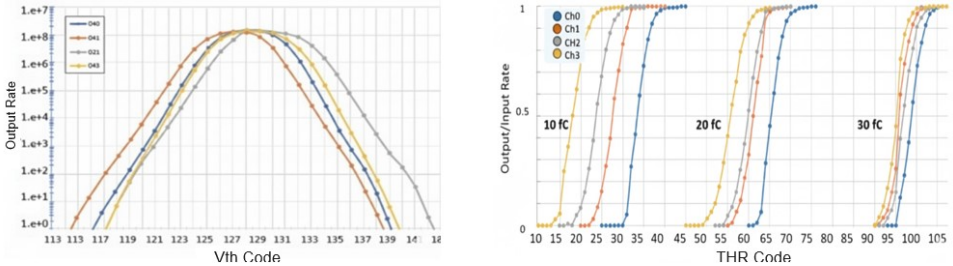

Figure 4. (a) output rate vs. threshold voltage (b) threshold scan for 4-channels.

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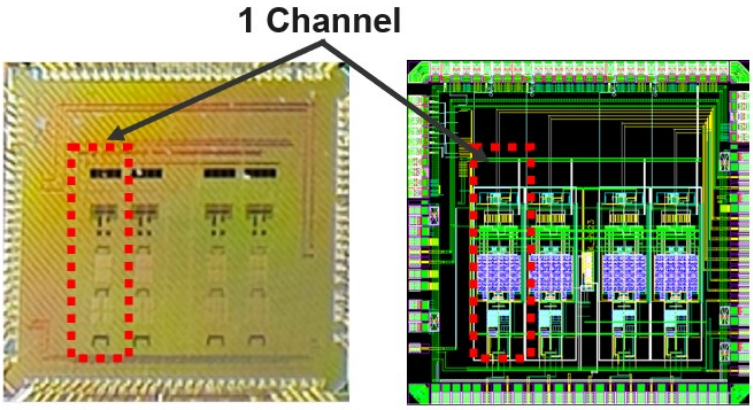

Figure 5. Chip photo and design layout of area 4 mm^2.

Table 1. State-of-the-art comparison.

Parameter	This work	[2]	[3]
Technology	65 nm	130 nm	500 nm
Channel Area	0.235 mm^2	0.4 mm^2	—
Supply Voltage	1.2 V	3.3 V	3.3 V
Channel Power	12.8 mW	33 mW	36.3 mW
Detector Capacitance	60 pF	60 pF	60 pF
Shaping Function	Bipolar	Bipolar	Bipolar
Input Charge	5–100 fC	5–100 fC	5–100 fC
Signal Peaking Time	14.6 ns	15 ns	15 ns
Sensitivity	8 mV/fC	14 mV/fC	8.9 mV/fC
SNR	15 dB	15 dB	10.9 dB

4 Conclusion

A four-channel readout chip for ATLAS MDT detectors is presented, along with its measurement results. The design is implemented in TSMC 65 nm CMOS technology, targeting power- and area-efficient operation while preserving the performance requirements of the ATLAS MDT system [2, 3]. Through architectural optimizations and technology scaling, the proposed channel achieves a 57.4% improvement in power efficiency and occupies only 58.75% of the silicon area compared to the previous implementation [2], as summarized in table 1.

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