A High Speed, High Gain Preamplifier System for Silicon Strip Detectors

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Abstract

A high speed, high gain amplifier system has been designed for silicon strip detectors. The amplifier has been designed using a semicustom bipolar linear array. This paper focuses on a practical integration of this amplifier into a working system. To maximize board density and reduce cost a new, relatively inexpensive custom chip carrier was designed. The design approach could be useful for other custom or semicustom chip designs. Insight into the design of a 128 channel preamplifier circuit board for low noise and low crosstalk using the new carrier is presented.

High channel density presents challenges in cabling. A relatively new high density cable with mass termination capability was used for transmitting signals from the preamp to the discriminator boards. As a part of the overall design, the approach taken for shielding of the detector, preamplifier cards, and output cables is discussed.

Introduction

The amplifier described in this paper is part of a high speed silicon strip detector readout system being developed at Fermilab [1]. This system will be used by two experiments, E-771 and E-789, in the 1990 fixed target run. Both of these experiments will operate at very high interaction rates with the goal of accumulating for study large samples of B particles. Each of these experiments will contain more than 10000 channels of silicon strip electronics. Although this paper is generally applicable to both experiments, the requirements for E-771 will be used as a specific example.

Front End System

The silicon strip detector for E-771 is comprised of 24 planes of silicon, each with 688 strips. Plane to plane spacing averages 0.5 inches. Signals from a silicon plane are fanned out over fine pitch circuitry on flexible Kapton to six high density connectors for preamplifier cards. Each preamplifier card has provision for 128 channels and has differential outputs for each of the channels. Thus there are 256 output signals per card. Outputs from a preamp card are transmitted over four fine pitch ribbon cables which are about 20 feet long to discriminator circuits housed in FASTBUS crates.

The preamplifier packaging design was driven by a need to minimize the Kapton length and reduce the associated capacitance in order to improve the signal to noise performance of the system. Since the silicon planes are physically close together, a circuit board which could be mounted on nearly the same pitch as the silicon planes was designed. The size of the circuit board, the pitch of the pins on the preamplifier chips, the choice of input and output connectors, and choice of output cable were all driven by the desire to place the preamplifiers close to the silicon planes.

Another design criterion was that preamplifier cards be easily replaceable and repairable. These factors influence the type of input and output connectors used and the construction of the preamplifier board.

To achieve the desired goals, an integrated design of the front end electronics was implemented. The integrated design in this context means considering the chip design, chip packaging design, board design, heat dissipation, and shielding design all at the same time.

Preamplifier

The preamplifier response for a charge impulse is required to be 20 to 40 ns baseline to baseline and have an equivalent input noise of less than 1800 electrons RMS. To achieve the design in a physically small package with reasonably fast construction time, a semicustom, bipolar chip was designed using the Tektronix Quickchip 2S linear array. Four channels of the preamplifier are designed on a single die. The design and performance of this preamplifier chip is covered in another paper presented at the 1989 Nuclear Science Symposium [2].

The preamplifier chip was designed to maximize the isolation between input and output pads by locating the pads far apart and to make power supply busing across many chips easy. Figure 1 is a bonding pad diagram which shows that the inputs and outputs are on opposite ends of the chip to reduce feedback. Power supply connections are made on the sides of the chip to permit power busing under the chip. Identical power connections are made on each side of the die to facilitate the mounting of the chips in the chip carrier package which was chosen.

Chip Packaging

Each circuit board is to have 128 channels and thus 32 four channel dies mounted on it. To fit the chips onto the preamplifier board, the chips had to be mounted relatively

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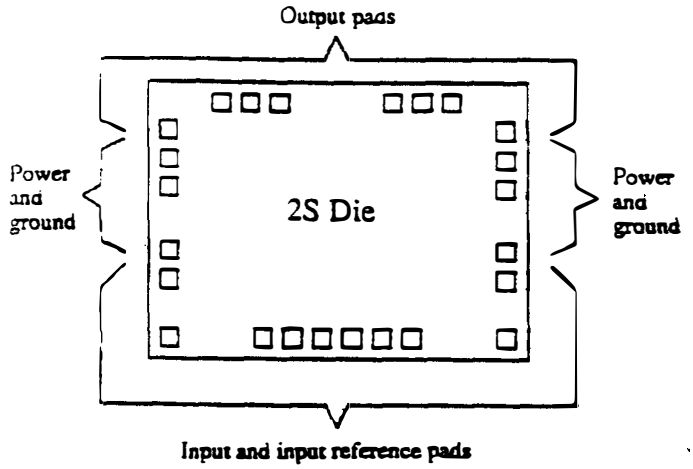

Figure 1 - Preamplifier Die Bonding Pads

close to each other. Chip on board (COB) mounting of the bare dies was considered to be impractical because of the large number of dies to be mounted. Secondly, COB does not readily permit replacement of a bad die after assembly. Thus a chip carrier was desired which would facilitate replacement of bad chips. To fit the required number of channels onto a board, a leadless surface mount chip carrier with a pitch of 25 mils was necessary. Standard packages which would meet the space requirements were not available. Therefore a custom package was designed.

The type of package designed is manufactured by Tectonic, Ltd in England and sold under the trade name of EPIC [3] by S A Communications of San Diego, CA. Advantages of the package in addition to full choice of package dimensions include ease of design, fast delivery, and relatively low cost. The primary disadvantages are that the package is not well sealed and replacement of a faulty device requires special care.

The EPIC chip carrier is made of B-T (bismaleimide-triazine) which is similar to the FR-4 material that is commonly used to make printed circuit boards. Thus, there is no temperature coefficient mismatch between the package and the printed circuit board to cause solder joint

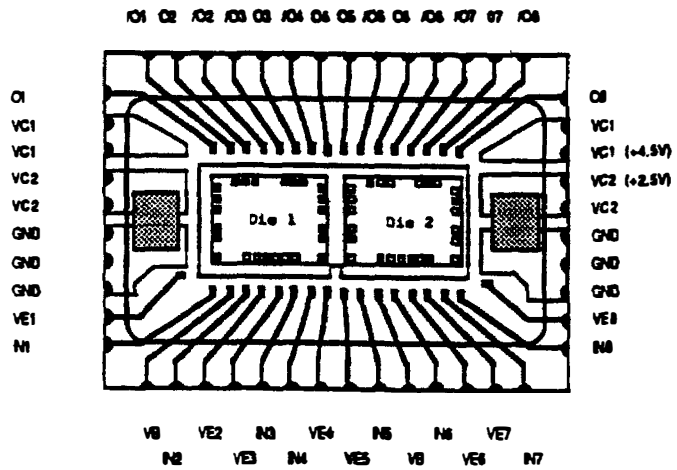

Figure 2 - Custom EPIC Chip Carrier Layout

failure problems. The glass transition temperature for B-T, however, is about 210°C, which makes it more suitable for gold ball bonding and surface mount reflow soldering.

To make most effective use of the space on the circuit board and reduce the packaging cost, the package was designed to have space for two dies (eight channels of preamplifier). The package was ordered by sending the layout shown in Figure 2 to the manufacturer's representative in the USA. Chip carriers were normally returned in about 4 weeks. As can be seen, provision was made inside the chip carrier for 2 internal bypass capacitors for critical power supply voltages. This feature was very helpful in preventing the output drivers on the chip from oscillating. Effectively, the assembled chip carrier becomes a mini hybrid with surface mount provisions. Figure 3 shows an assembled chip carrier with the lid removed.

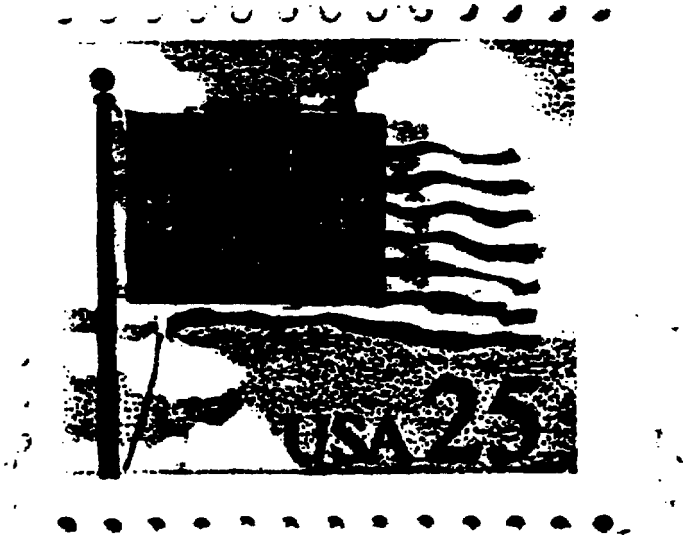

Figure 3 - Assembled EPIC Chip Carrier with Lid Removed to show 8 Preamplifier Channels.

The EPIC type of package has received only limited attention in the USA. However, the package has been extensively tested and used by British Telecon in the United Kingdom. Accelerated life tests performed by the manufacturer show the package to be highly reliable.

A preliminary measurement of the thermal impedance of the EPIC package to the circuit board described in the next section is about 80°C/watt. The preamplifiers dissipate about 350 mw per EPIC package.

Due to the inherent construction of the EPIC packages, they are not well sealed against moisture. To provide adequate protection, the chip surfaces must be coated or sealed to prevent contamination of the bonding pads. Two different materials have been tested on the preamplifiers. One is a polyimide surface coating (Rely-imide #210D) made by M & T Chemicals and the other is a glob top encapsulant (FP4323) made by Hysol for COB applications. Packages with both types of coating were thermally cycled. Packages with heavy coats of the polyimide material that covered the bonding wires (not recommended by the manufacturer) showed damage to the bonding wires after several days of thermal cycling. Similar

tests performed with thin coatings, 1-2 mils, and no coating of the bond wires showed no damage. The encapsulant material has shown no problems. Both materials when properly applied appear to be acceptable solutions to the moisture problem.

Initially, poor wire bonds to the package were encountered when using a gold wire bonder. This was apparently due to thin gold plating (8 to 15 microinches) inside the carriers. After ordering packages with a minimum of 32 microinches of gold, the problem disappeared.

Solder mounting and replacement of the EPIC packages requires special attention. Production assembly was accomplished with IR solder reflow techniques. Because of the fine pitch components, stencils rather than screens were used to deposit the solder paste. Special fine mesh solderpaste with low slump characteristics was necessary. Replacement of a single EPIC package by an experienced person requires about 10 minutes.

The EPIC package is relatively inexpensive for a custom package. Nonreccuring engineering charges are about $1500 and the cost per package is $1.06 for a few thousand pieces.

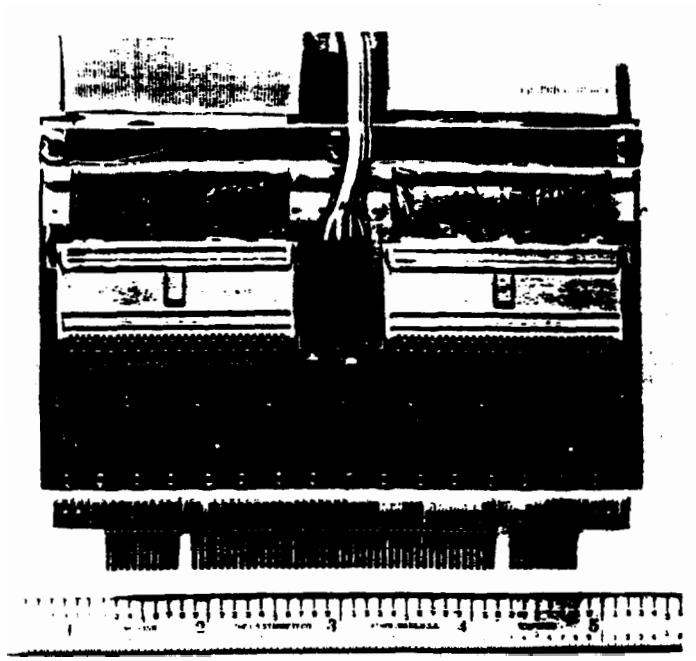

Figure 4 -128 Channel Preamplifier Card With Connectors.

Board Layout

As has been mentioned, the printed circuit board and the chip carrier are an integrated design. Each printed circuit board which is 3.5 inches by 4.5 inches has 128 channels of preamplifiers. Seventy percent of the board space is devoted to input and output connectors. Eight chip carriers are mounted in a row on each side of the board. Power is brought into the center of the board with a cable and then distributed under the chips on each side of the board to minimize voltage drop. Power supply bypassing is done as close to the chip carriers as possible.

The circuit board has four layers. The center two layers are primarily ground plane, and act as a low impedance amplifier reference. They also provide impedance control for the output traces. Each channel of amplifier has a dedicated reference, or Vee, connection. Each four channel chip has a common ground connection for the output driver pulldown resistors on the chip. It is important that these all connect directly to the same low impedance reference, or ground plane, to reduce crosstalk. In fact, the common pulldown resistor ground connection is made through three parallel package pins to insure a low inductance connection to the board. Multiple vias are used to connect the chip ground pins to the ground planes in the center of the board. All bypassing is as tight as possible to the ground plane.

The ground plane layers also distribute the heat from the chips to the entire board. The board thus tends to act as a cooling fin. There are 144 circuit boards distributed over four sides of the detector. Forced air is used to cool the circuit boards.

Figure 4 shows an assembled card. Input signals are brought onto the card from the detector via an inexpensive, 132 pin 50 mil pitch card edge connector. This connector permits easy insertion and extraction of 128 channels of electronics with less than 10 pounds of force. Two 64 pin, high density connectors on each side of the card are used to send signals to the discriminator boards.

Shielding Design

A double RF shield is employed around the detector as shown in Figure 5. The inner shield encloses all of the silicon strip detector planes. Penetrations are made through the shield for the preamplifier cards to pass through and plug into connectors mounted on the detectors inside. Small beryllium copper RF gasketing strips are used to make contact from the shield to the exposed ground plane on the two sides of the preamplifier card near the card edge connector. See Figure 4. The RF shield is carried through the circuit card by means of a series of via holes located where the gasketing contacts the board. This arrangement maintains RF shield integrity which would have been reduced by the card slots. Also, this allows a very low impedance connection between the RF shield and the amplifier grounds. This was found to be absolutely essential in eliminating coupling between the preamplifier input leads coming from the detector and the higher signal level preamplifier outputs.

A second RF shield is placed around all of the preamplifier cards and the inner RF shield. Power supply leads for the preamplifiers are brought through the outer shield in four locations and then distributed. The outer shield eliminates pick up on the power distribution cables.

Preamplifier output cable bundles passing through the outer RF shield are shielded to reduce pick up on the cables. The bundle shields are terminated to the outer RF shield at the detector to effectively extend the outer shield to include the cables. The bundle shields are also connected at the receiving end to the FASTBUS crate racks.

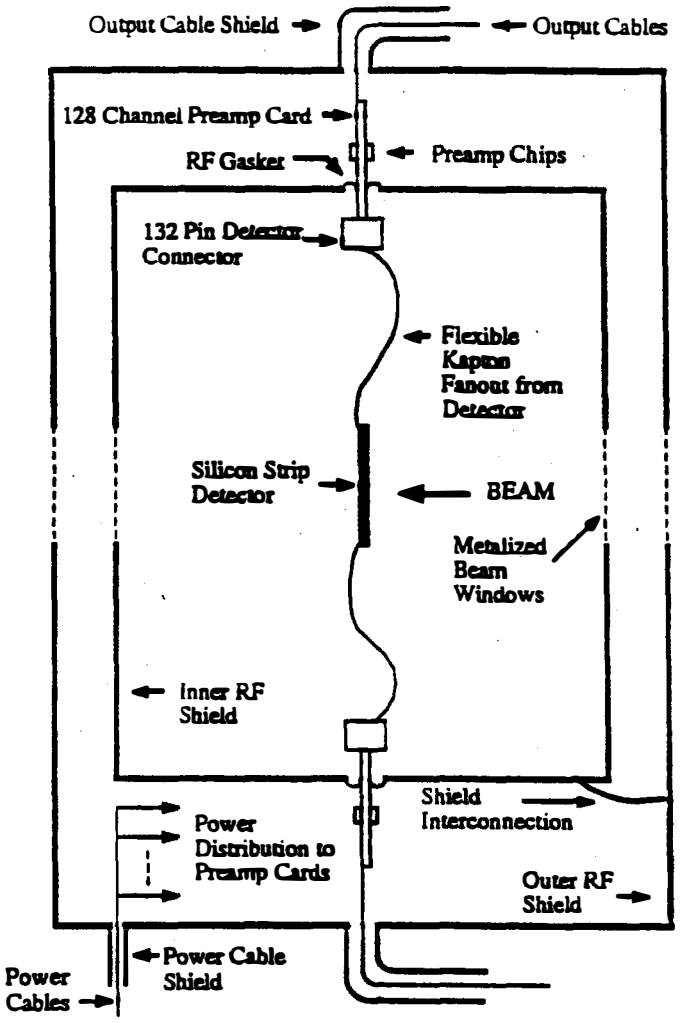

Figure 5 - Silicon Strip Detector and Preamplifier Card Shielding

Output Cables

A mass terminable, flexible, 64 conductor, 25 mil pitch ribbon cable was chosen to transmit the large number of signals at the output of each preamplifier card to the discriminator cards. The cable which is made by Spectra-Strip (#133-3013-064) has an embedded ground plane for impedance control and cross talk reduction. All wires in the cable are used as signal conductors.

Four of the cables are connected to each preamplifier card, for a total of 576 cables in the system. Each cable is relatively light weight, flexible, and stacks well into bundles for shielding.

For this application, pairs of conductors are driven differentially. The differential impedance of the cable is 100 ohms. Although the output signals are differential, the ground plane of the cable is connected to the preamplifier ground plane to provide a return path for imbalanced signals. Also, fixing each cable ground plane to the same reference reduces coupling which can cause oscillations. To make the connection to the preamp ground plane, the ground plane on the cable is folded back and wrapped with conductive adhesive copper tape and then clamped to the preamplifier ground plane as shown in Figure 4. In addition to making the ground connection to the circuit board, the clamp also doubles as a cable strain relief.

At the receiving end, each signal conductor is AC coupled and terminated with 50 ohms to a common po which is connected to ground. Forward cross talk between adjacent conductor pairs in the cable is about 0.5% for a ten foot cable with 5 ns rise time pulse. This is quite acceptable for the silicon strip application.

Preamplifier Power

A "quiet power" source is provided for the preamplifier cards to eliminate noise injection from the power source. A separate double shielded transformer is used to provide AC power to the preamp power supplies. Only linear power supplies are used for the preamps. Power cables from the power supplies to the detector are shielded outside the RF shield and bypassed just inside the outer RF shield to stop any noise transmitted down the cables from entering the RF enclosure.

Once the Power supply voltages are brought inside the outer shield, they are distributed to the individual preamplifier cards by means of short ribbon cables. Each of the two power supply voltages on the ribbon cable to each card is fused. The fuses are located inside the outer RF shield. Easy access doors to the fuses are provided for maintenance purposes.

Summary

The front end electronics for the silicon strip detector i packaging problem as well as an electrical design problem. Both factors needed to be considered in the early design stages of the project to build a system which not only meets the electrical design criteria, but is manufactureable and readily repairable. In completing the design, packaging ideas which should be applicable to other systems were developed.

Acknowledgments

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