Eagle Internal Note
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RD2 : SILICON TRACKER AND PRESHOWER - TECHNICAL DESCRIPTION

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1. INTRODUCTION

The purpose of this note is to provide a technical description of the SITP which will be of use for detailed discussions of the integration of the detector in the design of an LHC experiment. More detailed results have been presented elsewhere [1]. We present our results in the context of the two existing designs, Eagle A and Eagle B, which both include a LAr electromagnetic calorimeter.

As has been demonstrated by previous studies, the material involved in a LAr design precludes the use of a preshower before the cryostat wall. However, the need for a preshower detector has been established by studies of photon identification, in particular for the $H^0 \rightarrow \gamma\gamma$ mode. This note therefore assumes that a cold preshower detector will be embedded in the LAr calorimeter. The SITP would then perform as an outer barrel tracker, used:

i) as part of a combined central tracker with other systems,
ii) as part of the electron identification by track preshower matching, and
iii) as part of the muon identification by providing the crucial measurement of the muon entry point to the calorimeter material.

In the event of a warm EM calorimeter being the preferred option as in EAGLE C, the SITP layout can be easily reconfigured to provide a precision preshower layer (see the original SITP proposal [2]). Many studies have in fact been made with this configuration.

Performance figures in this note are given for the SITP tracker alone. The combined operation of the SITP detector with other detectors is discussed elsewhere [3]. The different detector layout of reference [3] represents an optimized layout for momentum precision.

Since the outer tracking is expected to be the last tracking layer to fail in a hostile LHC environment, redundancy of the electron and muon identification and momentum accuracy is crucial. We therefore think that the SITP design should not be compromised in an overall tracking optimisation.

2. DESIGN

An advantage of the SITP design is that considerable flexibility is possible in the granularity and radial position of each plane. For definiteness, a pair of designs are discussed here that are being studied in detail. We assume that the radial space from 65 to 115 cm is available for the outer tracking in the EAGLE A design. We are concerned that the EAGLE B design, for which the minimum outer tracking radius is 95 cm, leaves inadequate room for both a 6-layer tracker and a high-efficiency barrel TRD. Even if mechanically possible, reducing the radial space implies a loss of momentum resolution, and increased ambiguity levels in the matching between inner and outer track segments.

The EAGLE A tracker consists of 6 detector layers, arranged as 3 superlayers with radii 70, 85 and 100 cm. Each layer contains crystals that overlap in both ϕ and Z, giving hermetic coverage. The remaining 10 cm of free space will be occupied by a polythene moderator, which will be required to reduce the damage levels from neutrons, not only to the silicon detectors (see below for the radiation tolerance expected) but also to the electronics of all the detectors in the central cavity.

Two types of detector are foreseen, currently 2.4 cm square and of 250 micron thickness. Strip detectors have 64 strips with a pitch of 375 microns, while pad detectors have 64 square pads of 3 mm by 3 mm. The most recent design is shown in Figure 1. The strip geometry is likely to be of 200 μm strips on 5 cm crystals in the case of an outer-tracker layout. In this configuration, the strip detectors give measurements of r-ϕ with a 60 μm precision, and a Z precision of 15 mm. The pad detectors have a Z measurement precision of 1 mm, thereby reducing the overlap area for ambiguous hits. The tracker covers the Z range from -125 to +125 cm, giving a total silicon area of 80 square meters, with 8.7 million readout channels.

The Eagle B tracker consists of 3 superlayers as above, at radii of 97, 103 and 109 cm. This reduces the space available for a neutron moderator, but the polythene of the TRD radiator may in part compensate for this. The total silicon area is 97 m^2, with 10.8 million readout channels. These design parameters are forced upon us by the EAGLE B layout. Detailed mechanical studies are not complete, but it seems difficult to fit both the modules and the required services into this small radial space. An increase in the radial

space would result in a large cost increase of the EAGLE detector. Moving inwards would compromise the TRD efficiency.

The material per layer would be around 1.5 -2% of a radiation length (4% per superlayer, 12% total) at 90°, if a conventional copper multilayer board readout is used. It may be possible to substantially reduce this figure if novel fibre-based readout schemes can be used. Such schemes are under investigation.

3. PERFORMANCE

One great advantage of silicon detectors is their high efficiency, measured in test beams to be >> 99% for tracks crossing 250 microns of material. One must nonetheless design for some inefficiency due to bad electronics channels, or connection problems. In addition, activity near tracks, created by secondary processes in preceding material, can render some space points useless. For these reasons our benchmark design contains 3 superlayers, each measuring both ϕ and Z. This allows a track vector to be reconstructed in the event of a point being lost.

Studies have been made for both the EAGLE A and EAGLE B designs, assuming in both cases that the inner tracker contains 4% of a radiation length of material.

For isolated hadrons, the momentum resolution using the outer tracker alone with 3 layers of 200 micron strips and a transverse vertex precision of 20 microns, is respectively

$$dp_t/p_t = 1.1\ p_t\ (\text{TeV}) \oplus 0.004\ \sqrt{(\sin\theta)}$$
$$dp_t/p_t = 2.2\ p_t\ (\text{TeV}) \oplus 0.011\ \sqrt{(\sin\theta)}$$

for the EAGLE A and B designs, where the second term in each case is the multiple scattering contribution added in quadrature. With an improved momentum measurement using as well the inner tracking detector, the momentum resolution of Figure 2 is achieved [3]. Although the momentum resolution is considerably improved by combining the information of all tracking detectors, the resolution is adequate using the SITP detector alone.

While the tracking efficiency for isolated hadrons is close to 100%, the presence of material significantly deteriorates the identification and measurement capability for low-p_t electrons. Table 1 shows the efficiency of electron identification using a configuration similar to that of EAGLE A. A mono-energetic electron is traced through the full apparatus. The calorimeter energy is then reconstructed as a cluster (80 MeV cell cut)

using an adjacent-side algorithm, and an rms radius evaluated. A search is then made for reconstructed tracks pointing to the cluster. Given the following 3 cuts:

i) a requirement on the cluster radius of less than 1 cell unit in both the η and ϕ directions [isolation cut, cut a],

ii) a requirement that the reconstructed calorimeter energy is reconstructed to within 3 σ of the peak energy assuming a calorimeter resolution of 0.1 $\sqrt{(E)}$, [correct-energy cut, cut b]

iii) the reconstruction of a unique 5- or 6- point track pointing to the cluster within a window of $d\eta \times d\phi = 1.5 \times 4.0$ cell units about the cluster centroid [track-cal match, cut c].

CUT	Energy (GeV) 10	40	η
a	96	99	0.
	.92	.99	1.2
a+b	.94	.99	0.
	.88	.98	1.2
c/a+b	.99	.99	0.
	.98	.99	1.2
a+b+c	.93	.98	0.
	.86	.97	1.2

The main loss results from accompanying (correlated) track activity caused by up-stream material. In the EAGLE B design the presence of TRD material affects the efficiency. For 10 GeV tracks at rapidity 1.2 (the end of the SITP acceptance) the efficiency is 80% for cuts (a+b+c).

Electron bremsstrahlung in the inner material also causes a deterioration of momentum resolution. Figure 3 shows the reconstructed inverse p_t for generated 10 GeV p_t electrons at $\eta = 1.2$, in each design. As shown in Figure 4, there is a strong correlation

between the extrapolated track distance from the centre of the reconstructed calorimeter cluster, and the reconstructed track momentum. The data are shown for 10 GeV at $\eta = 1.2$, before and after the energy cut. At some expense of efficiency, a clean electron sample is obtained.

4. ENGINEERING

Several engineering options are being considered to assemble crystals as a full-sized detector. One such option is described below. Issues being studied include :

i) the electrical and mechanical contact of the crystals and associated electronics, with a required crystal precision of less than 60 μm,
ii) the assembly of this motherboard on a support cylinder, and
iii) the electro-mechanical aspects of signal readout (see below).

Alignment will be needed to a level of less than 60 μm. Crystals shown in Figure 1 will be mounted (Figure 5) in a tile structure onto a circuit board (Figure 6). Nominally 64 counters are considered per board. The mask pattern of each crystal is known to better than 10 μm, and can be aligned with respect to known fiducial points to this level. These boards will then be mounted either directly on the support cylinder or onto intermediate modules of length 125 cm, using precision drilled holes, and checked by travelling microscope. In this latter case, the assembled modules would be mounted on the support during final installation. Finally a track based alignment will be used since the number of modules is small.

A double layer of counters (see Figure 6b) will be mounted on each side of the carbon fibre support sandwich (approx 1 mm equivalant carbon fibre), and the mass of each layer will be approximately 150 kg. The 3 support tubes will have reinforcement flanges at each end, and will be mechanically linked to maintain a static deformation of less than 1mm.

The major issue to be faced is not initial alignment but rather the alignment stability. This is especially crucial given the possibility of detector operation at low temperature to minimise the effect of bulk radiation damage in the detectors (see below). The board mounting must take account of thermal dilation, and the different expansion coefficients of component materials. Tests are planned to measure the reproducibility of a prototype after extended temperature cycling.

Cooling may be provided by circulating an inert fluor (for example Fluorinet FC72) through cooling pipes built into each module (Figure 5). The pipes have an internal

cross section of ~ 1 mm^2, and will directly contact the silicon crystals and the electronics chips. In the layout of Figure 5, silicon counter operation at -20° C is assumed with a maximum temperature difference of 10° C. Assuming a power consumption of 5 mW per channel, the estimated cooling power of 1 KW m^{-2} is twice that required. Prototype tests are in progress.

The full detector will be placed in a gas-tight volume circulated with dry nitrogen and insulated from external heat input.

5. ELECTRONICS AND READOUT

The electronics specifications of the main SITP detector chip foresee the following major elements (blocks) as shown in Figure 7:

i) A fast (< 15 nsec ristime) preamplifier operating in charge integration mode with an rms noise of < 1500 electrons. Good noise performance for detector operation (see below) of up to 10 μA.
ii) Storage of the charge on an analogue pipeline of up to 2 μsec (128 cells at a clock speed of 67 MHz). Stability and cell-to-cell uniformity of the pipeline that is small compared with a minimum ionising charge deposition, to avoid calibrations. Charge deposition over two 15 ns cells. Asynchronous read/write of the pipeline, with full skip and other control logic.
iii) A discriminator and sparsification block preceding an ADC.
iv) A final ADC and memory buffer block.

It is intended to place this functionality on a single chip of :

i) Up to 64 channels, with a 2 μsec pipeline length, and a chip size of the order 1 cm^2.
ii) A power cunsumption of 5 mW per channel.
iii) A final noise, using an SITP detector with a 5 μA current, of 10:1 for a minimum ionising signal when integrated over 2 time slots.

This detector, and we think all detectors of the tracking region, should have analog electronics if possible to enable realistic detector and event understanding. We require an ADC of approx 6-bit range for the tracker, but a much larger dynamic range is required for the preshower (under study for either the silicon or cold preshower options).

To achieve the design aims noted above, we are proceeding step by step with the successive electronics blocks. Significant progress has been reported during the last year [1], which is summarised below. Figure 8 shows the Sr^{90} signal at the output of a 4-channel chip prototype connected to a silicon diode, and operating at a clock rate of 67

MHz. Figure 9 shows the output signal (4 successive time slots) from a 32-channel prototype when charge is injected on one of the channels.

Existing chip functionality and performance	
Item	Performance
Sampling speed	> 67 MHz
Sampling time	2 times 15 ns
Noise	ENC < 2500 rms electrons (15 ns sample)
Analog memory	1usec length (64 cells)
Power	10 mW per channel
Size	32 channels on chip of 6×8 mm^2

The preamplifier and pipeline elements have been successfully merged with close to the required functionality and performance at the intended 67 MHz clock speed.

As already noted, we intend that all the functional blocks should be part of a single chip. The present emphasis is to reach the required noise and power specifications. Together with real-estate questions of the chip readout, those two issues items will finally determine the viability of the chip. A separate project [4] investigates the use of fibre optic readout from the board. The point of fibre-optic readout may be after either the preamplifier or ADC steps of our chip, depending on the performance of that project, and of our chip. It is necessary however that no analog signals be transferred via circuit board (copper).

A second major specification of our electronics is resistance to high radiation levels:

~ 10-20 Mrad charged particle radiation,

~ 2.10^{14} n cm^{-2} for neutrons.

Three possible radiation hard candidate technologies are being investigated (RD9, Saclay, RAL) for the SITP detector. They are the HSOI13HD process of Thomson-TMS (RD9), the DMILL process of Saclay, and the bulk Cmos Harris process being investigated by RAL (see radiation section).

It is intended that the full SITP data be available for a second level trigger. In the case of the mechanics structure described above, a chip would be mounted behind each silicon crystal. Each motherboard would be electrically independent, with digitised signals from each chip being serially transferred via the circuit board to one or more memory buffers. The signals would subsequently be transferred via optical fibre to the data aquisition. The clock signals for each mother board would also be received via optical fibre. Both the electronic and detector bias voltages, however, must be distributed on the board. The trade-off between material thickness and electronics flexibility is now starting to be addressed.

6. SECOND LEVEL TRACK TRIGGER

The outer silicon detector can be used to provide a second level trigger on high P_t charged particles. This will be important for the electron trigger as the calorimeter electron trigger will tend to select π^0 dominated jets. Therefore false electron candidates can be removed by demanding the presence of a high P_t charged track pointing to the calorimeter trigger cluster. The high pt track trigger can also be used to help trigger on muons and taus.

This trigger study has been performed with a design for EAGLE A which differs slightly from the benchmark, by including an extra layer of r-ϕ strips at the expense of one layer of pads. This has the advantage of improving the pattern recognition and redundancy for the momentum measurement, at a cost to the Z resolution in the case of inefficiency. The best optimisation of the final setup will have to take into account the performance of the trigger, and of the global pattern recognition.

A high p_t track trigger has been simulated using Geant. The algorithm requires at least three out of four hit r-ϕ strip planes in a road. The road is defined by a width of $2\pi/2064$ radians in the r-ϕ plane. This is equivalent to a trigger threshold of about 20 GeV/c. To keep the occupancy low roads are constructed out of 40 overlapping Z slices.

The efficiency for isolated electrons a function of p_t is shown in Fig 10. The effect of high luminosity running was allowed for by adding an average of 10 minimum bias events to each electron. The trigger shows a reasonably sharp threshold at 20 GeV/c. The rejection power of the trigger against jets passing the level 1 calorimeter trigger is currently being studied.

The trigger could be implemented in either fast processors or if this solution required too many processors it could be done in hardware in a similar way to the ZEUS first level track trigger.

7. RADIATION HARDNESS OF DETECTOR AND ELECTRONICS

The expected damage due to neutrons is several orders of magnitude greater than that caused by charged particles, and our initial efforts have investigated neutron irradiation to levels beyond those calculated to be reached in Eagle at the proposed SITP radius, which corresponds to positions 1, 2, and 3 in configuration 6 of the calculations of Ferrari, Sala, Fasso, and Stevenson [5]. The predicted neutron fluxes, believed to be reliable to to within a factor 2, are in the range 2-4 10^{12} cm^{-2} yr^{-1} for the proposed rapidity range; this assumes a 10 cm. thick neutron moderator which reduces the fluence in the relevent energy range by a factor 10.

The CV and IV characteristics of a silicon diode after neutron irradiation change in a complicated manner which is not yet fully understood. However we have shown that the devices can continue to work at LHC levels of irradiation. When the effective donor concentration N_{eff} is plotted against neutron fluence ϕ_n, the values drop to near zero and then increase again as shown in Figure 11. This is interpreted as an "inversion" of the material from n-type to apparent p-type. We have shown that there is a decrease in interpad resistance at the same time but that this is not sufficient to prevent the detector from functioning, despite the type inversion. The minimal value at depletion voltage is 10MOhm after an irradiation of 3.10^{13} n cm^{-2}.

The effect of the changes of donor concentration is mitigated by "self-annealing", which has been observed to have components which differ in time-constant from essentially infinite to a few minutes. This allows a detector to survive longer when undergoing the steady irradiation of an LHC operating period. Moreover we have established that the annealing takes place to the same extent when a detector which has been irradiated while cooled (e.g. -20° C) is subsequently warmed up. This would allow a detector which is cooled during operation to recover during relatively infrequent periods at room temperature and continue operation when cooled again.

Self annealing corrections are therefore necessary to predict the behaviour in real operation. At an operating temperature of -20° C most self annealing processes are frozen out, and so the detector will recover from radiation damage during scheduled shutdowns at room temperature. Using our measurements of the self annealing constants, we find that even one day of annealing at +20° C during an LHC year would be sufficient to maintain safe operation for at least 10 years of operation. This means that after 10 years of operation, we expect the detector leakage current at room temperature to remain under 1

microamp per pad, and the depletion voltage to remain less than 150V, without any special measures to warm the detector [6,7,8]. Figure 12 shows the depletion voltage estimated according to the following scenario:

i) Initial diodes of 5 KΩ cm with a thickness of 250 micron,
ii) A 100 day run per year, followed by 20° C annealing,
iii) A neutron dose per year of 5 10^{12}n cm^{-2}.

We note however the following caveats. The above results are for neutron damage alone, and ignore possible ageing effects. They also do not consider possible charge trapping effects at low temperature (these studies are under way).

An important factor is the implementation of the data acquisition electronics in a radiation tolerant technology (see section 5). Some of the basic structures for the RD2 electronics have been put on a radiation hard CMOS technology, as a joint effort with the RD9 project. This uses the film fil SOI (HSOI3HD) process (0.15 micron) of Thomson TMS. Some other CMOS technologies are good candidates to withstand the radiation levels inside the LHC detectors. Projects to develop rad-hard electronics for LHC also exist at RAL (CMOS technology) and CEA-Saclay (Dmill process). Similar rad-hard implementations are also intended in the RAL and CEA-Saclay programs.

8. COST

Our present estimate for the SITP electronics and read-out is 2 SFr per channel, including the processing of wafers in rad. hard technology which accounts for 50% of the total. There is an uncertainty in this figure related to volume production costs and to yield, which we shall continue to explore. We also assume a figure of 15 SFr. per cm^2 for the silicon detectors, a figure subject to similar uncertainties. On this basis, the following costings refer to the Eagle A (8.7×10^6 Si channels) and Eagle B (10.8×10^6 Si channels):

Item	Unit Price (kSFr.)	Number A	Number B	Cost(kSFr.) A	Cost(kSFr.) B
1. Rad-hard Front-end chips (64 channels)+	0.1	36k	168k	13600	16800
2. Boards (64 chips), logic, buffer memory and clock dist.	0.8	2.1k	2.6k	1700	2100
3. Data collection buffers (16 boards)	2.0	132	164	260	330
4. Clock and control dist.	-	-	-	500	500
5. Data signal transfer	-	-	-	1000	1000
6. Power supplies				350	400
7. DAQ, clock calibration, production test eqpt. etc.				600	600
8. Silicon pad detectors		136k	168k	12000	14550
9. Support structure and cooling				3000	3000
TOTAL				33010	39380

+ Current best estimate from discussion with Harris and Thomson.

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   A. Poppleton et al, EAGLE internal note INDET-NO-001 (1992).

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6. S.J. Bates. The development of a silicon detector for LHC, 1st year PhD report, Cambridge University, September 1991.

7. Minutes of the Dortmund SITP, radiation meeting, 26/11/91, SITP-TR-019.

8. R. Wunstorf et al, Results on Radiation Hardness of Silicon Detectors up to neutron dof 10^{15} n cm^{-2}. Talk given at the 5th Pisa Meeting on "Frontier Detectors for Frontier Physics", 1991, to be published in Nucl. Inst. Meth.

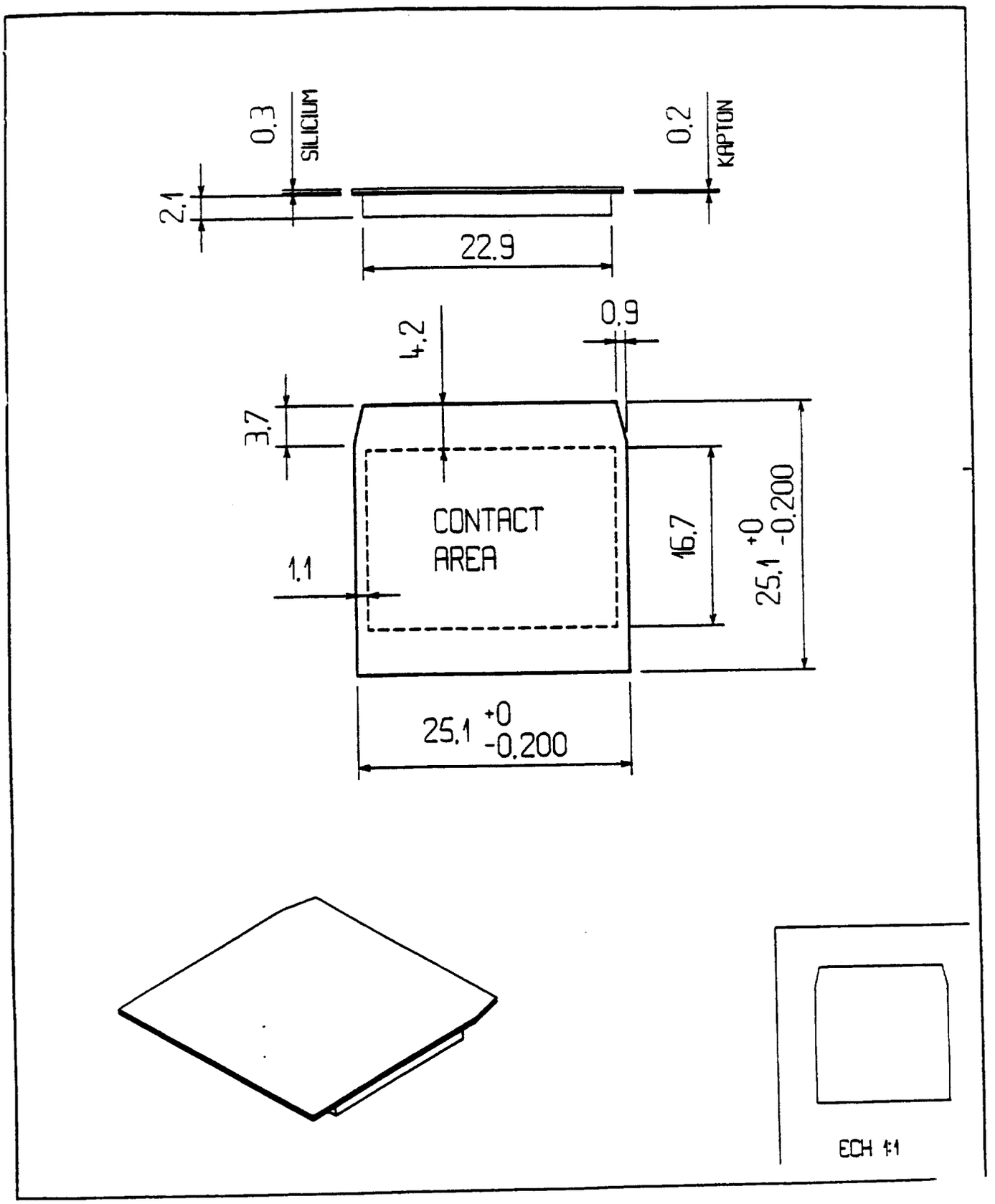

Fig. 1 Most recent geometry for SITP detector prototypes.

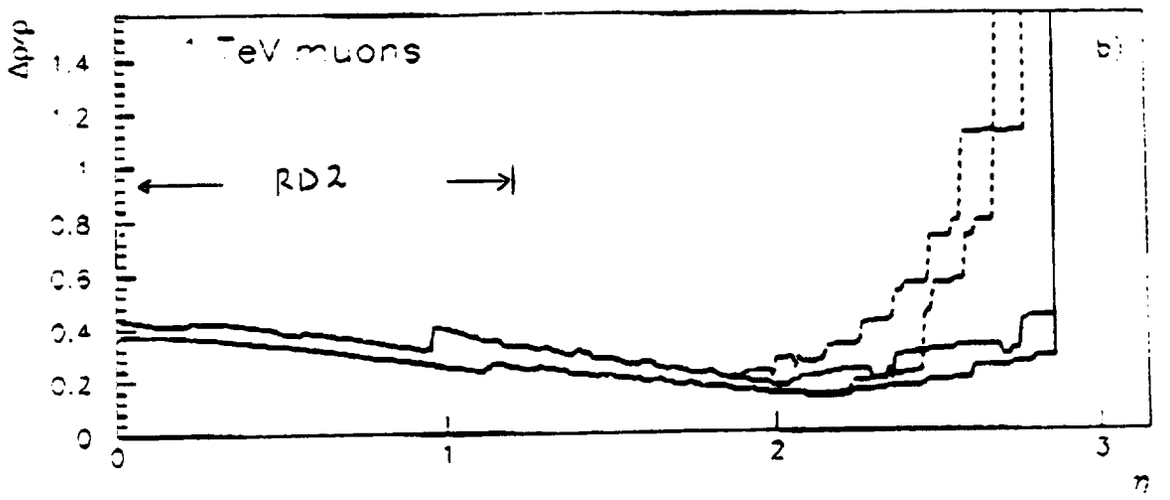

Fig. 2 Momentum resolution in EAGLE A, using the inner and outer tracking detectors in the central region [3].

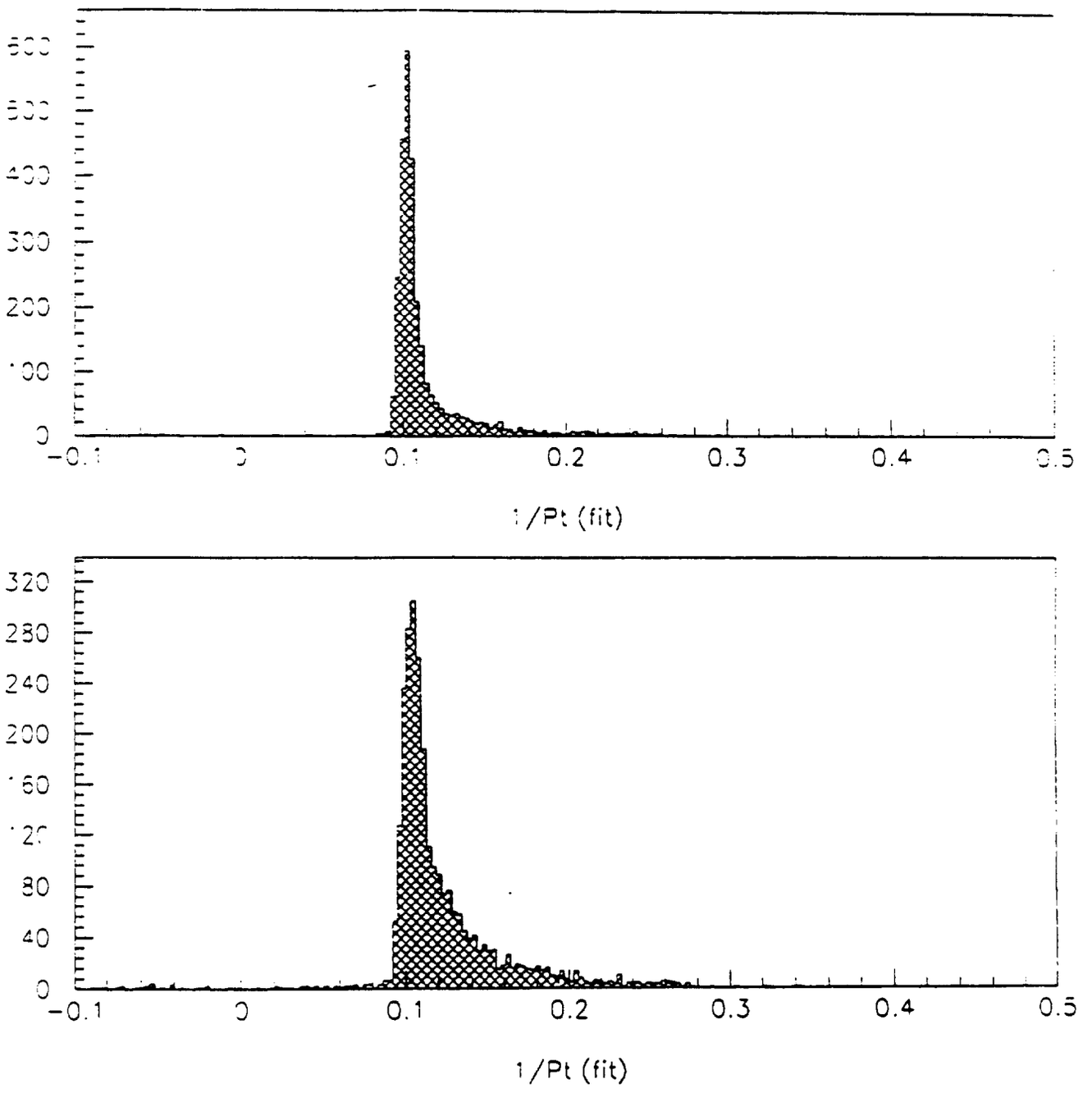

Fig. 3 The reconstructed inverse pt distribution for 10 GeV electrons at $\eta = 1.2$, for the EAGLE A (a) and EAGLE B (b) layouts

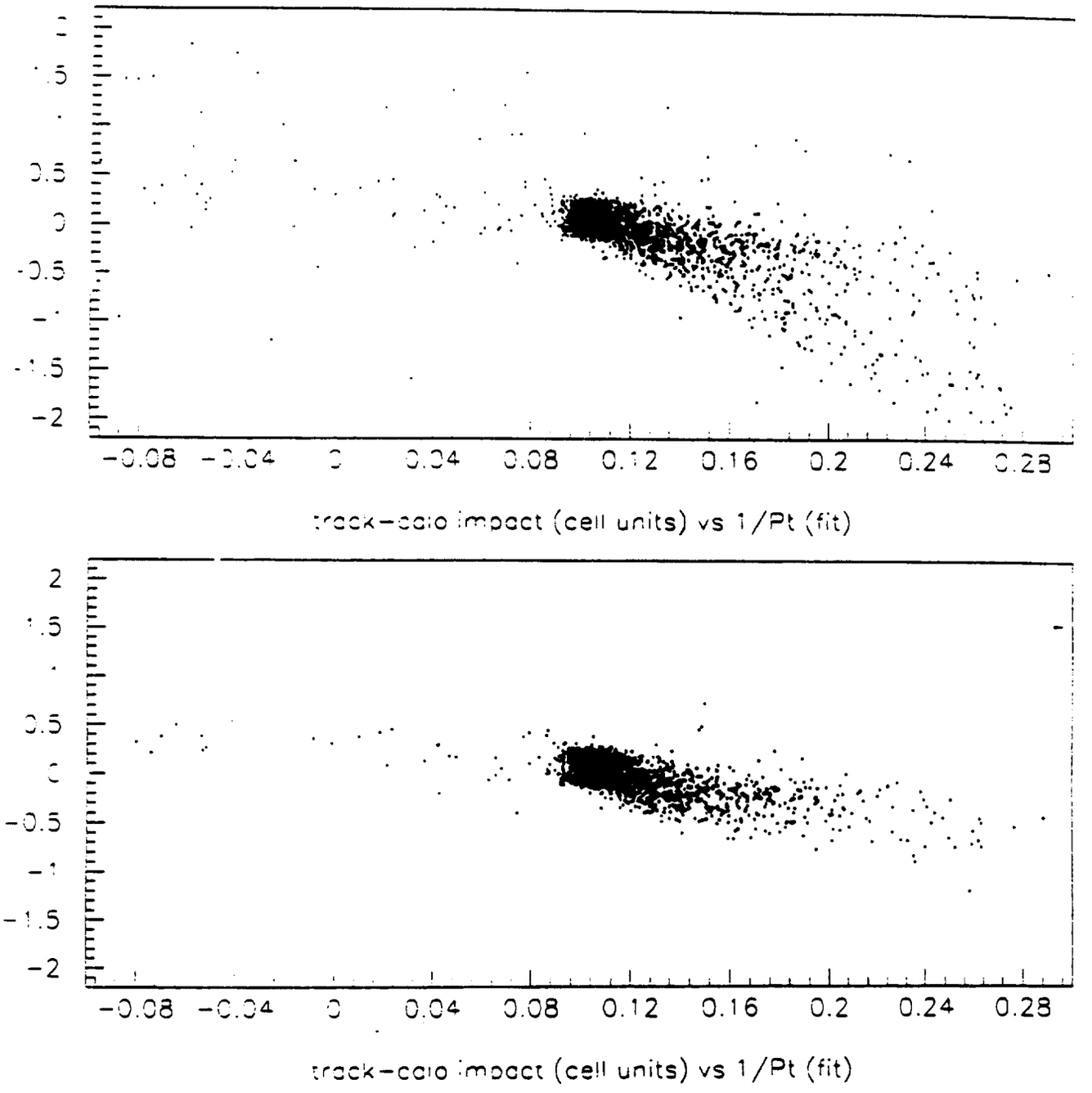

Fig. 4 The distribution of $1/p_t$ vs the distance of the extrapolated track from the calorimeter cluster centre, using a layout close to that of EAGLE B. The plots are shown for 10 GeV p_t electrons at η = 1.2, before and after a cut (3 σ) on the reconstructed calorimeter cluster energy.

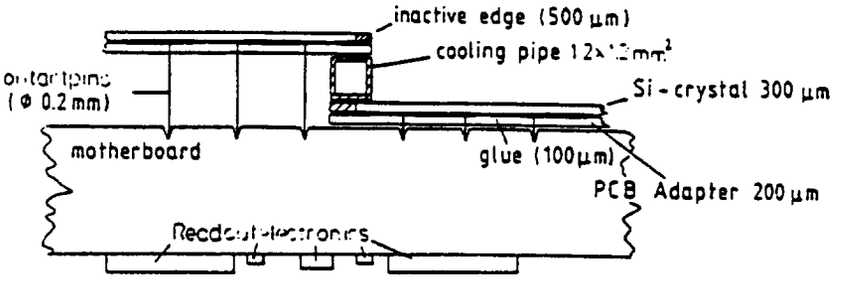

Fig. 5 Placement of silicon crystals and ancillary cooling on the circuit board for an SITP module.

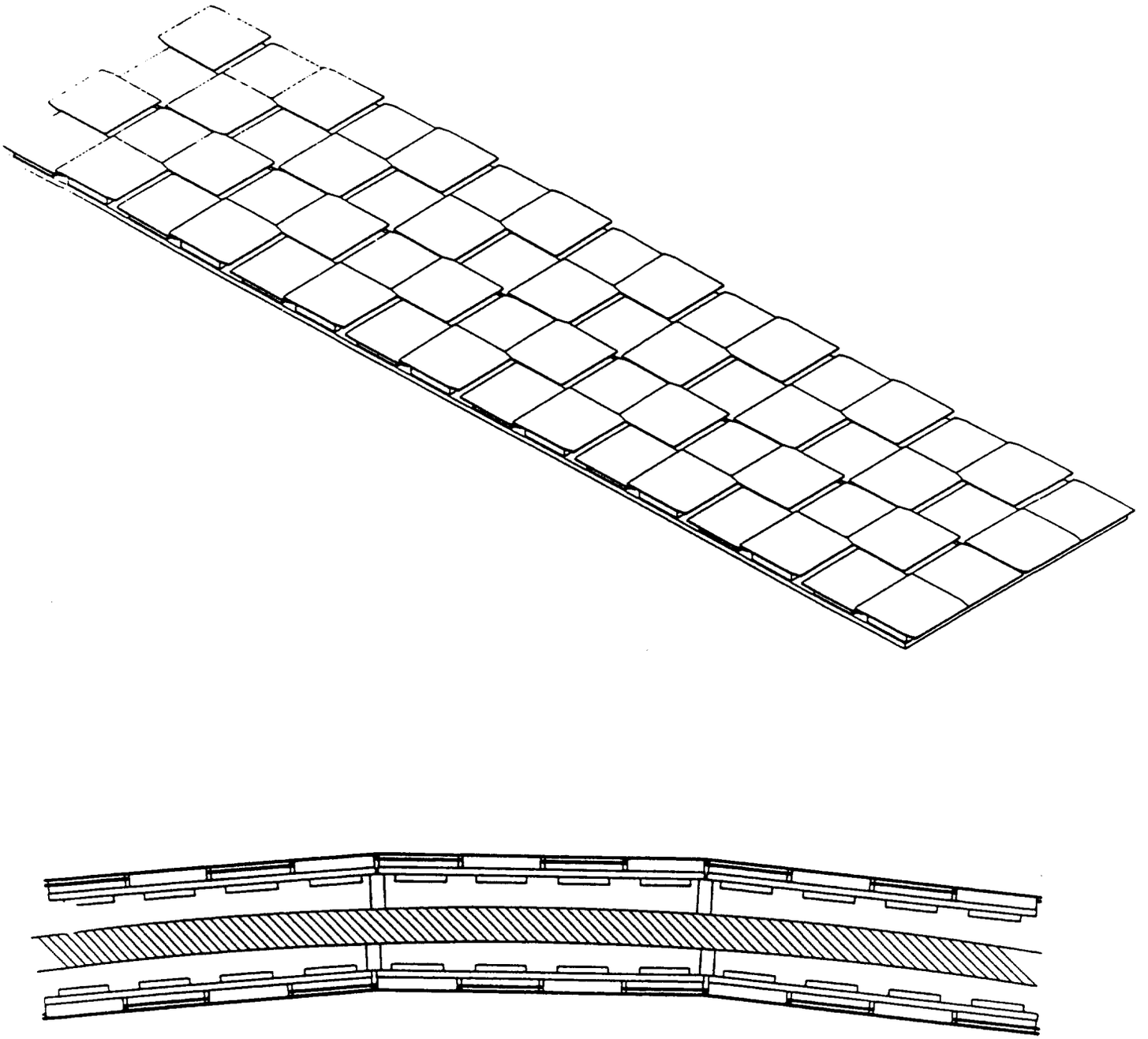

Fig. 6 Layout of counters on an SITP module, showing the tile structure and the arrangement of SITP modules on the support structure.

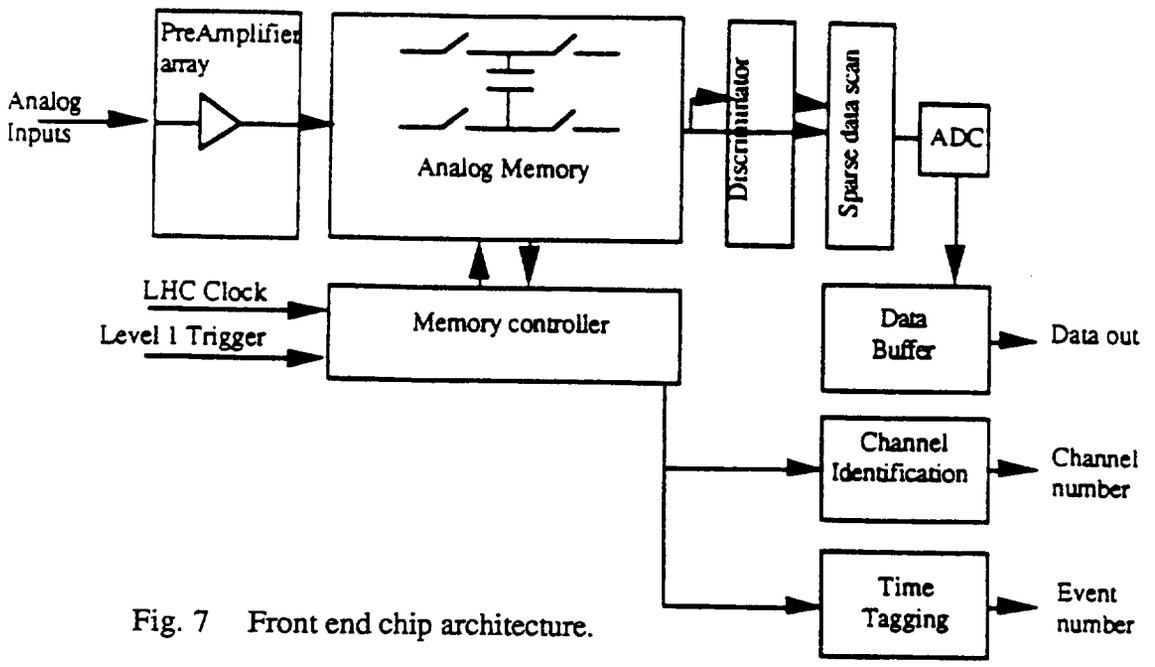

Fig. 7 Front end chip architecture.

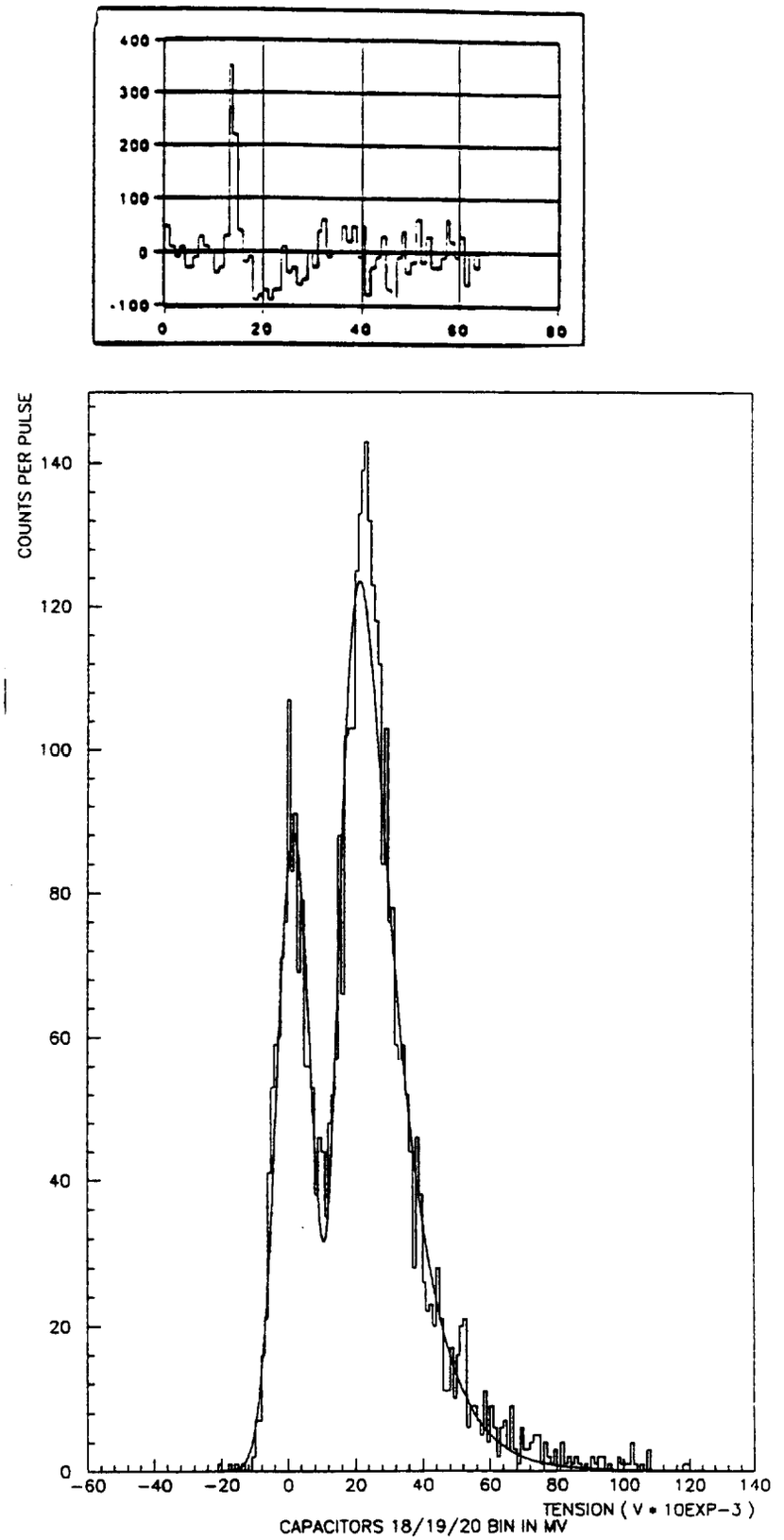

Fig. 8 Time distribution of a source signal at the output of the 4-channel chip prototype (a), and pulse height distribution after integration over 3 time buckets (b).

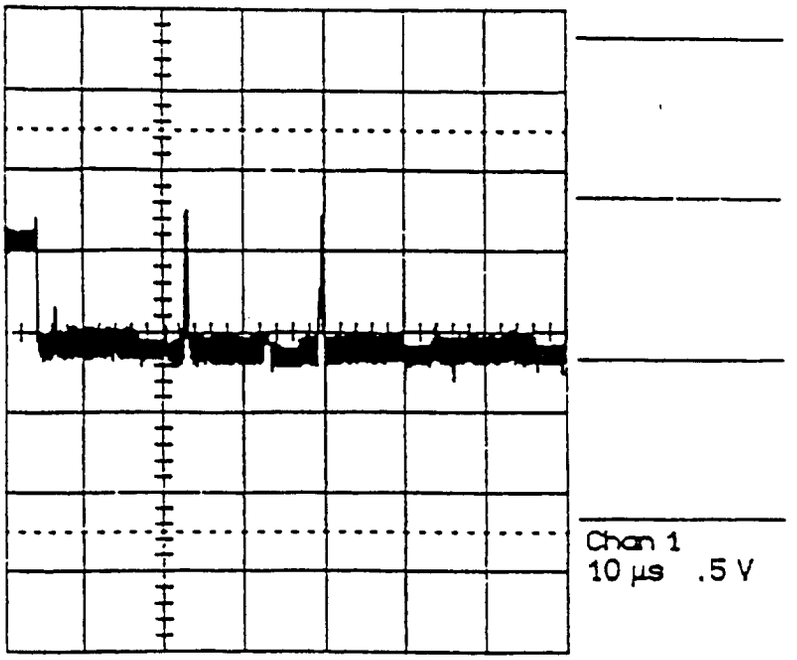

Fig. 9 Output signal from the SITP 32 channel chip, with charge injected on one of its channels.

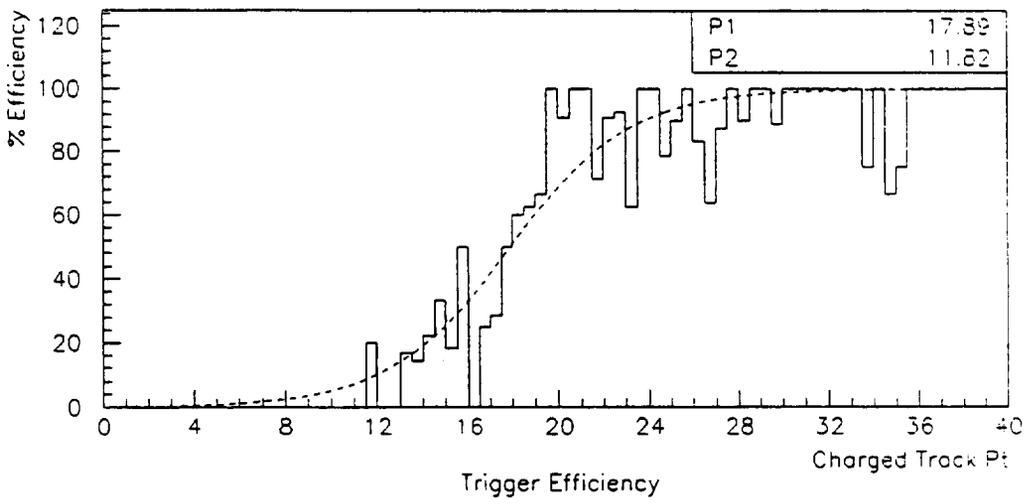

Fig. 10 Second level trigger efficiency estimated using the SITP detector to identify a high-p_t track associated to a calorimeter cluster.

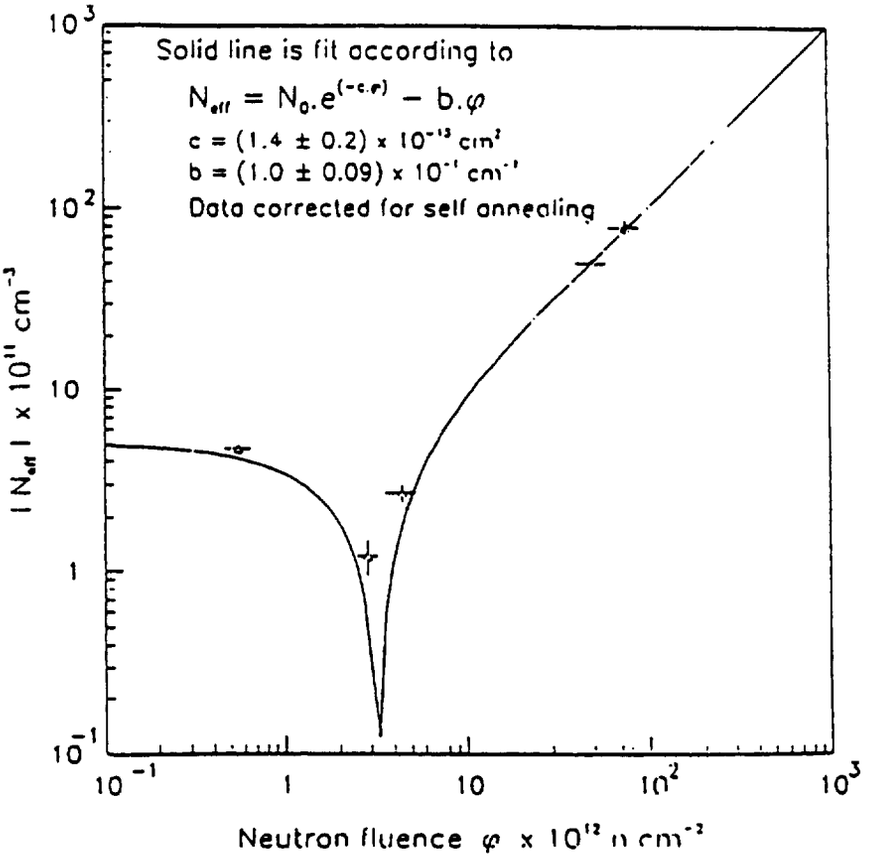

Fig. 11 Effective doping concentration of a typical silicon detector vs neutron fluence.

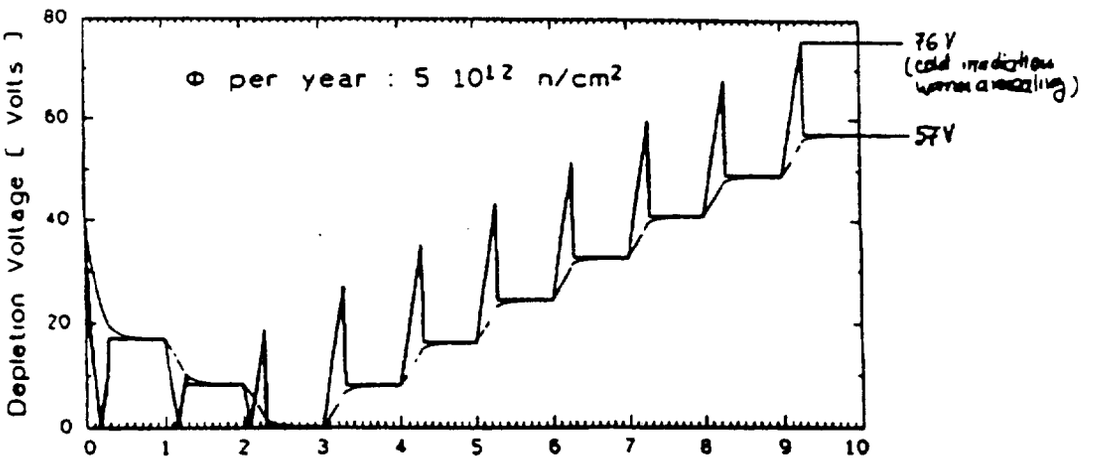

Fig. 12 Behaviour of depletion voltage over a 10-year period, for counters that a neutron irradiated, ignoring long term ageing affects.