Fermilab

TM-1319
0435.000

PULSED POWER SUPPLIES FOR THE FERMILAB 1 TEV SWITCHYARD*

L. Bartelson and J. Walton

June 1985

*Submitted to the 1985 Particle Accelerator Conference (NPS), Vancouver, British Columbia, Canada, May 13-16, 1985.

PULSED POWER SUPPLIES FOR THE FERMILAB 1 TEV SWITCHYARD

L. Bartelson and J. Walton

Fermi National Accelerator Laboratory*
P.O. Box 500
Batavia, Illinois 60510

Introduction

An upgraded system of pulsed switching magnets has been implemented in the Fermilab Switchyard to accommodate proton energies up to 1 TeV. These devices are required for switching the "slow" and "fast" extracted beams into their respective beam lines. "Slow" beam passes undeflected through the magnet in the off condition. During a pulse "slow" is disabled and "fast", which is of ~1 ms duration, is deflected. The requirement then is for a "flat-top" current pulse of minimum rise and fall time.

The circuit chosen is of the resonant charge recovery type. Several different styles and combinations of magnets are employed according to beam line requirements and constraints. In all cases maximum voltage is limited to 600 volts and pulse width to 100 ms.

Principle of Operation

The basic pulser circuit is shown in Fig.1 with associated current and voltage waveforms in Fig.2. There are four distinct steps in the pulse generating process. We shall follow through these, starting with main capacitor bank C charged to voltage Vc and commutating capacitor c charged to vc.

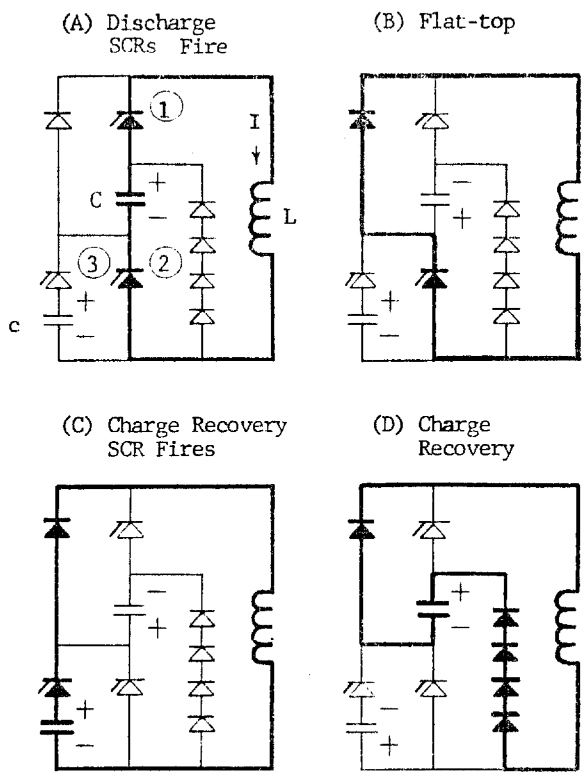

Fig. 1 Basic Pulser Circuit

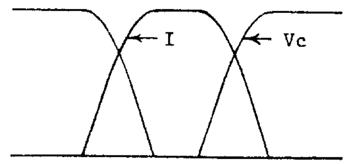

Fig. 2 Idealized Current and Voltage Waveforms

(A) Discharge SCR's Fire

Discharge SCRs 1 and 2 are triggered simultaneously. Current in the load magnet rises sinusoidally to a peak value of $Vc\sqrt{C/L}$ in a time of $\pi/2\sqrt{LC}$. Here we have assumed a slightly idealized condition of zero resistance for all elements.

(B) Flat-top

We see from Fig.2 that capacitor bank voltage leads load current by 90°. As current passes through a maximum capacitor voltage reverses polarity. This polarity reversal applies forward bias to the diode, switching it on and SCR #1 off. Note that the same forward bias is applied to the 4 series diodes but current preferentially switches to the single diode because of its lower forward voltage drop. The circuit now consists of a charged inductor driving current through a low resistance path. Load current decays with time constant L/R, typically ~.5 sec. This generates the "flat-top".

(C) Charge-Recovery SCR Fires

After a flat-top of ~20 msec charge recovery SCR #3 is triggered. This commutates SCR #2, diverting current through SCR #3 and commutating capacitor c.

(D) Charge Recovery

Capacitor c is rapidly discharged and reverses polarity about .2 msec after SCR #3 is triggered. This polarity reversal causes the 4 series diodes to be biased on. Now current has been switched back into the main capacitor bank in the correct polarity to recharge it. Current falls in a sinusoidal fashion as the capacitor bank is recharged to its initial voltage (neglecting losses).

Hardware

A typical switching station consists of a laminated magnet with L = .014 Henry, R = .016 Ω and 1,000 ampere current requirement. Taking Vc = 600 volts and C = .04 Farad gives a rise (and fall) time of 37 msec. Add 20 msec of flat-top for a total pulse width of 94 msec. Such a large value of capacitance dictates use of electrolytic capacitors. The 600 volt specification is met by having 2 series banks of 450 volt capacitors (see Fig.3). Ninety-six capacitors are required for .04 Farad. A diode is necessary to protect against one bank or the other experiencing polarity reversal as Vc drops to zero because in practice 2 banks can not be perfectly matched. In effect both halves of C are protected by diodes. Note that Vc must go negative in step B but only by ~2 volts which is within the operating range for

*Operated by Universities Research Association, Inc. under contract with the U.S. Department of Energy.

electrolytic capacitors. Energy storage electrolytic capacitors with low equivalent series resistance were chosen. All diodes and SCRs (phase control type) have a voltage rating of 1800V and current rating greater than 1,000A RMS.

It is important to maximize L/R of the total circuit. Since cable runs are ~500 ft, 500 MCM copper conductor was chosen.

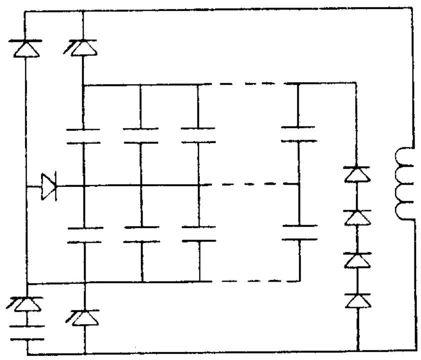

Fig. 3 Capacitor Bank Details

DC Level

In one case it is necessary to provide a pulse on top of a DC current level due to beam line constraints. This is accomplished by having a relatively large inductance in series with a current regulated DC supply (see Fig.4). The pulse current seen by the DC supply is attenuated from that in the load by the factor ℓ/L.

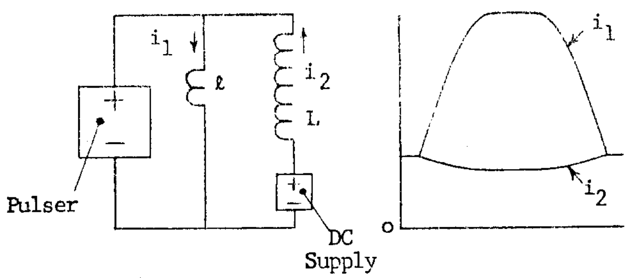

Fig. 4 DC Level

Controls and Instrumentation

Pulse-to-pulse variation must be limited to ~.1%. This is achieved by closely regulating main capacitor bank voltage. During a pulse the charging supply is inhibited (see Fig.5). After a pulse the capacitor bank voltage is about 20% low due to various circuit losses. When inhibit terminates, the voltage regulation loop is enabled and switches the charging supply into the capacitor bank. As soon as the required voltage is reached the supply is switched out. Switching is accomplished with gate-turn-off SCRs. A 3 phase charging supply was chosen to give finer regulation.

Another specification is that pulse current be adjustable over a wide range by varying a single reference level. This requires that commutating capacitor voltage must track main capacitor bank voltage. Since fairly low currents are involved here regulation is accomplished by switching on and off a solid state relay rather than gate-turn-off SCRs.

Pulse current is monitored by a Hall-effect type current transducer. This signal is sampled and held at the same time during flat-top for each pulse. Various personnel safety and over-temperature interlocks are also implemented.

Results

Seven units have been in continuous operation (5 pulses/minute) for about 6 months with no major failures. One modification has been required: a small commutating capacitor and SCR network has been added across discharge SCR #1 to insure turn-off. This SCR is triggered in the middle of flat-top. A typical current pulse is shown in Fig.6. Droop during flat-top is <.2%/msec.

Acknowledgements

We wish to thank George Krafczyk and Dan Wolff for their helpful suggestions, and Ken Sievert and Leroy Middlebrooks for their major role in building and commissioning of these devices.

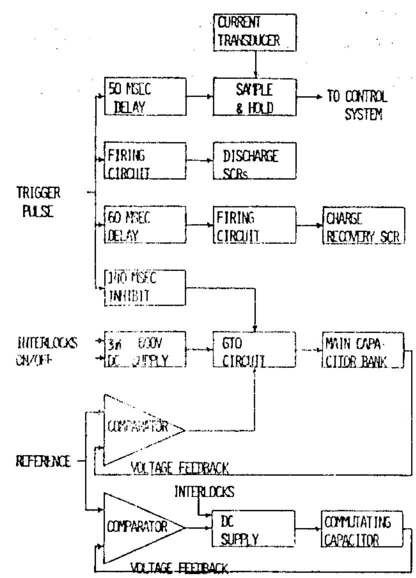

Fig. 5 Controls and Instrumentation

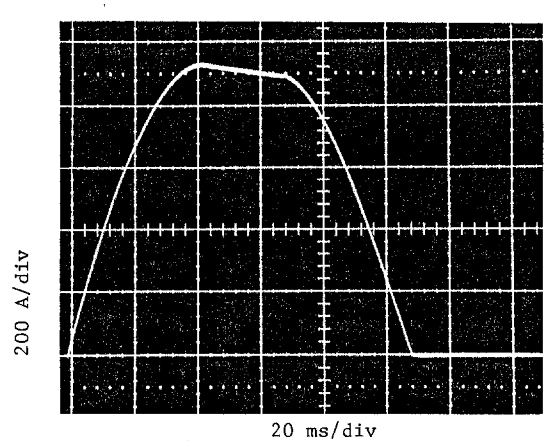

Fig. 6 Typical Current Pulse