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AC-LGADs Fermilab Front-End Electronics Characterization

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Abstract

We characterized the front-end electronics used to process high-frequency signals from low-gain avalanche diodes (LGADs) at the Fermilab Test Beam Facility. LGADs are silicon detectors employed for charged particle tracking, offering exceptional spatial and temporal resolution. The purpose of this characterization was to understand how the time resolution is influenced by the front-end electronics. To achieve this, we developed a setup capable of generating input signals with varying amplitudes. The output results demonstrated that signal processing by the front-end electronics plays a crucial role in enhancing time resolution. We showed that the time resolution achieved by the FEE board is better than $2\,ps$ at the 1σ level.

Keywords: High-frequency signal processing, Front-end electronics, Low-gain avalanche diode, Timing resolution, Jitter

1. Introduction

The luminosity upgrade of the LHC brings new challenges: up to hundreds of simultaneous collisions per bunch crossing are expected with this upgrade [1, 2, 3]; therefore, it is imperative to distinguish these events from

each other to ensure a good quality particle identification (PID) and vertex reconstruction.
One of the alternatives to take on these challenges is the AC-coupled low-gain avalanche diode (AC-LGAD), a silicon-based device that provide an excellent reconstruction of spatial and time information [4, 5, 6]. Recent studies [7] estimate a spacial and time resolution in the order of 6-10 μm and 30 ps respectively.

In order to extract the performance limits of the AC-LGAD, a specially designed front end electronics (FEE) must be used. A 16-channel LGAD Test board (Fig.1) was used as FEE to amplify and read the signals acquired by the AC-LGADs. This board was utilized successfully in the 2021 [7] and 2022 [8] AC-LGADs test beam campaigns at the Fermilab Test Beam Facility. The

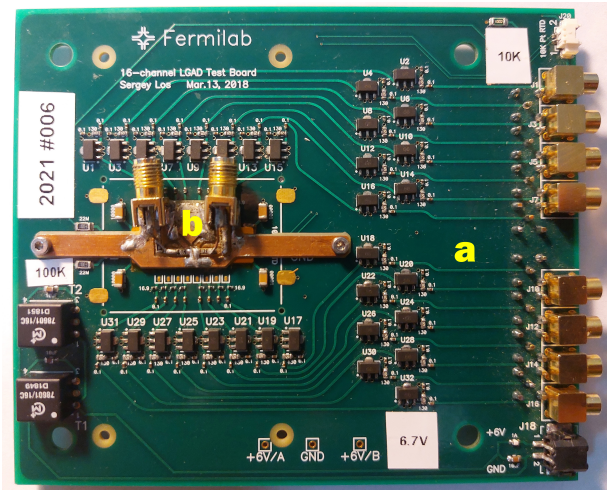

Figure 1: FEE board (a) with the designed charge injector (b) in place of an AC-LGAD.

main objective of this research is the characterization of the Fermilab FEE Board, which acts as the Device Under Test (DUT), starting from detailing its electronic schematic, the experimental setup and equipment utilized, the features of the signals used to characterize the DUT, and the results in terms of frequency response, gain, noise RMS, signal-to-noise ratio (SNR), and time resolution (jitter).

2. AC-LGADs Fermilab Front-End Electronics

The DUT has 16 dedicated input channels for each strip or pad of the corresponding AC-LGAD device. Each channel consists of a two-stage amplifier based on the *Minicircuits Gali S66+* surface mount monolithic amplifier, which provides amplification in the DC to 3 GHz frequency range. The amplifier is internally matched to 50 Ω, which requires that the traces of the board are designed with a 50 Ω impedance. The schematic of a single channel is shown in Fig. 2. In this particular configuration, the amplifiers used a 25 Ω input impedance and a bandwidth of 1 GHz. The amplifier chain of each readout channel has a uniform gain with an approximate 10% variation from channel to channel [9]. At 2 GHz, the expected gain for each amplifier

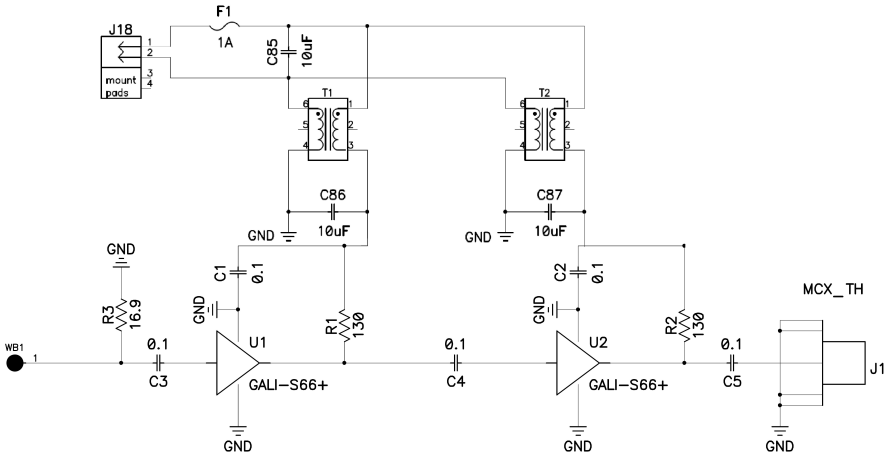

Figure 2: Single channel equivalent schematic.

stage is about 18.2 dB. The manufacturer specifies [10] the typical output power at 1 dB compression is 3.3 dBm, at 2 GHz. This output, at 50 Ω, is equivalent to $\sim$ 327 mV. Due to having two stages, the gain at 2 GHz is a factor of $\sim$ 66, hence a voltage range amplitude in $0 - 4.95\,mV$ ensures a constant gain at that frequency. The total trans-impedance on the DUT, after two stages of amplification, is roughly 4.3 $k\Omega$. The gain for LGAD signals is such that each femtocoulomb of input charge results in an additional $5mV$ in signal amplitude (that is, $100mV$ output for a $20fC$ input) [7].

3. Experimental Setup Overview

For the characterization process, we set basic conditions regarding the powering of the board and its temperature. We set $6.8\,V$ in a *Keithley 2230-30-1 DC Power Supply* to power the DUT. At that voltage, the current required by the DUT was $0.537\,A$. The board was kept inside the box (Fig. 3) at a temperature of $\sim 21.7\,°C$ throughout the tests using a *Lauda Alpha RA 8* recirculating chiller. We measured the temperature with a $10K$ RTD sensor connected directly to the DUT.

We used a *SiLabs Si5332-6EX-EVB REV 2.0* LVDS low-jitter clock generator (less than 175 fs RMS phase jitter) configured at $84.3\,MHz$ to produce squared signals of fixed width and amplitude. One of the outputs of the clock generator is connected directly to the first channel of the oscilloscope as a trigger for the experiment. Two other outputs of the clock generator fed a pulse generator, designed by the CALTECH INQNET [11] team, based on the *NB6L295 Dual Channel Programmable Delay Chip*. This device takes two input signals and produces two delayed signals which are driven into a *MC100LVEP05* Low Voltage Positive Emitter-Couple Logic (LVPECL) *AND* gate. The differences in the delays can produce nanosecond-width pulses, that would emulate those produced by a Minimum Ionizing Particle (MIP) when hitting an AC-LGAD. Additionally, we used different attenuation levels at the output of the pulse generator to achieve a similar voltage amplitude to those produced by the signals of MIPs and to study the behavior of the SNR. The range of amplitudes for the input test pulses was chosen to be representative of the charge deposited by a Minimum Ionizing Particle (MIP) in a 50 μm thick AC-LGAD. For such detectors, a collected charge of approximately 20 fC is a typical operating point to achieve a time resolution of 30 ps [9]. The FEE board under study provides a gain such that a 20 fC input charge results in a 100 mV output signal [7]. Considering the board's voltage gain of approximately 66 (a factor derived from its two-stage amplification), this corresponds to an input pulse amplitude of about 1.5 mV. As detailed in Table 1, the input pulse amplitudes used in this work range from 0.942 mV to 5.189 mV, which effectively covers the signal range relevant for MIP detection and allows for the characterization of the SNR performance around this critical operating point.

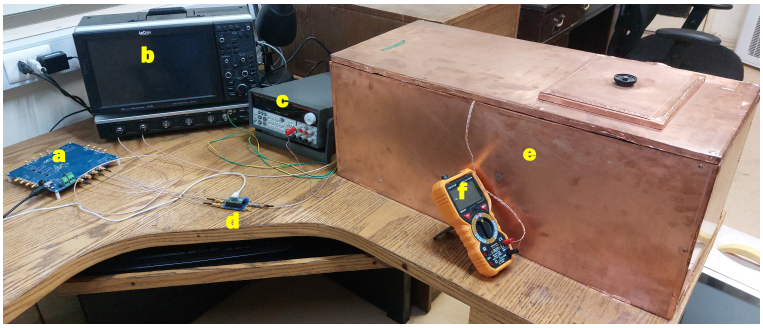

Figure 3: From left to right: clock generator (a), oscilloscope (b), power supply (c), pulse generator (d), EMI shielded enclosure containing the DUT (e), and multimeter for RTD measurement (f).

The signal produced by the pulse generator (see Fig. 4) was set at 1 ns width and 260 mV amplitude. The measured 20-80% rise time of the output pulses is on average $\sim$ 350 ps, a value that is primarily limited by the instrument response of the 1 GHz bandwidth oscilloscope. The non-ideal pulse shape, including the observed overshoot and subsequent ringing, is a characteristic artifact of the pulse generator's design, which relies on a high-speed LVPECL logic gate (*MC100LVEP05*) not originally intended for generating clean analog test signals. To provide a single-ended input to the charge injector, one of the two differential outputs of the pulse generator is used, which is then AC-coupled to remove its DC component.

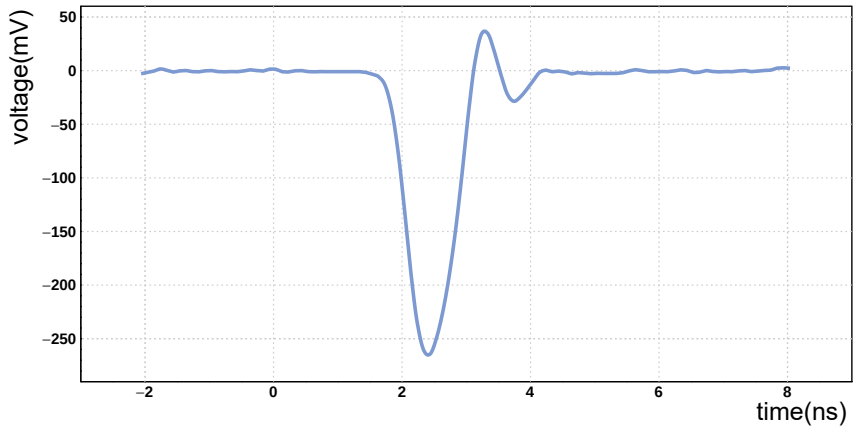

Figure 4: Output from the pulse generator without any attenuation applied.

We manufactured a charge injector (Fig. 1) to guide the output signals of the pulse generator into an input channel of the DUT. The injector consisted of an SMA input connector with a 50 Ω resistor coupled to ground to match the input impedance of the cables; additionally, a 100 nF capacitor was connected in series with the input connector to eliminate LVPECL common mode voltage, and at the output of the charge injector, we used a spring-loaded contact connector. To isolate the DUT from external electromagnetic noise, it was placed inside a custom-built EMI shielded enclosure (Fig. 3). The data acquisition was performed using a *LeCroy WaveRunner 610Zi* oscilloscope. This instrument has a $1 GHz$ bandwidth and a maximum sampling rate of $20 GSa/s$. The bandwidth imposes a manufacturer-specified $10-90\%$ rise time of $375\,ps$, which sets a fundamental limit on the measurement of fast signal transitions.

We arranged these devices in different configurations to perform the characterization.

4. Gain and Jitter characterization

4.1. Experimental Setup

The experimental setup used for the gain and jitter characterization is depicted in Fig. 5. A low-jitter clock generator provides the primary time reference for the system. This clock signal is sent to two destinations: directly to a reference channel on the oscilloscope, and as a trigger to the pulse generator. The pulse generator produces test signals that emulate those from a MIP. These signals are then passed through a variable attenuator, which allows for the adjustment of their amplitude to study the DUT's performance across a range of input signal levels. The attenuated pulse is fed into the FEE board (DUT) via the custom charge injector. Finally, the oscilloscope simultaneously captures the amplified output signal from the DUT and the original reference clock signal. This configuration allows for a precise measurement of the output signal's characteristics (amplitude, rise time) and the time difference between the reference and the DUT output, which is essential for the jitter analysis.

4.2. Overview of The Pulses

We used specially-developed software to acquire and convert binary data directly from the oscilloscope to ROOT framework data files [12]. This software was developed by the FNAL CMS-MTD team, which was successfully

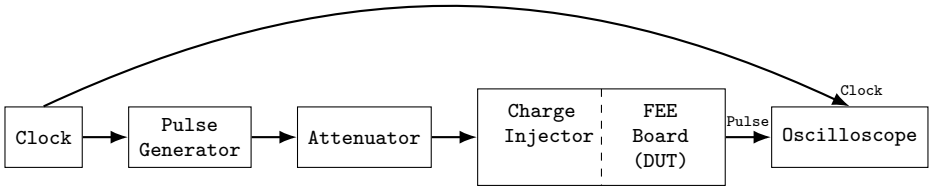

Figure 5: Experimental setup for amplitude, noise RMS and jitter analysis.

utilized in previous works [7, 8]. As a reference, Fig. 6 shows 5000 events for the 40 dB configuration.

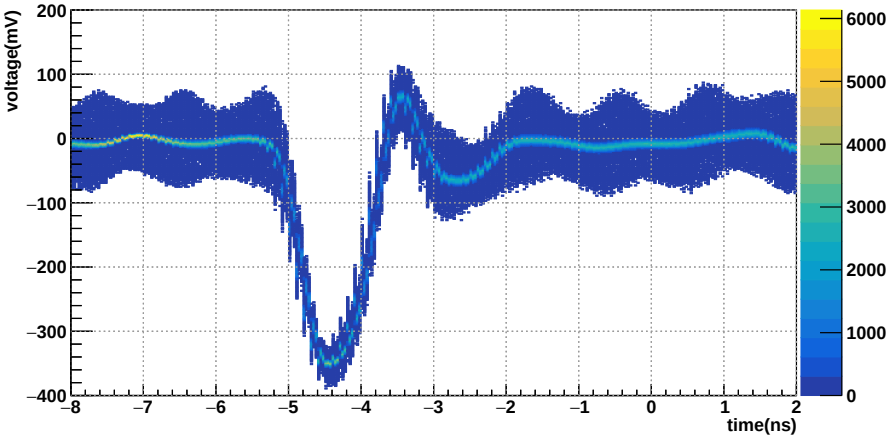

Figure 6: 5000 events acquired from the output of the readout board of FNAL using the CMS-MTD Timing DAQ codes [13].

In Fig. 7 can be seen a comparative plot between one event for every configuration.

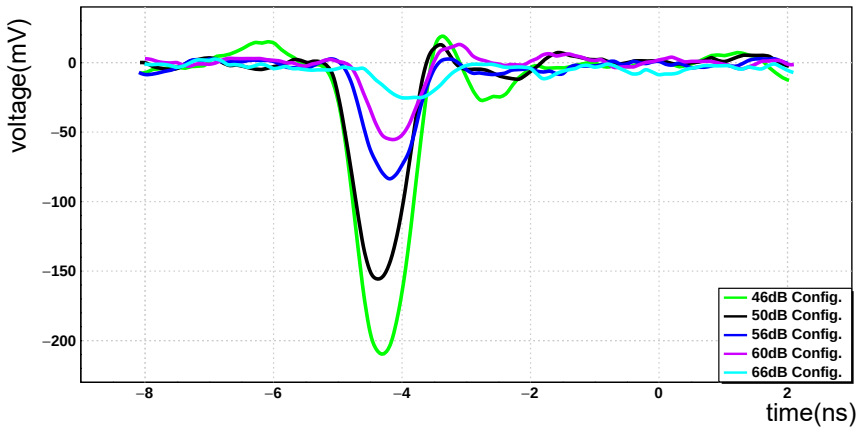

Figure 7: Outputs from the FEE for different attenuators between the pulse generator and the FEE input.

4.3. Gain Results

Pulses of different amplitudes were applied at the input pad of channel 8 of the board, with the clock generator set at $84.3\,MHz$. The output amplitudes were measured as seen in Fig. 8.

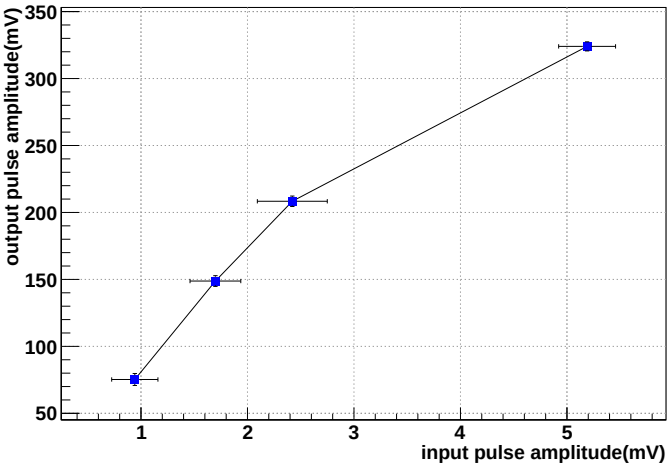

Figure 8: Output amplitudes as a function of input amplitudes, channel 8.

As a result from the amplitude comparison, the gain was calculated for

each pulse, as presented in table 1. This was corroborated with the VNA results shown in the following section.

The output signals were characterized over a wide range of input attenuations, from 40 dB to 66 dB, as shown in Fig. 7. However, direct measurement of the corresponding *input* pulse amplitudes was only feasible for attenuations up to 56 dB. For higher attenuation values (i.e., 60 dB and 66 dB), the input signal amplitude fell below the noise floor of the oscilloscope, preventing a reliable characterization. For this reason, the quantitative gain analysis presented in Table 1 and Fig. 8 is limited to the subset of measurements where both input and output signals could be accurately measured.

Attenuation at pulse generator output dB	**Input pulse amplitude mV**	**Output pulse amplitude mV**	**Gain dB**
56	0.942 ± 0.217	75.267 ± 4.459	38.05 ± 2.07
50	1.698 ± 0.238	148.785 ± 4.008	38.85 ± 1.24
46	2.421 ± 0.328	208.359 ± 3.888	38.70 ± 1.19
40	5.189 ± 0.267	324.017 ± 3.392	35.91 ± 0.47

Table 1: Output amplitudes from the FEE and the corresponding input pulse amplitude at the channel input. The attenuators are installed after the pulse generator to get the shown input amplitudes. The drop in the gain for the biggest input pulse can be explained by the gain compression of the *Minicircuits Gali S66+* amplifier at that amplitude.

4.4. Jitter measurement

To evaluate the time resolution, the signals were processed using the CMS-MTD Timing DAQ framework [13]. After identifying the rising edge on the selected oscilloscope input channel, the time difference between input signals was computed at a constant fraction of their respective amplitudes. The variance of the resulting time difference distribution, as defined in Equation 1, corresponds to the measured jitter. Using the experimental setup shown in Fig. 5, the analysis focused on the time difference between a reference signal (clock) and the device under test (FEE board).

$$\Delta t = t(50\% \text{ Rising Edge @ Reference}) - t(50\% \text{ Rising Edge @ DUT}), \quad (1)$$

4.4.1. Time resolution

If a noisy analog pulse is applied to a leading edge trigger, the timing uncertainty can be obtained by projecting the variance σ_n of the momentary

signal amplitude on its rate of change at the trigger threshold V_T. This yields the variance in time σ_t -time resolution-, called jitter [14].

$$\sigma_t = \frac{\sigma_n}{\frac{dV}{dt}\Big|_{V_T}} + \delta t \tag{2}$$

Assuming the rising edge is roughly described by a straight line, the previous expressions can be associated with the following concepts:

- σ_n to the Noise RMS.
- σ_t to the Time Resolution.
- $\frac{dV}{dt}$ to $\frac{\text{Amplitude}}{\text{Rise Time}}$.
- δt to the the residual jitter of the associated electronics.

We can project the noise on its rate of change at the trigger threshold to obtain an expression for the jitter [14]. Thus, re-arranging the previous approximations we obtain:

$$\sigma_t \approx \frac{\text{Rise Time}}{\text{SNR}} + \delta t \tag{3}$$

Hence, an increase in the SNR should provide a better time resolution, since the rise time depends on fixed characteristics of the input signal, readout electronics and ADC bandwidth. Moreover, we notice that the last term cannot be reduced as we increase the input signal, so the asymptotic behavior of the jitter δt will be the *time resolution of the system*. Thus, as part of the characterization of the FEE, we will measure the contribution of the FEE readout board in the time resolution to understand its impact on the AC-LGADs measurements.
We set the same voltage and time scales in the oscilloscope for most of the configurations since a variation in the voltage scale can change the level of ADC noise.

4.4.2. Pulse generator and associated electronics jitter

As part of the characterization, we measured the jitter of the system comprising the clock, pulse generator, charge injector, and oscilloscope, as shown in Fig. 9. To facilitate this measurement, a custom adapter was

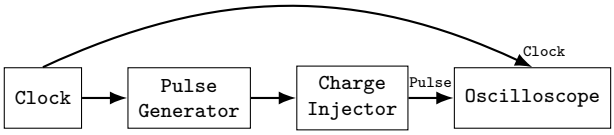

Figure 9: Experimental setup for jitter analysis of the pulse generator and associated electronics. The attenuators were not considered in the analysis since their effect in the time resolution is negligible and they were only used to change the input pulse amplitudes.

developed to enable a direct connection between the oscilloscope and the charge injector.

To measure the baseline jitter of the pulse generator and oscilloscope ($\sigma_{pulse\ generator}$), the output of the generator was fed into a passive 50 Ω power splitter. The two identical resulting signals were connected to two separate channels of the oscilloscope. The jitter was then calculated from the standard deviation of the distribution of the time difference between the two channels, measured at a constant fraction of their amplitude. This differential measurement method effectively cancels the intrinsic jitter of the pulse generator, isolating the combined jitter contributions from the oscilloscope and cabling, which constitutes the baseline resolution of the measurement system.

The measured time resolution is given by:

$$\sigma_{pulse\ generator} = 4.13 \pm 0.12\ (ps) \tag{4}$$

4.4.3. Output amplitudes, rise time, jitter, noise and SNR

Using the setup shown in Figure 5, we characterized several parameters of the output signals. The results are summarized in Table 2. An increase in the signal-to-noise ratio (SNR) is observed to significantly enhance the time resolution, highlighting the importance of front-end electronics (FEE) in the performance of such sensors. Notably, the noise levels remain approximately constant across different output amplitudes, underscoring that the improvement in resolution is primarily driven by the increase in signal amplitude rather than a reduction in noise. It should be noted that the measured rise times are comparable to the oscilloscope's manufacturer-specified $10 - 90\%$ rise time of 375 ps. Therefore, the values presented in the table should be considered an upper limit, as they are likely dominated by the instrumental response of the oscilloscope.

Att. (dB)	**Rise time $_{20-80\%}$ (ps)**	**Noise RMS (mV)**	**Amp. (mV)**	**SNR**	**Jitter (ps)**
36	300 ± 6	1.84 ± 0.40	795 ± 1	487 ± 105	4.63 ± 0.03
40	344 ± 14	3.04 ± 1.04	331 ± 3	129 ± 33	6.14 ± 0.11
46	353 ± 16	2.57 ± 0.86	206 ± 4	76 ± 21	8.21 ± 0.16
50	382 ± 28	2.29 ± 0.85	152 ± 3	82 ± 22	11.36 ± 0.17
56	358 ± 40	2.89 ± 1.01	73 ± 4	47 ± 14	22.66 ± 0.30
60	435 ± 59	2.20 ± 0.87	53 ± 4	31 ± 9	30.38 ± 0.46
66	357 ± 94	2.38 ± 0.94	25 ± 4	13 ± 4	78.55 ± 1.39

Table 2: Summary of the extracted parameters. Reported uncertainties are statistical only and do not account for systematic effects.

4.4.4. FEE Board Time Resolution

As demonstrated in the model proposed by [14], the time resolution exhibits an asymptotic behavior as a function of the signal-to-noise ratio (SNR), a trend that is clearly observed in Fig. 10.

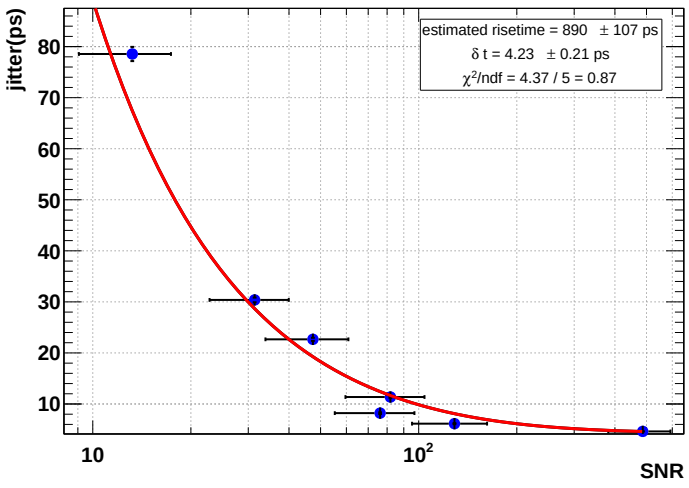

Figure 10: Jitter as a function of signal-to-noise ratio (SNR). The solid line represents a weighted least-squares fit to the data using a model that quadratically adds an SNR-dependent term and a constant asymptotic jitter floor (δt). The resulting fit parameters, including the extracted asymptotic jitter, are displayed.

The data were fitted using a model based on the quadratic sum of an SNR-dependent term and a constant noise floor, δt, given by the function $\sqrt{\left({}^{risetime}/_{SNR}\right)^2 + \delta t^2}$. This model provides an excellent description of the data, as indicated by the resulting ${}^{\chi^2}/_{ndf} = 0.87$.

The fit yields an asymptotic jitter of $\delta t = 4.23 \pm 0.21\ ps$. The first parameter represents an effective rise time, and is found to be $890 \pm 107\ ps$. It is important to note that this effective parameter should not be directly identified with the physically measured $20 - 80\%$ rise time of the individual pulses (which is, on average, $\sim 350\ ps$ according to Table 2). Instead, this fit parameter absorbs more complex system behaviors, including the slight variation of the rise time with SNR, into a single effective value that best describes the overall trend of the data. The primary result from this robust fit is the extraction of the physically consistent asymptotic jitter floor, δt.

Assuming that the jitter introduced by the FEE board is statistically uncorrelated with the jitter contributions from other elements in the experimental setup, the total time resolution can be expressed as:

$$\delta t^2 = \sigma^2_{FEE} + \sigma^2_{pulse\ generator} \tag{5}$$

where:

- σ_{FEE} is the time resolution of the FEE board.
- δt is the time resolution of the experimental setup in Fig. 5.
- $\sigma_{pulse\ generator}$ is the time resolution of the experimental setup in Fig. 9.

Using this relation and the previously quoted values, the time resolution of the readout board was estimated as:

$$\sigma_{\mathrm{FEE}} = 0.91 \pm 1.12\ (ps) \tag{6}$$

Since the uncertainty is larger than the central value, the result is consistent with zero. We therefore set an upper limit on the contribution of the FEE board to the time resolution of $2\ ps$ (1σ confidence level).

5. Frequency Response

5.1. Experimental Setup

We used a 6 GHz bandwidth vector network analyzer (VNA), branded *NanoRFE VNA6000*, to measure the frequency response (S_{21}) of a single

channel. To protect the VNA's ports from the high gain of the DUT, a 20 dB attenuator was placed at the input of the charge injector and a 10 dB attenuator at the output of the FEE board. The complete signal path for the measurement was: VNA Port 1 → 20 dB Attenuator → Charge Injector → FEE Board Input → FEE Board Output → 10 dB Attenuator → VNA Port 2.

A two-port Short-Open-Load-Through (SOLT) calibration [15] was performed to de-embed the measurement chain, including the attenuators. For the *Through* standard, a custom adapter was fabricated to connect the charge injector's input directly to an SMA output. Therefore, the VNA was calibrated to set its reference plane at the DUT's input and output, with the internal calibration algorithm accounting for the losses of the attenuators. No manual mathematical corrections were applied to the data post-measurement (see Fig. 11).

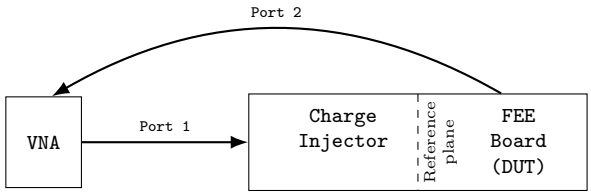

Figure 11: Experimental setup for the frequency response analysis. The SOLT calibration was performed at the Reference Plane using a custom adapter. For clarity, the protective attenuators used during the measurement are not shown in this diagram.

5.2. Results

The forward voltage gain S_{21} is plotted for channel 8 in Fig. 12. The gain is approximately 35 dB across the measured frequency range. This value is systematically lower than the $\sim 38\,dB$ gain obtained with the pulse method (Table 1). This discrepancy is likely attributable to the systematic uncertainty introduced by the VNA calibration process itself. The use of a custom-fabricated, non-ideal *Through* standard can lead to an imperfect de-embedding of the measurement chain by the VNA's algorithm, resulting in a systematic offset in the final S_{21} measurement.

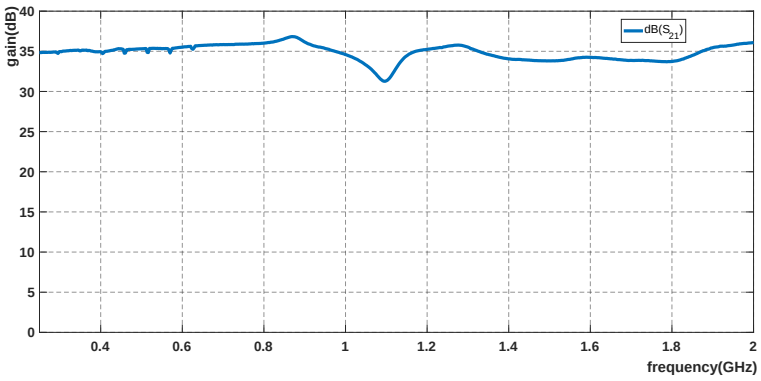

Figure 12: S_{21} parameter for channel 8 obtained with VNA. The gain is approximately 35 dB for all the measured frequency range. Results are similar to table 1.

6. Noise Spectrum

6.1. Experimental Setup

We used the Spectrum Analyzer *WR6ZI-RK-SPECTRUM* optional software package of the oscilloscope to estimate the noise spectrum introduced by the DUT.

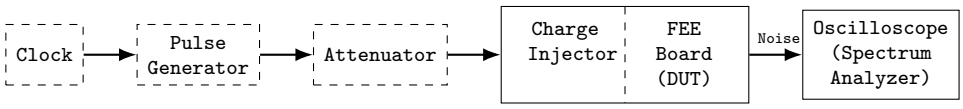

Figure 13: Experimental setup for the noise spectrum analysis. To estimate the baseline noise, all the system was connected but the FEE Board was not powered. To get the total output noise, all the setup was connected but no pulse signal was generated. Thus, the FEE Board noise was obtained according to equation 7.

As explained in [16], the estimated magnitude spectrum $|\hat{X}(f)|$ could be extracted by subtracting the time-averaged noise $|\overline{N(f)}|$ from the signal magnitude spectrum $|Y(f)|$:

$$|\hat{X}(f)| = |Y(f)| - |\overline{N(f)}| \tag{7}$$

In our case, for equation 7, $|\hat{X}(f)|$ is the FEE Board introduced noise spectrum, $|Y(f)|$ is the total output noise, and $|\overline{N(f)}|$ is the baseline noise introduced by the oscilloscope itself and other setup elements. This can be shown since the oscilloscope baseline noise is uncorrelated with the output

noise from the FEE Board, thus we can apply the expectation operator and obtain:

$$\begin{aligned} \mathbb{E}[\mid \hat{X}(f) \mid] &= \mathbb{E}[\mid Y(f) \mid] - \mathbb{E}[\mid \overline{N(f)} \mid] \\ &= \mathbb{E}[\mid X(f) + N(f) \mid] - \mathbb{E}[\mid \overline{N(f)} \mid] \\ &\approx \mathbb{E}[\mid X(f) \mid] \end{aligned} \tag{8}$$

Therefore, in order to obtain the output noise power spectrum introduced by the board, we subtracted the oscilloscope baseline noise spectrum (all the system setup was connected, but the FEE readout board was not powered, see Fig. 13) from the noise spectrum obtained as output from the FEE board powered on, without any input signal going through the system (see Fig.14).

6.2. Results

Figure 14 shows the power spectral density of the noise at the output of the FEE board, after subtracting the baseline noise contribution from the oscilloscope and other setup elements. The estimated board noise (blue curve) is observed to be relatively flat across the frequency spectrum up to approximately 1 GHz. This is consistent with the nominal bandwidth of both the front-end electronics and the oscilloscope used for the measurement. The gradual drop in the observed power spectrum above 1 GHz is a direct consequence of the oscilloscope's analog bandwidth limit. Several discrete peaks are visible in the total measured noise, which are likely due to ambient electromagnetic interference in the laboratory environment not fully suppressed by the shielding enclosure. The integrated noise over this bandwidth *should theoretically correspond* to the noise RMS values presented in Table 2, which are a key parameter in determining the time resolution.

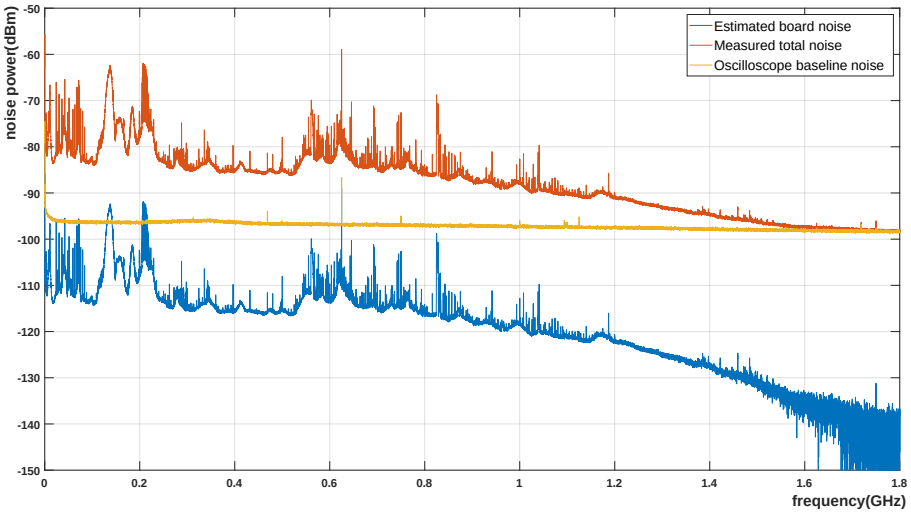

Figure 14: Output noise power spectra. The oscilloscope analog bandwidth is 1 GHz, which explains the gradual drop in the observed power spectra.

7. Conclusions and Outlook

We performed a detailed characterization of the front-end electronics (FEE) designed for the signal processing of AC-LGADs, using test signals similar in nature to those employed at FNAL for readout board evaluation. The time resolution of the experimental setup exhibited an asymptotic trend with increasing SNR, which allowed us to extract the contribution of the FEE to the overall time resolution.

The results confirm that the high-gain, low-noise amplification provided by the FEE is essential for achieving high time resolution. By preserving the initial signal-to-noise ratio of the sensor's signal while raising its amplitude far above the noise floor of the measurement system, the FEE enables precise timing measurements. Furthermore, the baseline noise is not significantly amplified; in fact, the observed noise levels fluctuate within a range that is approximately 10% of the amplitude of the smallest signal generated in our setup.

The measured performance of the FEE meets the requirements established by previous simulation studies on LGAD pulse processing [17], which indicate that for 50 μm LGADs targeting a time resolution of 35 ps, the FEE must provide a bandwidth exceeding 350 MHz and ensure an SNR greater than 30.

This work focused on the characterization of a single channel. A complete assessment of the board's performance in a multi-channel environment would require the characterization of inter-channel effects, such as crosstalk. Such measurements necessitated the design and fabrication of a dedicated multi-channel charge injection board, which was beyond the scope of this initial study focused on establishing a robust methodology for time resolution analysis. This comprehensive inter-channel characterization remains a crucial step for future work.

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