The new readout system for the ALICE Zero Degree Calorimeter in LHC Run 3

Paolo De Remigis[1,*] , Pietro Cortese[1, 2], Giorgio Cotto[1, 3], Nora De Marco[1], Luca Lombardo[1, 4], Carlo Puggioni[5], Mario Sitta[1, 2] and Stefan Cristi Zugravel[1, 4]

[1]INFN Torino, Italia
[2]Università del Piemonte Orientale, Italia
[3]Università di Torino, Italia
[4]Politecnico di Torino, Italia
[5]INFN Cagliari, Italia
(*) deremigi@infn.it

***Abstract* —The Zero Degree Calorimeter (ZDC) was designed to provide the event geometry and luminosity measurements in heavy-ion operation. In order to exploit the potential offered by the LHC's increased luminosity in Run 3, the ZDC upgraded its readout system to acquire all collisions in self - triggered mode without dead time. The purpose of the upgrade was to enable the detector to cope with the increased event rate while preserving its time and charge resolution performance. The ZDC operating conditions in Run 3 Pb – Pb collisions are extremely challenging due to the presence of electromagnetic dissociation processes (EMD). For example when running in self-triggered mode the ZDC system will need to sustain a readout rate of ∼2.5 MHz for the channels of the most exposed calorimeters compared to the foreseen hadronic rate of 50 kHz sustained by the other detectors. The previous electronics, based on Charge-to-digital converters (QDCs), with a fixed dead time of ∼ 10 μs, and on readout through VME bus, could not cope with such a high rate. Moreover, a crucial aspect of the ZDC operation in Run 3 is acquiring the events with a reduced bunch spacing of 50 ns (lower than the length of the signal of ∼ 60 ns) in the presence of high signal dynamics (from a single neutron to ∼ 60 neutrons). The new acquisition chain is based on a 12 bit digitizer with a sampling rate of about 1 GS/s, assembled on an FPGA Mezzanine Card. The signals produced by the ZDC channels are digitized, and samples are processed through an FPGA to extract information such as timing, baseline average estimation and luminosity. The architecture of the new readout system, the auto trigger strategy, the firmware organization and the ZDC performance during 2022 Pb–Pb collisions are presented.**

***Keywords* —FPGA readout; ALICE ZDC.**

I. INTRODUCTION

The Large Hadron Collider (LHC) is a very big facility at CERN, where it is possible to create interactions between two particle beams, which can be either protons or ions. On that large machine four experimental apparatus are installed to study the fundamental elements of the matter, with each one devoted to a particular aspect. The A Large Ion Collider Experiment (ALICE) is a detector dedicated to heavy – ion physics, particularly designed to study a phase of matter called Quark-Gluon Plasma (QGP) [1] . The ALICE detector consists of different sub detectors, each designed to look for specific types of particle, and the Zero Degree Calorimeter (ZDC) is the one that detects the energy of the spectator nucleons [2] .

It is specifically composed of two identical sets of calorimeters located at 112.5 m from the interaction point. Each set consists of a Neutron (ZN) and a Proton (ZP) calorimeter. The ZN and ZP are quartz – fiber spaghetti calorimeters with silica optical fibres as active material embedded in a dense absorber. The principle of operation is based on the detection of Cherenkov light, produced by the charged particles of the shower in the fibres. The light produced by the hadronic showers is collected by photomultipliers. The main purpose is to provide measurements of the time of the collision, vertex position, centrality, event plane and to measure the luminosity in heavy - ion operations.

The previous readout system for the ZDC detector was based on the commercial Caen module in VME format, such as Charge to Digital Converter (QDC) and Time to Digital Converter (TDC). The goal was charge integration to analyze the signal amplitude, and timing evaluation to detect the arrival time of the nucleons on the calorimeters.

Due to a QDC conversion time of 10 μs the event rate was limited to approximately 100 kHz on average.

The new requirements [3] for the ZDC during the LHC Run 3 is to operate in self – triggered mode without dead time at an average event rate of 2.5 M event/s, preserving the amplitude and time resolution. The proposed readout architecture is FPGA - based to add the possibility of online data processing and managing a system that can be easily reconfigured in case of need. The FPGA is arranged on a VME carrier that hosts two FPGA Mezzanine Card (FMC) ports, see Fig. 1, allowing the possibility to add other hardware functions.

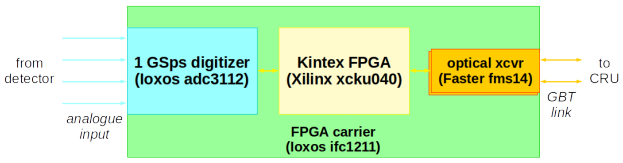

Fig. 1 The readout based on FPGA with two FMC port for the interfacing.

These ports are used to interface with a fast digitizer to acquire the analogue input from the photomultiplier, and for the insertion of a multi – channel optical transceiver to match with the DAQ via optical fibres.

II. MAIN COMPONENTS

The selected digitizer is the commercial adc3112, from the Ioxos company, in FMC format and equipped with 4 analogue channels able to run at a sample rate of 1 GS/s with a 12 b resolution. The sampling clock is jitter cleaned by a two - stage PLL, and the source can be internal from the VCXO, external from the front panel connector or the FPGA via the FMC connector. The converter circuit features a low – pass filter, which is used for noise reduction, and a 2× decimation filter in order to acquire 12 sample per bunch crossing.

The module is equipped with analogue channels with differential DC coupled input, but the input stage can also be software configured as single - ended mode with 50 Ω input resistance. Direct coupling is crucial for the ZDC because the photomultipliers of the detector produce a unipolar signal that evolves only in the negative voltage domain. So to avoid ADC saturation when a signal becomes very large, a positive voltage offset is inserted to exploit the 1 V_{pp} input range.

The selected FPGA carrier is the commercial ifc1211, from the Ioxos company, that is a module in VME format equipped with a PowerPC processor, a Xilinx FPGA and many other interface ports with two FMC. The embedded FPGA is the ku040 from the Kintex UltraScale family, with more than 500 pin dedicated to custom input / output functions.

That FPGA is used to perform online data processing on the samples coming from the digitizer by implementing a custom trigger algorithm, and to serialize the data by handling some serial data links.

III. THE ARCHITECTURE

Each FPGA runs the readout firmware to handle signal samples from the 4 ADC channels. The architecture can be considered flat in the sense that no hierarchically higher entity controls the task of each FPGA, and they do not require to exchange any information with each other. Each FPGA applies a custom trigger algorithm on the data stream coming from each analogue channel, and takes care of the data formatting to comply with the GigaBit Transceiver (GBT) protocol.

The GBT is a custom transmission protocol developed at CERN, based on a serial link running at 4.8 Gb/s, particularly suitable in noisy environments. Each link is a full duplex, meaning it is bi–directional thanks to two optical fibres. The first, in the forward direction, transfers the data, whereas the second, in the reverse direction, carries timing information.

Each readout FPGA, in addition to managing the data stream toward the DAQ, recovers the LHC clock and the trigger messages that are sent on the reverse optical link of the GBT protocol. Then it decodes the information on a secondary communication channel, based on the Single Word Transfer (SWT) protocol, to perform slow control and detector configuration.

During Run 3 the event rate is very high, and the pile-up appears [4] . In other words, it is quite probable that a signal is present on the tail of the previous signal. In such a situation, the selection of the event based on a simple threshold is no longer valid, above all, because to the input dynamics is high up to 1 : 60 considering corresponding signals up to 60 nucleons.

To solve this problem, a custom algorithm was applied to compare close samples with respect to a threshold as in (1), repeated several times:

$$\begin{aligned}&(y_i - y_{i+k} > t) \wedge \\ &\wedge (y_{i+1} - y_{i+k+1} > t) \wedge \\ &\wedge (y_{i+2} - y_{i+k+2} > t) \,.\end{aligned} \tag{1}$$

In practice, the difference between neighbouring samples y_i and y_{i+k} is calculated and, if it is greater than a threshold value t, the related event is a good candidate for acquisition. When this occurs 3 consecutive times, the event is considered interesting, and the acquisition is triggered. The number of conditions that must be verified to trigger is a parameter. To keep the efficiency high, it is possible to loosen the control from a triple to a double condition. The effect of this custom algorithm is that it behaves like a differential threshold or, in other words, it acts like a threshold on the derivative of the signal.

Considering the typical waveforms produced by photomultipliers and the expected rise time of the signals, the values $k = 4$ and $t = 10$ for the algorithm parameters are very likely. Considering that the signals are matched with the ADC input range of 1 V_{pp} and the digitizer resolution of 12 b, the typical threshold is about one – third the amplitude of a single neutron event.

Once the event is considered interesting due to the auto-trigger algorithm or ALICE central trigger, it is tagged with some information, see Fig. 2, and only those events are pushed in the corresponding channel FIFO. Each FPGA handles data from 4 analogue channels and sends the information over two serial optical links providing the necessary bandwidth, so a multiplexer followed by another FIFO is needed to allow the back – pressure.

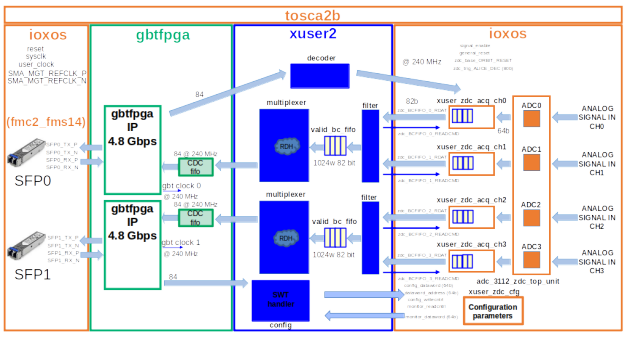

Fig. 2. The firmware architecture implemented managing 4 input channels.

Then the data stream is transferred to the entity implementing the GBT serial protocol at the speed of 4.8 Gbps, where each data word is completed by several redundancy bits for error

correction.

Finally, the two serial data streams are sent to the other FMC module equipped with SFP+ optical transceivers; the same links are used to receive the trigger messages or the configuration parameters.

Due to the slight change in frequency after the proton or ion filling of the LHC ring, it can sometimes happen that the sampling clock becomes different from the transmission clock. For this reason, the Clock Domain Crossing (CDC) FIFO was added to the system to allow for smooth data transfer between different clock regions.

IV. CURRENT OPERATION

The new readout system was installed at CERN in the summer of 2022 and was integrated into the ALICE DAQ chain resulting in full compliance with the experiment requirement. Waveforms from a single pp interaction, observed by one ZN, are shown in Fig. 3. This means that the ZDC can acquire data in auto - trigger mode, as required for LHC Run 3, or with triggers provided by the Central Trigger Processor, as it was in the past.

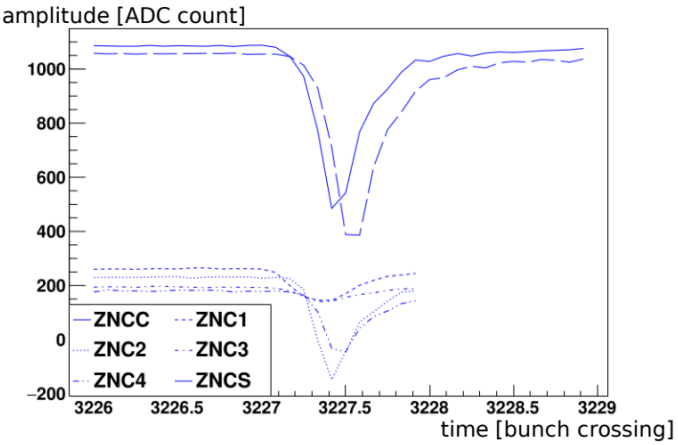

Fig. 3. Example of waveform, where a bunch crossing corresponds to 25 ns.

The commissioning with proton beams was performed last autumn 2022 in special runs at low luminosity, during which ZDC could acquire data thanks to the low value of the crossing angle of the incident beams.

The ZDC then took data together with all other ALICE detectors in november 2022 during the Pb – Pb pilot run.

The standard reference, to assess the quality of the whole ZDC detector, is the amplitude resolution of the peak relative to signals corresponding to events with a single neutron, see Fig. 4. From a preliminary analysis the resolution for the amplitude of the single neutron peak results to be around 15 %, improved with respect to what was achieved in the past Run 2. The peak relating to events with a single neutron is clearly evident and differs from the peak related to other events with 2, 3, 4, 5, .. neutrons [5] .

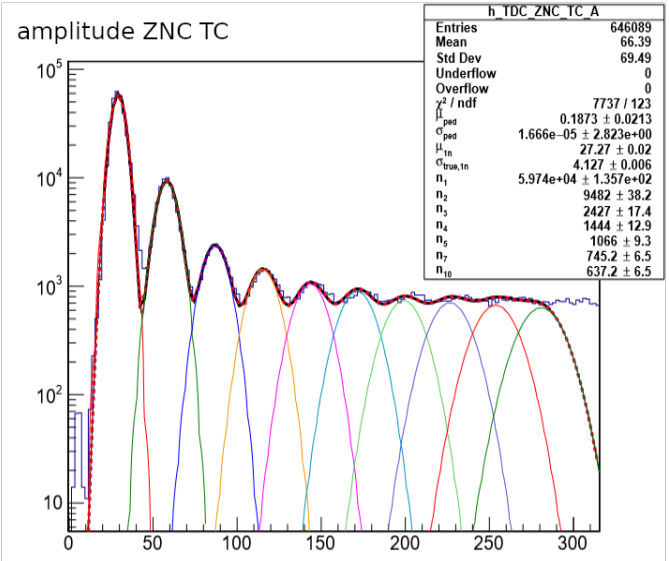

Fig. 4. ZN signal amplitude spectrum in minimum bias Pb – Pb collisions.

V. CONCLUSIONS

A new readout system of the ALICE ZDC detector developed for Run 3 can operate in self - triggered mode without dead time at a rate of 2.5 M event/s with an energy resolution of 15 %.

The hardware is FPGA based, equipped with a commercial 1 GS/s digitizer with a 12 b resolution from Ioxos, and implements a custom auto – trigger algorithm.

The system takes data in the global acquisition and complies with the different acquiring modes foreseen in ALICE; furthermore the full integration within the DCS environment has been completed.

The ALICE ZDC detector is expected to be fully operational during the next Pb – Pb data taking in autumn 2023, providing the event geometry and luminosity measurement.

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