Monolithic Active Pixel Matrix with Binary Counters ASIC with nested wells

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ABSTRACT: **M**onolithic **A**ctive **M**atrix with **B**inary C**o**unters (MAMBO) V ASIC has been designed for detecting and measuring low energy X-rays. A nested well structure with a buried n-well (BNW) and a deeper buried p-well (BPW) is used to electrically isolate the detector from the electronics. BNW acts as an AC ground to electrical signals and behaves as a shield. BPW allows for a homogenous electric field in the entire detector volume. The ASIC consists of a matrix of 50×52 pixels, each of 105x105μm^2. Each pixel contains analog functionality accomplished by a charge preamplifier, CR-RC^2 shaper and a baseline restorer. It also contains a window comparator with Upper and Lower thresholds which can be individually trimmed by 4 bit DACs to remove systematic offsets. The hits are registered by a 12 bit counter which is reconfigured as a shift register to serially output the data from the entire ASIC.

KEYWORDS: monolithic; detector; frontend electronics.

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Contents

1. Introduction

Combining the detector with the signal processing electronics without requirement of bump or other post-fabrication bonding techniques is possible using the Silicon on Insulator (SOI) process. Several designs of pixel detectors with complete in-pixel processing chain for imaging and test structures to explore the properties of the process have been manufactured using the Lapis (OKI) SOI process, available through the SOIPIX collaboration. Detailed tests have led to the conclusion that the process suffers from direct capacitive coupling between the detector and electronics. Hence it requires a careful approach for shielding the detector and electronics from each other.

2. Nested well structure

2.1 Concept

A fully depleted (FD) CMOS SOI 0.2 μm process is the base for this development. The nested well structure is shown in Figure 1. It consists of a buried n-well (BNW) underneath all the electronics which acts as an AC ground to all electrical signals capacitively coupling to BNW. A deeper buried p-well (BPW) allows for a homogenous electric field through the entire detector volume and is the charge collection electrode.

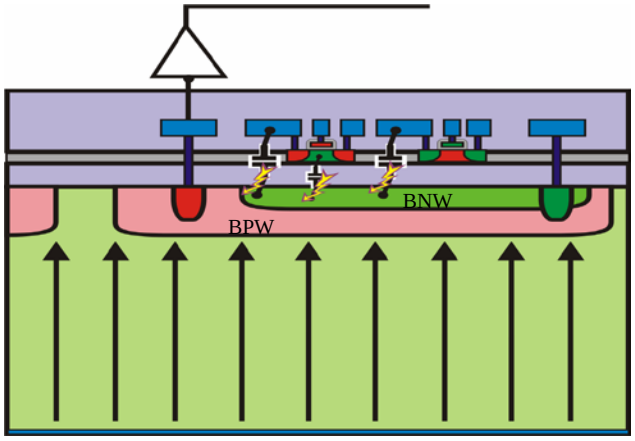

Figure 1 Conceptual view of the nested well structure, where BNW acts as a shield between the detector and the electronics

The nested well structure was collaboratively developed by Fermilab and Lapis Semiconductor Ltd (formerly OKI) and KEK as an effective method of shielding.
The main advantages of the structure includes

- Full isolation of the electronics and the detector charge collection node,
- Electric potential under any circuitry is kept constant at AC ground.
- Allows designs with amplification stages and virtual ground such as charge sensitive amplifier (CSA)
- Removes parasitics feedbacks and instabilities

The main disadvantage of the structure is

- Increased input capacitance of CSA which is directly dependent on the size of the designed pixel.

2.2 Simulation

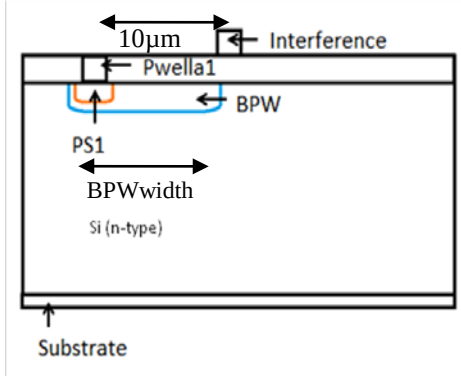

Figure 2 Pixel with Burried P Well (BPW), a step voltage is applied on the interference metal to determine charge coupling from the electronics to the detector

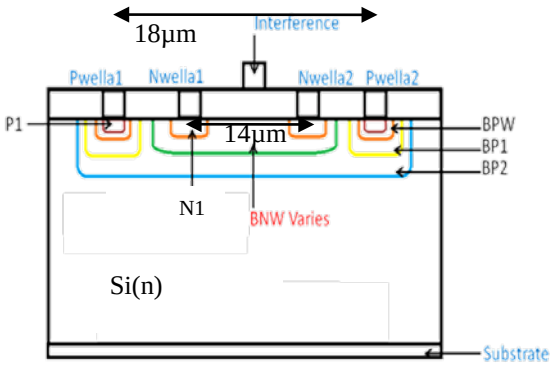

Figure 3 Pixel with nested well structure a step voltage is applied on the interference metal to determine effectiveness of the shielding between the electronics and the detector

The structures showed in Figure 2 and Figure 3 were simulated in Silvaco (device physics solver) to test the effectiveness of the nested well approach. The substrate is connected to a voltage called Die Pad. The interference metal is about 1µm wide. The capacitance between an

interference metal and pwell (BPW) contact increases as the width of the BPW increases and saturates when the interference metal is within the well boundary as shown in Figure 4, it is independent of the Die Pad (DP) voltage. The structure with just the BPW showed that any activity on the interference metal was directly injected into the p-well contact which would then be erroneously treated as an input signal by the amplifier as shown in . A step of voltage of 100mV is applied at the interference metal for various dc bias voltages (V_bias) of 0, 1 & 2V. The charge injected is a function of the BPW width as shown in Figure 5. Hence the nested well structure was developed to overcome these issues.

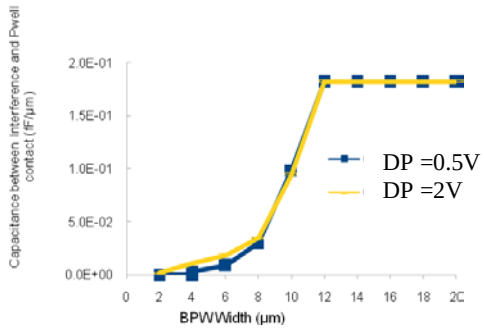

Figure 4 Capacitance between interference metal and pwell contact vs. BPW width which shows that the capacitance is directly proportional to the placement of the interference metal and it saturates once it is outside the well width

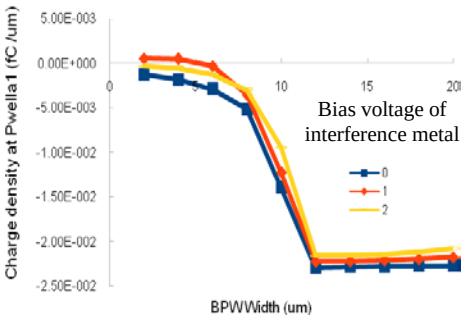

Figure 5 Charge collected at the pwell contact due to 100mV voltage step on interference metal, it is independent of the bias voltage of the interference metal with DP at 0.5V

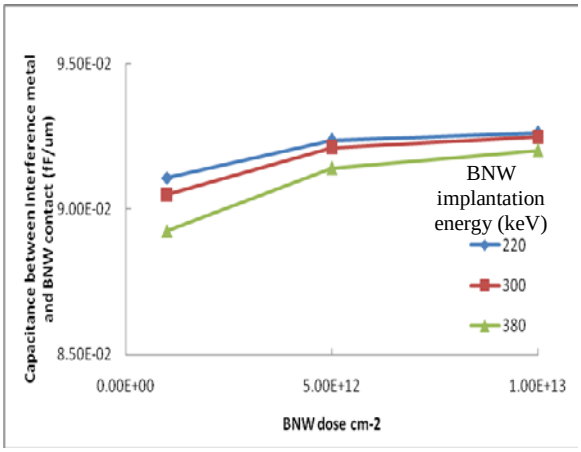

Figure 6 Capacitance between interference metal and BNW contact vs. BPW dose with Vbnw =0.5V and DP =2V, which shows that to lower the well capacitance it is desired to use higher implantation energies, however the change is insignificant.

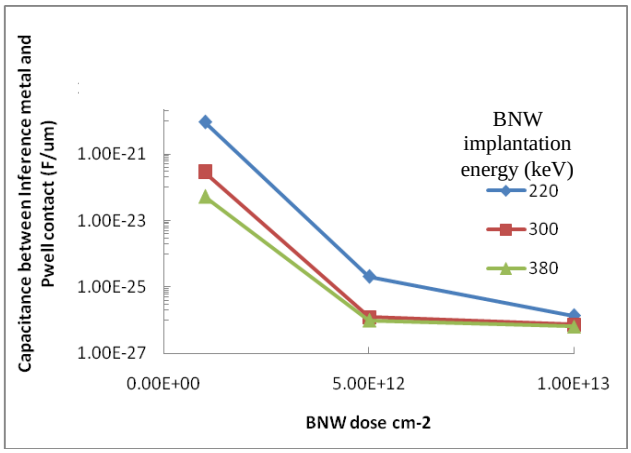

Figure 7 Capacitance between interference metal and pwell contact vs. BPW dose with Vbnw =0.5V and DP =2V, which shows that to lower the parasitic capacitance between the interference metal and p-well contact it is desired to use higher implantation energies and higher doses.

Various simulations are performed for optimizing the capacitances between interference metal and BNW contact and interference metal and pwell (BPW) contact as shown in Figure 6 and Figure 7 respectively. They depend on the combination of doping energies and the doses of Phosphorous in the implanting of BNW. For better shielding it is desired to have as high a dose and implantation energy for BNW as possible which is only limited by its effects on transistors. The diode capacitance (junction of BNW and BPW) is strongly dependent on the size of the designed pixel, namely on the area of the deep BPW and BNW. In the current layout the diode capacitance is approximately equal to 2.1pF for an area of 105µmx105µm; in the final design it is estimated that reducing the size of the pixel by 25-30% while maintaining the same functionality and further optimizing the conditions of doping of the implant will reduce this capacitance to 1 pF or even less. The ASIC was design to study the concept and hence the design and layout was optimized for testability and not for smallest achievable size.

3. MAMBO V ASIC: In-pixel electronics

Monolithic **A**ctive **M**atrix with **B**inary C**o**unters MAMBO V ASIC contains a matrix of 50 x 52 pixels of size 105µm x 105µm and occupies an area of 6mm x 6mm. Each pixel contains analogue functionality accomplished by a charge preamplifier, CR-RC^2 Shaper and a baseline restorer.

The preamplifier and shaper both use a regulated cascode with gain boosting of the input transistor to achieve a high open loop gain. Cascoding is essential in deep submicron processes because channel conductances (g_{ds}) are typically high, resulting in low dynamic resistances below 1MΩ. The preamplifier uses a 14fF feedback capacitance. The shaper uses an active transistor feedback resistance of 28MΩ and the input transistor transconductance (g_m) is equal to 6.5µS. A test capacitance of 1.7fF is connected at the input of the preamplifier for analog calibration.

The pixel also contains a window comparator with upper and lower thresholds which can be individually trimmed by 4 bit current steering DACs to remove systematic offsets. The window comparator consists of two hysteresis comparators and double discriminator logic (DDL). If the output of the shaper is within the upper and lower threshold it is counted as a hit, all other signals are discarded. The hits are registered by a 12 bit counter which is reconfigured as a shift register to serially output the data from the entire ASIC. The pixel contains an analogue and a digital buffer which can be enabled for single pixel tests. It also contains a configuration register, which controls various testing modes and can be used to disable the pixel. The pixel block diagram is shown in Figure 8.

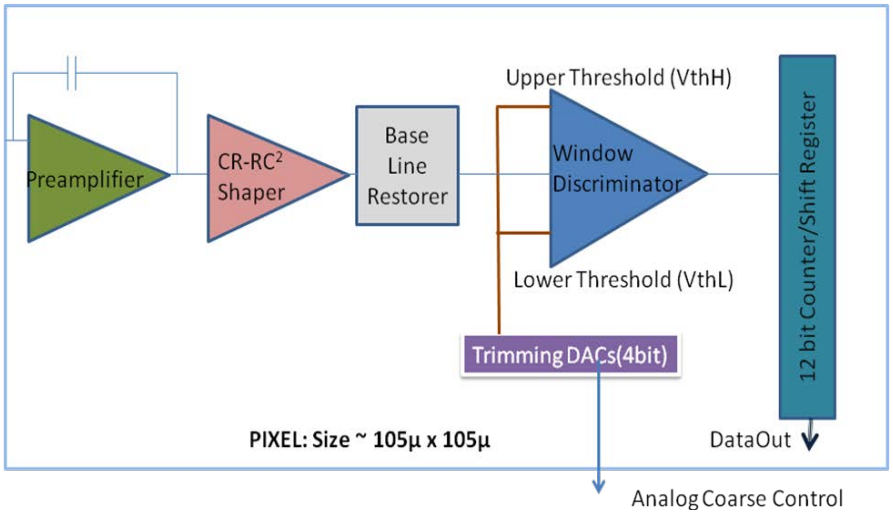

Figure 8 MAMBO V Pixel Block Diagram, each pixel contains a preamplifier, shaper, baseline restorer, window discriminator with 4 bit trimming DACs and reconfigurable counter/shift register

The ASIC can be configured into several test modes such as analog calibration, DAC trimming and counter test modes as shown in Figure 9 to enable efficient characterization tests.

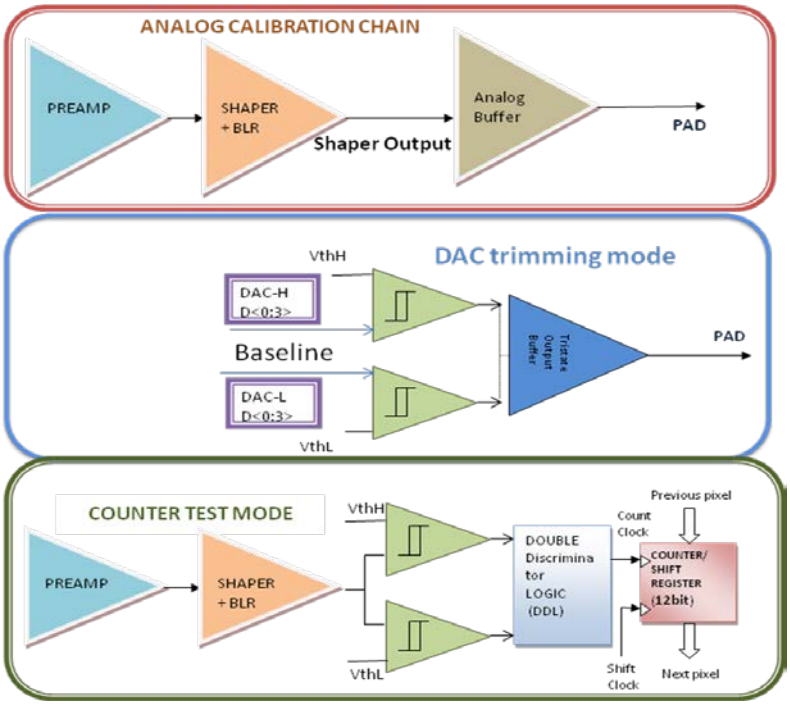

Figure 9 Each pixel of the ASIC can be tested individually in the analog calibration mode, DAC trimming mode or the counter test mode.

4. Tests

A 6x6mm^2 ASIC was manufactured in March 2012 using a Czochralski substrate with less than 1kΩ resistance for a detector area of 5.3x5.3mm^2 and wafer thickness of 325µm. Detector leakage, C/V and I/V measurements were performed for the entire area of the ASIC.

4.1 Detector performance

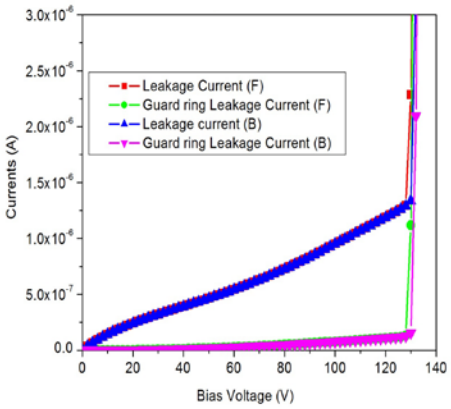

Figure 10 Detector I-V characteristics shows that breakdown occurs at around 130V.

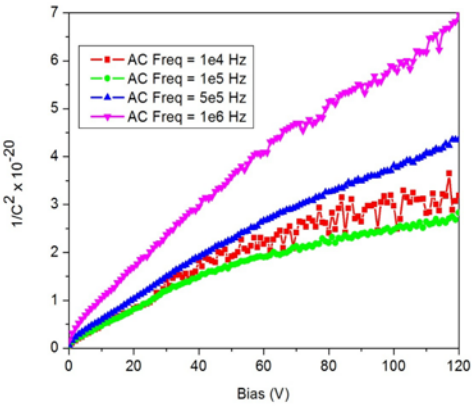

Figure 11 Detector 1/C^2-V characteristics shows that the detector is not fully depleted before breakdown occurs

The detector breakdown voltage is equal to 130V as shown in Figure 10, however as shown in Figure 11 full depletion is not achieved before voltage breakdown occurs. This would indicate that the doping level of the substrate in not adequate and a higher resistivity substrate is desirable.

4.2 Transistor performance in nested wells

The transfer characteristics (I_{ds} vs. V_{gs}) of NMOS and PMOS transistors is plotted in Figure 12 and Figure 13 respectively. As expected the performance of the electronics is independent of the substrate material. For an NMOS transistor of size 41x (0.64µm/0.8µm) and PMOS transistor of size 41x(2µm/0.5µm), the plots indicate that there is no threshold voltage shifts, on increasing the voltage on the Die Pad from 0-100V whereas on increasing the voltage of BNW (V_{BNW}) from 1-5V threshold voltage shift of approximately 100mV for PMOS and 150mV for NMOS transistors is observed, as expected.

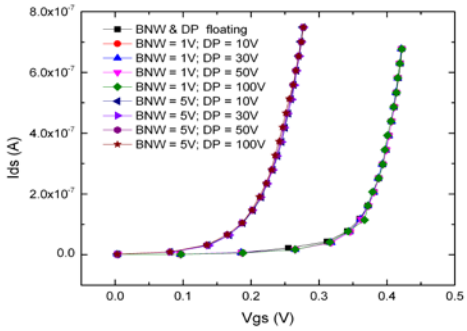

Figure 12 NMOS transistor characteristics, changing Die Pad voltage does not cause any threshold shifts in the transistor. Whereas on increasing the BNW voltage the transistor threshold increases.

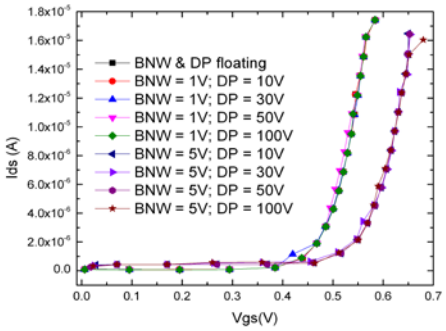

Figure 13 PMOS transistor characteristics, changing Die Pad voltage does not cause any threshold shifts in the transistor. Whereas on increasing the BNW voltage the transistor threshold increases.

4.3 DAC scans

Figure 14 and 15 shows the results of the 4 bit current steering DAC threshold scans for Die Pad (DP) voltages of 2V and 20V respectively, for all the 2600 pixels. The test is performed by connecting one input of the comparator to the shaper output and the other to baseline, which is the reference voltage for the analog signal. The current is varied in both the arms of the comparator by changing the DAC value, the counter records the number of noise hits obtained within a pre-determined time interval. A data set consists of the counter output vs. DAC value for each pixel and repeated 500 times. Each data set is Gaussian fitted and subsequently normalized. All these plots are then averaged at discrete data points corresponding to the DAC value. The tuning range for DAC values from 0000 to 1111 corresponds to ±90mV to ± 200mV for DAC currents ranging from 8nA to 64nA per pixel respectively. The plots show that increasing the DAC current allows for a wider range of offset to be corrected. The results confirm that increasing the Die Pad voltage to further deplete the detector does not alter the transistor performance.

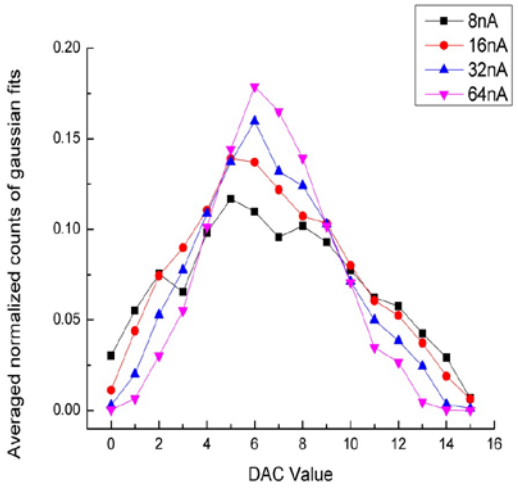

Figure 14 DAC scans at Die Pad = 2V

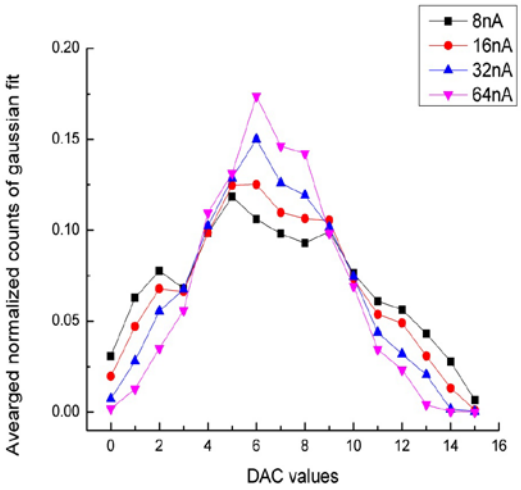

Figure 15 DAC scans at Die Pad = 20V

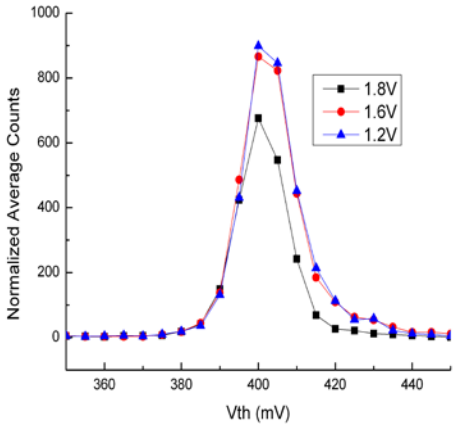

Figure 16 Average Counter output vs. Threshold Voltage for Counter supply voltage of 1.2, 1.6 and 1.8V

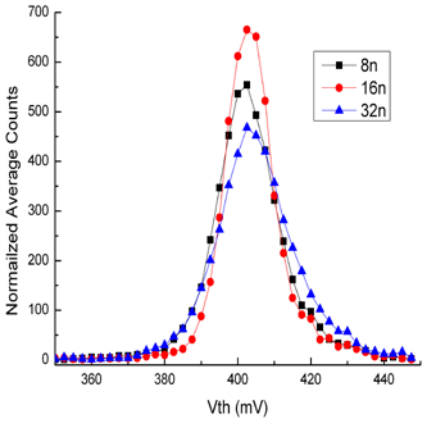

Figure 17 Average counter output vs. Threshold Voltage for DAC pixel currents of 8n, 16n, 32nA

Baseline is set to 400mV and applied as an external voltage to the baseline restorer. The DAC is set at the nominal value obtained from the DAC scans to cancel offset, the lower threshold of the window comparator is scanned to obtain plots shown in Figure 16 and 17 by varying counter power supply and the DAC current respectively. The DAC performance is independent of the supply voltage. Increasing the DAC current allows for a wider range of offset to be corrected, hence it has a slightly broader distribution.

4.4 Imaging

Figure 18 and 19 are images taken with the ASIC with offset cancellation using a ^{109}Cd 22keV source and a 1mm thick tungsten rectangular mask of 1.9mm x 1.9mm, and no mask respectively at a Die Pad voltage of 2V. The shadow around right and lower edge of the images is a result of the PCB obscuring the detector.

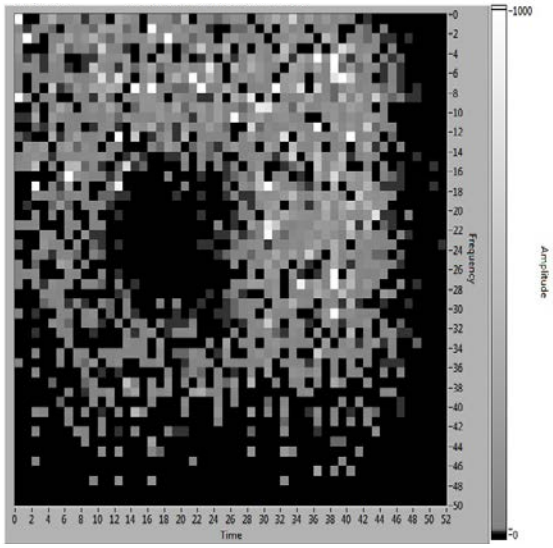

Figure 18 Image with tungsten mask shows that there are no hits where the mask is placed.

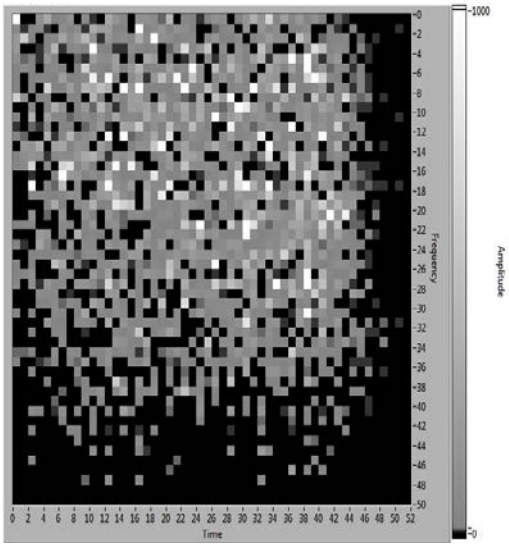

Figure 19 Image without any mask shows hits in the entire area of the ASIC

5. Conclusions

The OKI process is a step toward a new generation of monolithic detectors. Future process optimizations of doping to decrease parasitic capacitance are being performed. Preliminary tests indicate that the nested well structure successfully shields the detector and electronics. Detailed tests are underway of the signal processing chain and the detector- electronics combination.

Acknowledgments

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