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A COMPACT, ULTRAFAST HIGH-VOLTAGE PULSER FOR TRANVERSE ELECTROMAGNETIC KICKERS*

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Abstract

A compact, high-voltage (HV) pulser in the nanosecond regime for transverse electromagnetic (TEM) kickers is presented. TEM kickers are electromagnetic deflectors used in particle accelerators to redirect bunches of particles out of their original trajectory into a new path, such as alternate beam paths, detectors, or other instrumentation devices. The circuit proposed in this design consists of two main portions: a gate driver and a HV switch. The gate driver consists of an isolated and high-speed gate driver, powered by an isolated DC/DC converter with dual output voltages. The HV switch portion was simulated in Ansys HFSS and is composed of a SiC MOSFET, LC resonance components, and specialized diodes. When switched, the MOSFET is used to pump a high voltage into the LC circuit and diode stack, and the ultrafast diode turnoff delivers the final HV pulse to the resistor load. Careful layout techniques were implemented for the MOSFET driver to reduce pulse to pulse instability.

BACKGROUND

All particle accelerators require some form of electromagnetic deflector mechanism to redirect, or kick, particle bunches from their original trajectory into a new path, typically for alternate beam paths, detectors, or other instrumentation devices [1, 2]. These kickers must quickly reach the desired field, maintain that field for a certain time, and then quickly return to zero field. Thus, the drivers need to pump the required current into the kicker impedance, and therefore must operate with nanosecond rise and fall times, adjustable pulse top durations, fast repetition rates, and low jitter. This paper will focus on the design of the driver portion of the TEM kicker consisting of a HV Silicon Carbide (SiC) MOSFET, isolated high-speed gate driver, and an isolated DC/DC converter.

SIC MOSFET CHARACTERISTICS

Compared to their Silicon (Si) counterparts, SiC MOSFETs have different intrinsic material characteristics, summarized in Table 1 [3]. The greater bandgap energy and critical electric field breakdown means higher voltage operation and lower leakage current. Their faster saturation velocity means faster switching and lower power loss, and their better thermal conductivity means better thermals, leading to a smaller die for the same temperature rise. One downside to SiC is their lower electron mobility, which means a higher channel resistance that requires a higher gate drive voltage. These differences make SiC MOSFETS the preferred choice over Si in drivers for kicker designs.

Table 1: Comparison of Intrinsic Material Properties of SiC and Si MOSFETs

Property	Definition	SiC	Si
E_G [eV]	Bandgap Energy	3.2	1.12
E_C [MV/cm]	Critical Electric Field	2.2	0.25
V_s [$\times 10^6$ cm/s]	Saturation Velocity	20	10
μ_e [$cm^2/V\times s$]	Electron Mobility	950	1350
λ [W/cm×K]	Thermal Conductivity	3-4	1.5

GATE DRIVER FOR HV SIC MOSFETS

For this TEM kicker design, a high voltage is required to be supplied to the LC circuit and diode stack that supplies the final HV pulse to the resistor load. Due to the large voltage at the drain of the SiC MOSFET and fast switching, an isolated gate driver is needed to isolate the low-voltage circuitry from the high voltage and to enhance the common-mode transient immunity (CMTI) from high dv/dt. Two common methods for implementing isolation in gate drivers are galvanic and optical isolation.

Galvanic isolation uses a transformer to transmit the gate drive signal across an air gap. The signal that is applied on the primary winding creates a magnetic field in the core, which induces a corresponding voltage on the secondary winding. The main benefits of using galvanic isolation are low propagation delay and not needing any additional bias circuitry. However, the main drawbacks are its relatively larger size and potential for overshoot or ringing on the secondary due to parasitics and large leakage inductance.

Optical isolation uses an LED and phototransistor to transmit the gate drive signal across a barrier. The drive signal is applied to the LED, and the phototransistor converts the received light signal into a corresponding current. This signal is then usually buffered by a CMOS circuit to provide the final gate drive output. Compared to galvanic isolation, the drawbacks are its larger propagation delay and need for bias circuitry. However, the primary benefits of a smaller footprint, minimal parasitics, and lack of overshoot or ringing on the output is critical for TEM kickers.

PROPOSED GATE DRIVER DESIGN

A simplified schematic diagram of the proposed design of a HV SiC MOSFET gate driver for TEM kicker is shown in Fig. 1. For the HV SiC MOSFET, Microchip's MSC080SMA330B4 was selected due to its high voltage breakdown of 3.3 kV and lower total gate charge across the gate-to-source voltage range when compared to other alternatives with that high of a breakdown voltage.

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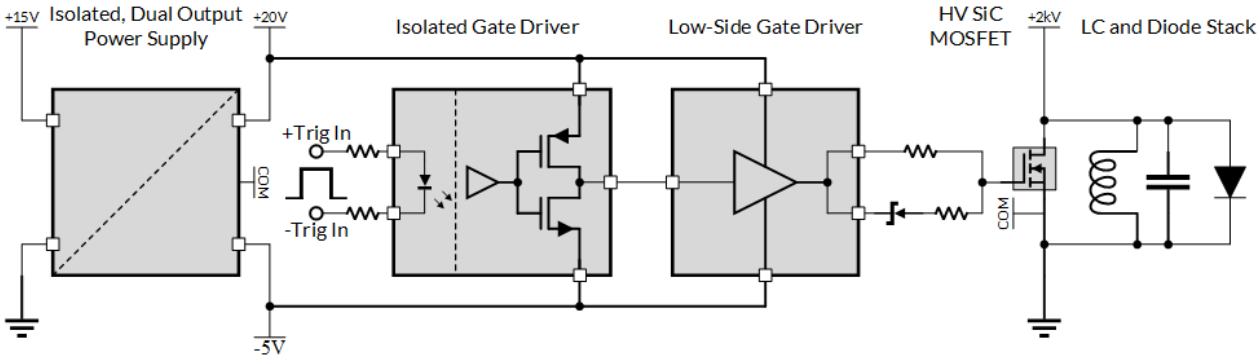

Figure 1: Simplified schematic diagram of proposed HV SiC gate driver with LC and diode stack details omitted.

For the gate driver, an isolated gate driver cascaded with an ultrafast low-side gate driver was used. To achieve the isolation, Skywork's Si8261BCD-C-IS was chosen for its 5.0 kV isolation and unique internal two-die structure that's separated by an isolation barrier. This device functions similarly to traditional opto-isolators but with substantial improvements to propagation delay, internal parasitics, EMI, and CMTI. Cascaded is Littelfuse's IXDN614SI, which can source and sink 14 A of peak current to provide the final gate drive signal to the HV SiC MOSFET. Both drivers do not need to be referenced to ground and are powered by a single, isolated, dual-output power supply.

The power supply chosen was RECOM's R15P22005D. This is an isolated, +20/-5 V dual output, 2 W power supply with a 6.3 kV isolation voltage and a low 3 pF isolation capacitance. This provides the turn-on and hard turn-off gate voltage for the HV SiC MOSFET, and the low isolation capacitance limits displacement current caused by high dv/dt during switching [4]. The common return of the power supply was connected to the SiC MOSFET's kelvin source to reduce the overall inductance and impedance of the gate driver's return path and lower the switching losses.

PCB LAYOUT CONSIDERATIONS

Due to high voltage and current slew rates, SiC MOSFET gate drivers are more susceptible to creepage, crosstalk, false turn-on, parasitic resonances, and EMI when compared to Si counterparts. To minimize that, careful layout techniques such as placement of slots, modified component pads, a compact gate drive loop, polygon pours, and proper placement of reference planes were used. The completed layout of the gate driver is seen in Fig. 2.

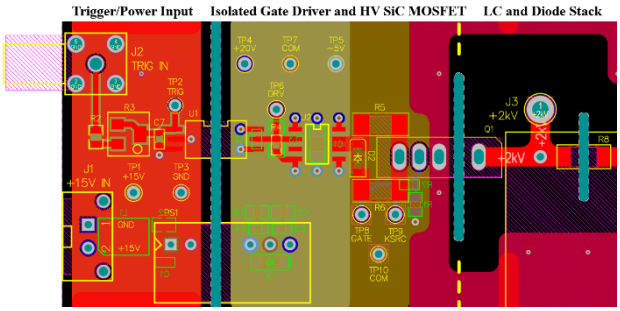

Figure 2: Layout of HV SiC MOSFET gate driver circuit.

EXPERIMENTAL RESULTS

The top view of the completed PCB prototype is shown in Fig. 3. The PCB was built with a standard laminate and prepreg material, Ventec VT-47. The total area of the input, gate driver, and HV SiC MOSFET is 2.21 in. × 1.36 in.

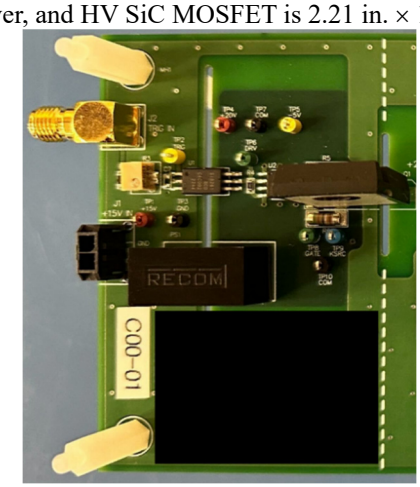

Figure 3: Top view of the HV SiC gate driver prototype. LC and diode stack portion of PCB omitted from view.

This gate driver design successfully drives the 3.3 kV SiC MOSFET at 320 kHz with a required pulse top, achieves a 27.0 ns rise time and 24.0 ns fall time, and exhibits minimal overshoot with no ringing. All the gate driver measurement results are summarized in Table 2. The rising and falling edge of the gate drive pulse waveform are shown in Fig. 4 and Fig. 5, respectively. In those below waveform captures, channel 1 in yellow is the input trigger signal, channel 2 in green is the gate drive signal, and channel 3 in blue is the gate signal of the 3.3 kV SiC MOSFET.

Table 2: Results of HV SiC MOSFET Gate Driver

Parameter	Description	Value
t_{pLH} [ns]	Propagation Delay, Low-High	75.5
t_{pHL} [ns]	Propagation Delay, High-Low	90.5
$t_{r,drv}$ [ns]	Rise Time, Gate Drive	12.0
$t_{f,drv}$ [ns]	Fall Time, Gate Drive	12.0
$t_{r,gate}$ [ns]	Rise Time, MOSFET Gate	27.0
$t_{f,gate}$ [ns]	Fall Time, MOSFET Gate	24.0

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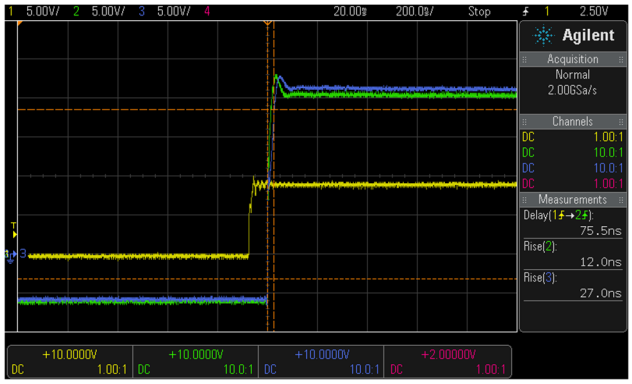

Figure 4: Rising edge of the gate waveform.

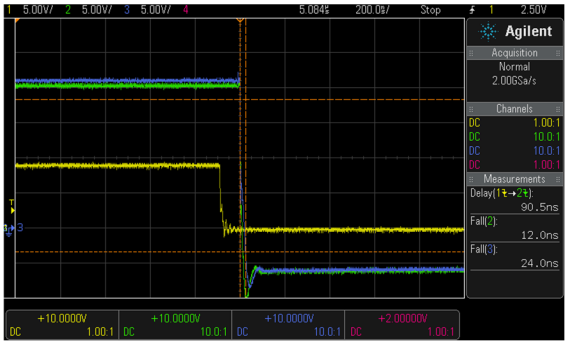

Figure 5: Falling edge of the gate waveform.

Results of the final HV pulsed output of the driven LC and diode stack into a 50-ohm kicker impedance are summarized in Table 3. A continuous wave (CW) run is shown in Fig. 6 and a zoomed view is in Fig. 7. In those below waveform captures, channel 1 in yellow is the HV output and channel 2 in blue is the current.

Table 3: Results of LC and Diode Stack HV Output Pulse

Parameter	Description	Value
$V_{pk,HV}$ [kV]	Voltage Peak	2.0
$t_{r,HV}$ [ns]	Rise Time	4.1
FWHM [ns]	Full Width at Half Max	7.5

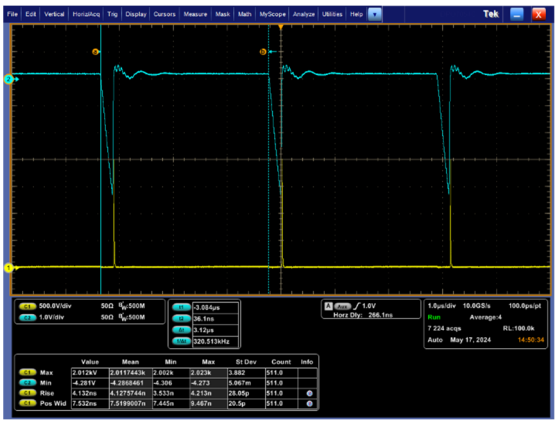

Figure 6: Final pulsed HV output of a 320 kHz CW run. Blue trace is a transient in the LC circuit. Yellow trace is the final HV pulsed output showing practically no residual power between neighbor pulses.

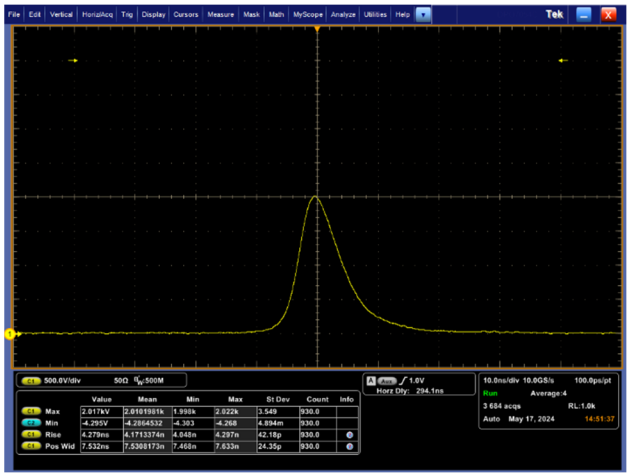

Figure 7: Zoomed view of final pulsed 2.0 kV output. A 70.0 V, 3.2 A power supply is used to produce this output.

CONCLUSION

In this paper, the proposed design of a HV SiC MOSFET gate driver for TEM kickers was presented, specifically to control the camshaft bunch orbit in the storage ring. TEM kickers are electromagnetic deflectors used in particle accelerators that require nanosecond rise and fall times, controllable pulse top durations, fast repetition rates, and low jitter. A prototype gate driver for a 3.3 kV SiC MOSFET was designed and built, and successfully delivered an ultrafast and stable pulse to the TEM kicker. The driver pulse was stable at 320 kHz, had a 27.0 ns rise time and 24.0 ns fall time, and exhibited minimal overshoot and no ringing. With only a supply of 70.0 V and 3.2 A, a final HV output pulse of 2.0 kV with a 4.1 ns rise time was achieved. Future work must be done to increase the gate driver bias power by designing a custom, isolated, dual output power supply to fully enable 1 MHz operation in CW mode.

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