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# DIRECT RF SAMPLING PROCESSOR FOR CAVITY BPM SYSTEM*

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*Abstract*

Digital beam signal processor is critical for the beam diagnostic resolution and on-line application performance. High speed & high precision ADC, high performance FPGA are the key devices for the evolution of the processor. At present, ADC technology has entered the era of RF direct sampling, which bandwidth is up to 9 GHz, sampling rate is higher than 2 GSPS, and sampling bits is up to 14 bits. If the beam signal is sampled directly and processed with an FPGA, the beam diagnostic system structure will be much more concise and stable. In this paper, a developed direct RF sampling processor for beam diagnostic in SXFEL and SSRF will be introduced, and the first application on cavity BPM system will be shown.

## INTRODUCTION

FEL is a well-known source of short pulse, high power x-ray beams with a high degree of radiation coherence. In order to achieve a high gain FEL lasing state, a precise overlap of the electron beam with the radiated photon beam is needed. Therefore, precise measurement of the beam position is required. Cavity BPM(CBPM) can meet the requirement for high resolution beam position measurements because of its coupled beam signal has the character of high signal to noise ratio (SNR).

A strong resonant cavity field is excited when beam passes through the cavity, including a TM010 monopole mode and a TM110 dipole mode. The TM010 is proportional to the charge of the bunch, while TM110 is proportional to the transverse offset of the beam relative to the electrical center of the cavity and charge [1]. The cavity output signal can be expressed as Eq. (1):

$$V_p = V_{out} \cdot e^{-t/2\tau} \cdot \sin(\omega t + \varphi) \quad (1)$$

Where $V_p$ is the output signal amplitude, $\tau$ is the decay constant, $\omega$ is the cavity central frequency and $\varphi$ is the phase when the bunch passes through the cavity.

## SUPERHETERODYNE RECEIVER VS DIRECT RF-SAMPLING

The central frequency of the cavity is generally in the GHz range, for example, the center frequency of CBPM in SXFEL is about 4.7 GHz.

Limited by ADC performance, the traditional cavity BPM electronics is based on superheterodyne receiver structure, which mixing the radio frequency (RF) signal down to an intermediate frequency (IF) signal or baseband signal firstly, then digitizing with an ADC.

Except for commonly used filters, amplifiers and adjustable attenuators, the RF front-end of the superheterodyne receiver system contains a local oscillator (LO) module and a mixing module. The RF front-end is usually complex, especially for LO's frequency synthesizer and mixing module. Too many analog components make the CBPM system vulnerable to environment changes and introduce measurement noise, also the cost is high and requires more stable install space [2].

The ideal signal processing electronics is digitizing RF signal directly and processing signal in digital domain. RF-sampling ADC makes this goal getting closer. Figure 1 compares high IF superheterodyne receiver to a direct RF-sampling receiver [3]. The direct RF-sampling receiver is noticeably simpler.

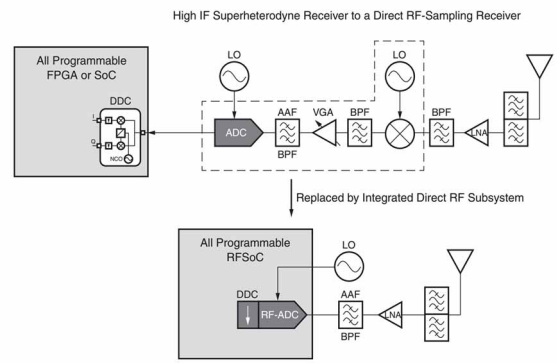


Figure 1: Superheterodyne receiver VS direct RF-sampling.

## DIRECT RF-SAMPLING CBPM ELECTRONICS

Figure 2 depicts the block diagram of direct RF-sampling CBPM electronics.

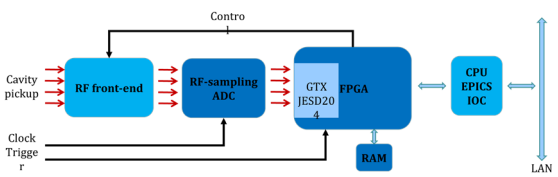


Figure 2: Block diagram of direct RF sampling.

The digital signal processing system mainly includes two parts: sampling and digital signal processing [4].

In sampling section, ADCs evolve rapidly. Currently, some high-performance ADCs have sampling rate of several GHz and bandwidths of 10 GHz. Table 1 lists some

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ADCs on the market. Then the CBPM signal in L/S/C band can be sampled with the ADCs directly.

Table 1: The RF-Sampling ADCs On Market

| Type | Sampling rate (GSPS) | Bandwidth (GHz) | Sampling bits |
|---|---|---|---|
| AD9208 | 3 | 9 | 14 |
| AD9213 | 10.25 | 6.5 | 12 |
| AD9209 | 4 | 8 | 12 |
| AFE7444 | 3 | 6 | 14 |
| AFE7900 | 3 | 7.4 | 14 |
| AFE7950 | 3 | 12 | 14 |

In digital signal processing section, the JESD204B serial interface standard supports 12.5 Gbps data transmit speed between ADCs and FPGA, which makes real-time data transmission and processing in FPGA is possible. Nowadays, powerful FPGA contains hard ARM cores, rich peripheral interfaces and massive logic resources, which can realise complex signal processing algorithms.

## *Direct RF-Sampling Processor*

The RF-sampling processor mainly includes a MPSoC FPGA carrier board and a four channels RF direct sampling ADC daughter board. The bandwidth of ADC is 9 GHz, sampling rates is 2.6 Gsps, sampling bits is 14. The FPGA is XCZU15EG, which contains 4 hard ARM cores, rich logic computing resources and 24 16.3 Gb/s GTH transceivers. Figure 3 is the photo of the processor.

Figure 3: Direct RF sampling processor.

## *ADC Performance Evaluation*

We set up a test bench with RF signal source in the laboratory to evaluate the performance of the processor. The input continuous signal frequency is 4.7 GHz, ADC sampling rate is 1.904 GHz. Figure 4 shows the results.

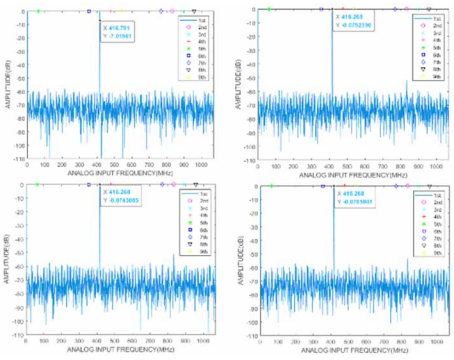

Figure 4: Four channel evaluation results.

Channel 1's detailed parameters are as following:

- SINAD=40.1907 dB
- SNR=41.1336 dB
- THD=-47.2868 dB
- SFDR=52.0934 dB
- SFDR2=52.0934 dB
- ENOB=8.21388

The ENOB of all four channels are above 8 bits.

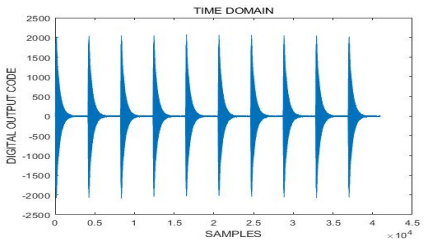


Figure 5: Sampling result in lab.

A vector signal generator is used to generate a pulsed exponentially decaying RF signal to simulate a CBPM signal. Figure 5 shows the captured raw data waveform with the processor in self-trigger mode.

## *Beam Test On SXFEL*

An on-line CBPM beam test was carried out on SXFEL with the processor.

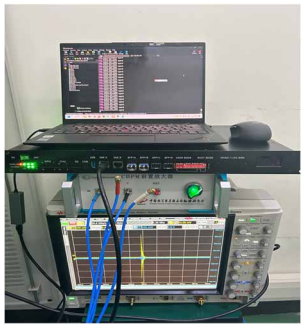

Figure 6: Beam test with direct RF processor.

Figure 6 is the field picture. The CBPM locates at the end of SXFEL. A RF front-end including only 4.7 GHz bandpass filters and amplifiers is connected between the pickups and the processor. The input clock was 119 MHz synchronized with the SXFEL RF and the sampling clock is 1904 MHz after the phase-locked loop (PLL) multiplication on the processor.

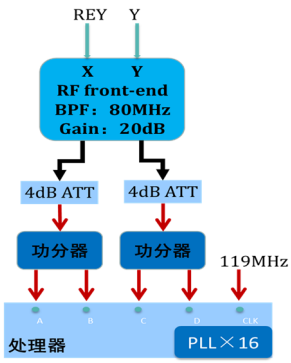


Figure 7: Block diagram for the SXFEL processor resolution measurement.

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Figure 7 shows the schematic diagram of the test. Firstly, the BPM signal is filtered by a 4.7 GHz BPF to eliminate noise, amplified by 20 dB gain, then attenuated by 4 dB and split into two ways and finally fed into the processor [5].

Figure 8 (left) shows the sampled raw data waveform and the right is the frequency spectrum of signal.

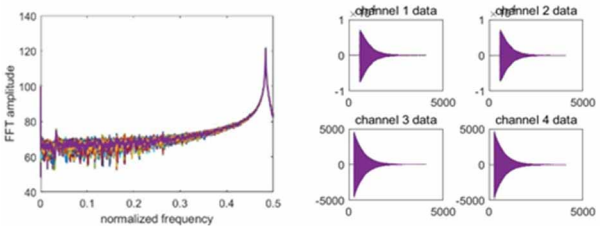


Figure 8: Raw waveform (left), frequency spectrum (right) of the sampled cavity BPM signal.

## *Signal Processing*

Three signal processing algorithms were used to process the sampled data in Matlab to evaluate the relative resolution, namely FFT, Hilbert and DDC. Figure 9 shows the relative resolution with the sum points of calculated results under different algorithms. All results are better than the 0.1% requirement. The FFT is 0.017%, the Hilbert is 0.005% and the DDC is 0.008% respectively. The algorithms are list as follows.

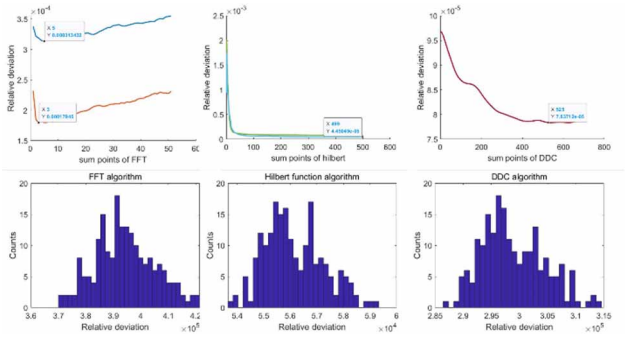


Figure 9: Results of three algorithms.

- FFT

$$X(k)=DFT[x(n)]=\sum_{n=0}^{N-1} x(n)\, W_N^{kn},k=0,1,\ldots,N-1$$

- Hilbert

$$\hat{x}(t)=x(t)*h(t)$$

$$\tilde{x}(t)=x(t)+j\hat{x}(t)$$

$$\tilde{X}(jw)=\begin{cases}2F(jw), & w \geq 0\\ 0, & w < 0\end{cases}$$

- DDC

$$S_I(t)=\frac{1}{2}I(t)+\frac{1}{2}I(t)\cos(2\pi * 2f_0t)-\frac{1}{2}Q(t)\sin(2\pi * 2f_0t)$$

$$S_Q(t)=\frac{1}{2}Q(t)+\frac{1}{2}I(t)\sin(2\pi * 2f_0t)-\frac{1}{2}Q(t)\cos(2\pi * 2f_0t)$$

$$\hat{I}(t)=\frac{1}{2}I(t)$$

$$\hat{Q}(t)=\frac{1}{2}Q(t)$$

## CONCLUSION

The RF direct sampling processor shows the relative resolution is much better than 0.1% for cavity BPM on SXFEL. It means that direct RF-sampling electronic can be built for CBPM in FEL to improve the system structure, for example SHINE which is still under construction. Next step is to develop the firmware and software on the processor to make it work on line, and design a new RF front-end module to build a RF direct sampling CBPM system.

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