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Status and prospect of the ATLAS TGC electronics upgrade for HL-LHC

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The trigger and readout electronics for the Thin Gap Chamber (TGC) detector at the ATLAS experiment will be replaced to fully exploit the physics potential of HL-LHC. For a flexible and highly efficient trigger algorithm, the new on-detector boards transmit data of all TGC hits at every bunch crossing to the off-detector boards to reconstruct muon tracks. In 2025, a major milestone was achieved: the completion of the fabrication and quality check (QC) of the on-detector boards. This document describes the design of the new system and the QC testing of the readout board, one of the TGC on-detector boards.

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1. Introduction

The ATLAS experiment at High-Luminosity LHC (HL-LHC) is planned to start operation in 2030 [1]. To cope with the increased collision rate, the Thin Gap Chamber (TGC) electronics [2], responsible for the endcap muon trigger, needs to be upgraded [3, 4]. A schematic overview of the TGC electronics system is shown in Figure 1. The system consists of the Amplifier-Shaper-Discriminator (ASD) boards, the Patch-Panel ASIC and Sender FPGA (PS) boards, JTAG AssisTance Hub (JATHub), Timing Alignment Master (TAM), and Sector Logic (SL) boards. The TGC electronics except for the SL are located on the on-detector side, while the SL is installed on the off-detector side. The PS board and Patch-Panel ASIC (PP ASIC) play a key role in the TGC data collection for the muon trigger and need to be operational for ten years. The system requires 1,434 boards and 11,472 chips, respectively. This document reports an overview of the PS board and the QC testing of the PP ASIC and PS board in mass production.

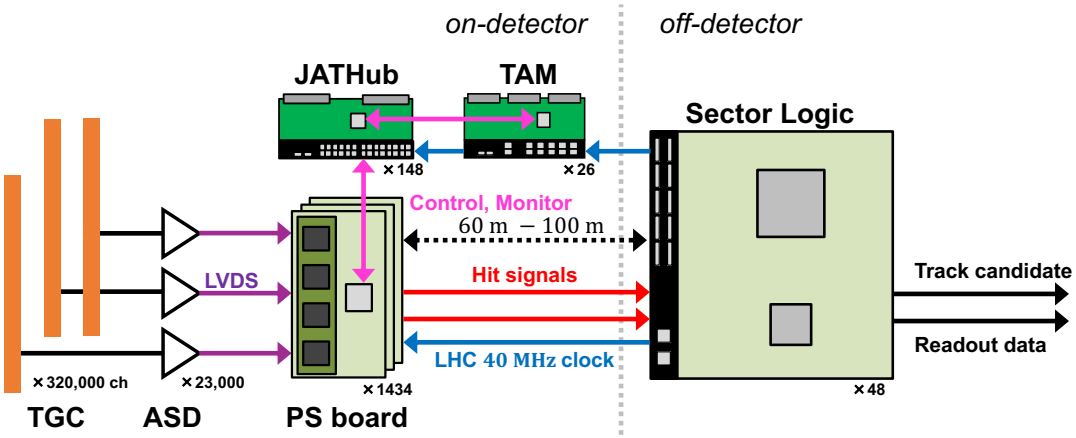


Figure 1: Schematic overview of the TGC electronics system. The PS board, JATHub, TAM and SL are developed for HL-LHC. The full TGC system has 320,000 channels. Each of 23,000 ASD boards receives muon hit signals from 16 channels. Each of 1,434 PS boards is connected with up to 16 ASD boards. Each of 48 SL boards is connected to a maximum of 29 PS boards and manages the processing of about 7,500 channels. The system includes 148 JATHubs, each connected to up to 11 PS boards. In addition, 26 TAM modules are used, each connected to up to 6 JATHubs.

2. Patch-Panel ASIC and Sender FPGA (PS) board

The PS boards collect all TGC hit signals in the system. The board is equipped with eight Patch-Panel (PP) ASICs, a Kintex-7 FPGA [5], a flash memory, a clock jitter cleaner (Si5395), two SFP+ transceivers, two DACs and an ADC to function as a readout board, as shown in Figure 2. The FPGA receives LHC 40 MHz clock distributed from SL via optical fibers and recovers it with a fixed latency. The jitter of the recovered clock is attenuated on Si5395. The PP ASICs align the hits timing exploiting variable delays and synchronize the hits with the LHC 40 MHz clock, where each hit is assigned to a bunch crossing. The FPGA forms hit bitmaps of 256 channels and transmitted to the SL via optical fibers. The flash memory of the PS board stores the FPGA firmware and also the control parameters, including the signal delay, the gate width, and signal masks. The parameters are configured by SL and distributed to each element at particular triggers,

e.g. the FPGA reconfiguration, serial links lost and transceiver reset signals [6]. The DACs drive the threshold voltage supplied to the discriminator on the ASD boards, while the ADC monitors this voltage. Radiation tolerance tests of the main components and the board [7] have been completed. In addition, the functionality has been validated through integrated tests with other TGC interfaces.

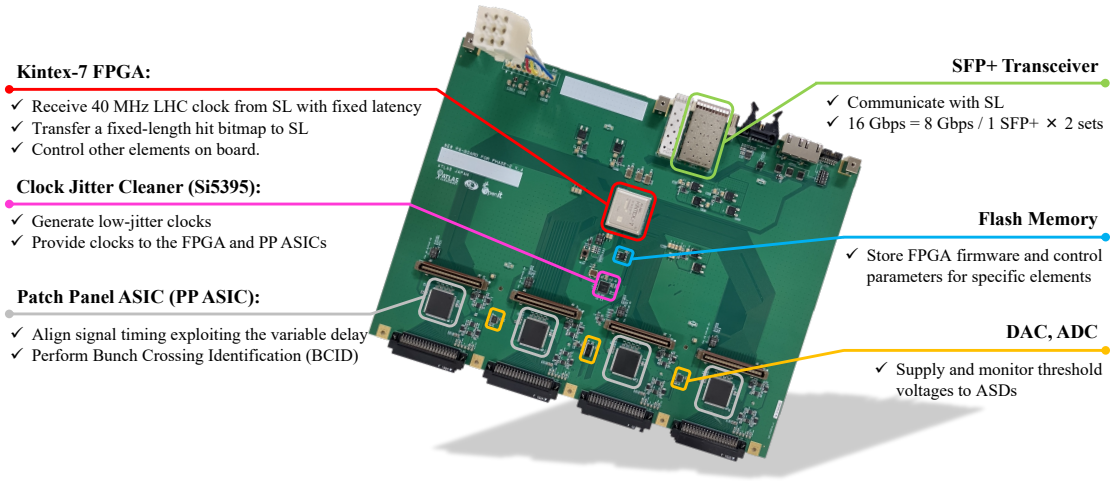


Figure 2: Overview of the PS board design (mother board). The board consists of a mother board and a daughter board, each of which mounts four PP ASICs.

3. QC testing for PP ASIC

Overview PP ASICs have several roles:

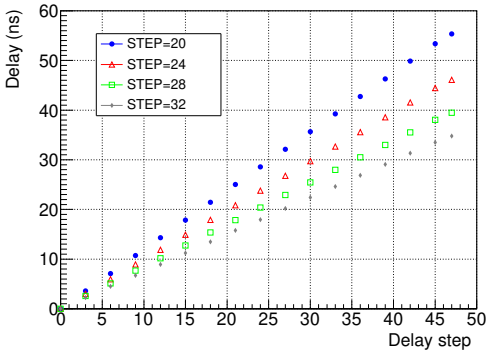
1. Receive LVDS signals from ASDs
2. Compensate for delay difference among channels due to time of flight of muons and cable length using PLL and variable delay[1]
3. Synchronize the signal with the LHC 40 MHz clock and identify the bunch crossing
4. Generate test pulse to ASD for tests of readout chain

To meet the timing requirements in the system, the delay compensation must achieve a timing control resolution below 1 ns, and a dynamic range[2] exceeding 40 ns.

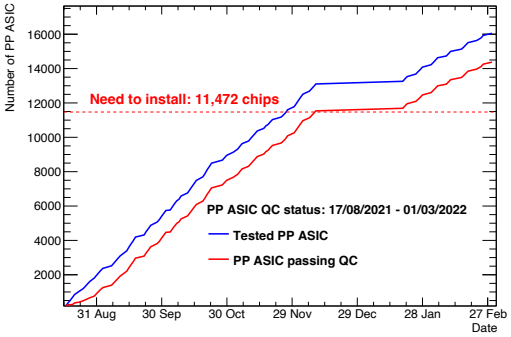
Result Figure 3(a) shows the measured delay of the variable delay depending on the number of delay units for a reference clock of 40 MHz. By changing PLL STEP, we can change the dynamic range and the resolution of the variable delay. The linearity is confirmed for all PLL step configurations. The PLL STEP 24 meets the requirements: the delay per step is less than 1 ns, and the dynamic range exceeds 40 ns. The QC testing achieved the required number of units for TGC installation, as shown in Figure 3(b).

[1] A common delay cell design is employed both in the PLL and variable delay circuits, controlled via a shared bias voltage adjusted by the charge pump. The signal propagation delay through the ring structure is approximately 25 ns. The number of delay cells (PLL step) used in the PLL is selectable from 20 to 32 steps.

[2] The maximum timing difference among channels in the current experiment is 26 ns.



(a) Measured propagation delay of the variable delay depending on the number of delay steps, shown as a typical result obtained from one PP ASIC. The results are presented for PLL STEPs 20, 24, 28, and 32.



(b) The QC result over time. The blue and red curves represent the cumulative number of tested chips and those passing QC, respectively. The red dashed line indicates the target number of chips required for installation.

Figure 3: Results for mass production PP ASICs.

4. QC testing for PS board

Concept and Design The QC testing system is required to evaluate the complete functionality of the PS board, including the full chain of hit signal readout, control, and monitoring, in combination with the ASD and JATHub boards (Figure 4). An initial single-board testing system [1] was developed to establish the framework. However, since testing a single board took approximately 40–50 minutes, this setup posed a bottleneck in throughput. To address this limitation, the system was upgraded to support parallel testing (Figure 5), significantly improving efficiency. In the new configuration, a JATHub master controls 10 JATHub slaves within a single test station. One JATHub handles JTAG communication, while the remaining nine handle other software-based testing items in parallel. Each test station is capable of testing up to 18 PS boards simultaneously. By operating two such stations concurrently, the performance of 36 boards can be evaluated in a single test cycle.

Result The QC testing performed based on the items of Figure 4 achieved the required number of units for TGC installation, as shown in Figure 6.

5. Conclusion

In this study, the QC testing for the mass production of PP ASICs and PS boards was conducted using dedicated testing systems. This system are comprehensive and thorough enough to evaluate the full functionality of the chips and boards. The tests were successfully performed on schedule. The passing rates are 14,375 / 16,054 for PP ASIC and 1,483 / 1,490 for PS board. This result satisfies the TGC installation requirement and the readout system is ready to meet the 4000 fb^{-1} of data-taking requirements of the HL-LHC experiment.

[1] User can access a Zynq SoC device mounted on one JATHub to evaluate one PS board.

1. **JTAG communication:**
   Write/read firmware to QSPI Flash Memory.
2. **Control parameters configuration and distribution:**
   Write parameters to QSPI and distribute them to the elements (DAC, PP ASIC).
3. **Recovery function:**
   Reconfigure FPGA by JATHub.
4. **Voltage monitoring (DAC, (x)ADC, power good):**
   Check proper operating values from register readout values.
   Configure DAC = 70 mV for this test.
5. **Clock phase measurement**
   Measure the clock (40 MHz) from the Si5395 using the reference clock (40 MHz) of JATHub.
6. **ASD testpulse test:**
   Check if hit signals are returned with the correct timing for 256 channels.

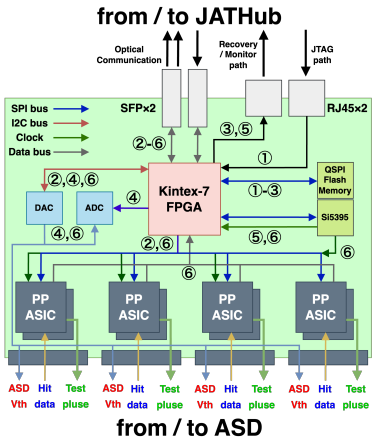


Figure 4: Mapping between the QC testing items and the PS board design. Each test item corresponds to a specific lane involved in the main functionalities of the PS board.

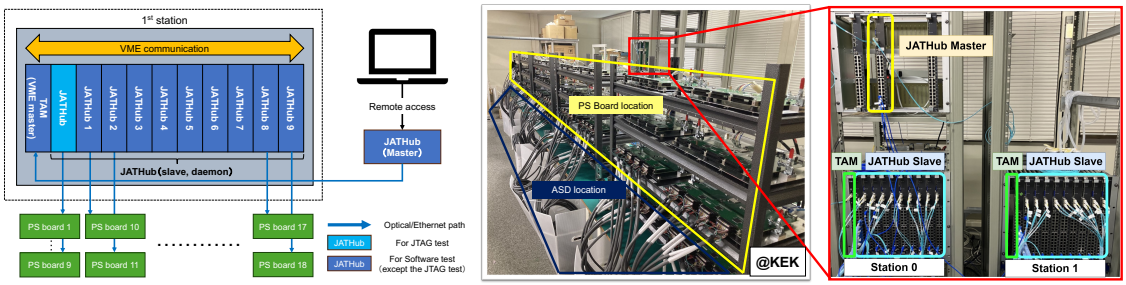


Figure 5: Overview of the QC testing design for PS board. The block diagram illustrates the system architecture, where a JATHub master controls 10 JATHub slaves within a single test station. One JATHub handles JTAG communication, while the remaining nine handle other software-based testing items in parallel. Each test station is capable of testing up to 18 PS boards simultaneously. Photos show the actual setup with two test stations.

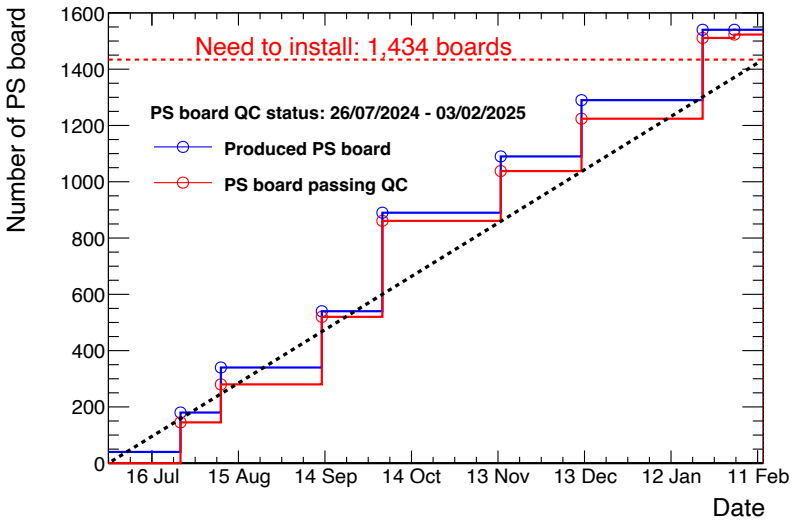


Figure 6: The QC result for mass production of PS boards over time. The blue and red lines represent the cumulative number of produced boards and those passing QC, respectively. The red dashed line indicates the target number of boards required for installation.

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