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A readout system based on SiPM for the dRICH detector at the EIC

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Abstract: The ePIC experiment at the future Electron-Ion Collider (EIC) aims to use silicon photomultipliers (SiPMs) as the photodetector technology for the dual-radiator ring-imaging Cherenkov detector (dRICH). Despite their advantages for this low light application and insensitivity to high magnetic fields, SiPMs are sensitive to radiation and require rigorous testing to ensure that their single-photon counting capabilities and dark count rate are kept under control over the years of

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operation. The presented results show the successful use of a complete prototype readout chain based on the ALCOR chip for SiPM characterization measurements and assembled in an optical plane for test-beam measurements using the dRICH prototype.

Keywords: Modular electronics; Front-end electronics for detector readout; Cherenkov detectors; Solid state detectors

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1 Introduction

The Electron Ion Collider is a future accelerator to be built at the Brookhaven National Laboratory in the early 2030s [1, 2]. The EIC will be the first collider designed for polarized electrons, polarized protons, and light nuclei. With its high center-of-mass energy (20 to 141 GeV) and large luminosity (10^{34} cm^{-2} s^{-1} for electron-proton scattering), it will enable scientists to explore the quark and gluon structure of protons and nuclei, helping to understand the origin of nuclear spin and mass. ePIC is the main detector, it is placed at the interaction point 6 and it will be built around a superconductive solenoid magnet with a magnetic field up to 1.7 T. Around that, a serie of subsystem is built for tracking, calorimetry and Particle IDentification (PID). PID is a significant challenge and the proposed solution for the forward region is a dual radiator Ring Imaging Cherenkov (dRICH) detector [3]. This dRICH is considered a compact and cost-effective choice to cover a wide range of particle momenta, from a few GeV/c up to 50 GeV/c, typical of the forward rapidity region, achieving 3σ K/π separation. As the name suggests, the detector exploits two Cherenkov radiators: aerogel and gas (C_2F_6) with refractive indices of 1.02 and 1.0008 respectively. The Cherenkov rings are reflected by an array of 6 spherical mirrors onto 6 optical readout sectors for a total surface of 3 square meters. The optical readout is required to have a spatial resolution of 3×3 mm^2 (that defines the photosensor pixel dimension) for a total of about 300,000 channels. The photosensors must be capable of efficiently detecting single photons within a high magnetic field of around 1 Tesla, while withstand mild radiation levels that are on the order of 10^{11} 1-MeV neq/cm^2 for the entire life of the experiment. Interestingly, the photosensors are placed outside of the detector's acceptance region, offering the opportunity for exploring the use of silicon photomultiplier sensors (SiPMs). The SiPMs are highly sensitive to photon detection, have excellent time resolution [4] and represent a cost-effective solution. Importantly, SiPMs, being solid state devices, are not affected by high magnetic fields. However, it's worth noting that SiPMs have their drawbacks, having intrinsic high dark count rates (DCR) at room temperature and being susceptible to radiation damage [4]. The radiation damage can lead to a significant increase in dark currents thus DCR levels, reducing the sensor life-span. However, the effect on the DCR can be mitigated with annealing techniques [5].

In order to study the radiation damage (and the recovery by different annealing techniques) to SiPMs and evaluate their detection capability after irradiation, we have developed a prototype of the readout system for future implementation into the dRICH detector. We tested several SiPMs from different vendors arranged in a $4 \times 6/8$ matrix mounted on a custom carrier PCB with fluences up to 10^{11} 1-MeV neq/cm^2. In order to keep the DCR low, the SiPMs are cooled down to $-30\,^{\circ}$C by means of peltier cells. To maintain flexibility, bias voltages are independently supplied to each SiPM through an adapter board. The signals from the SiPMs are routed to the front-end board, where an ALCOR ASIC [6] amplifies and timestamps them, generating a digital stream sent to an FPGA. In the following sections, we provide a description of the individual components of the readout system, along with results from the irradiation campaigns and the initial use in a prototype dRICH detector.

2 Material and methods

Carrier board and SiPMs. We designed four kinds of carrier boards specially engineered to accommodate different $3 \times 3\,\text{mm}^2$ SiPM devices that underwent several irradiation and annealing phases. The primary specifications for this carrier board are to withstand high-temperature oven annealing processes (up to 175 °C), to facilitate precise temperature control for the SiPM devices (-30 °C), and to enable high-current operations during annealing techniques involving high current delivered to the SiPMs. Furthermore, these carrier boards were also designed with the capability to perform imaging in a dRICH prototype. The high-temperature endurance was achieved by using a high Tg PCB material and employing high-temperature reflowing paste during the soldering process. Additionally, the connection between the carrier board and the adapter board was established using an edge connector, effectively eliminating the use of plastic components in this critical interface. This design choice ensures that the carrier board, once dismounted from the prototype, can withstand temperatures of up to 175 °C for annealing and remains resilient and functional afterward. To maximize thermal conduction with the peltier cell during −30 °C operations, the back side of the 8-layer PCB features full metalization exposure with no solder resist. Precise temperature control is achieved through the use of an LM73 temperature sensor, allowing for accurate setting and monitoring of the operative temperature. An essential characteristic of the carrier board is the absence of resistors in the bias voltage path. This design choice facilitates the passage of high currents through the SiPM sensors for the current annealing technique. Instead of resistors, a ferrite bead (1 kΩ at 100 MHz) is used in conjunction with 100 nF capacitor to cut high frequency noise on the bias line. As for the SiPM sensors, one board is outfitted with 16 Hamamatsu S13360-3050VS (50 µm cell pitch) sensors and 16 Hamamatsu S13360-3025VS (25 µm cell pitch) sensors, one board is equipped with 16 Hamamatsu S14160-3050HS (50 µm cell pitch) sensors and 16 Hamamatsu S14160-3015PS (15 µm cell pitch) sensors. Of the remaining two boards, one houses 12 NUV-HD-CHK sensors (40 µm cell pitch) and 12 NUV-HD-RH prototype sensors (15 µm cell pitch) provided by Fondazione Bruno Kessler (FBK) while the other 16 SENSL MICROFJ 30035 (35 µm cell pitch) and 16 SENSL MICROFJ 30020 (20 µm cell pitch). These diverse sensor configurations enable comprehensive experimentation and performance assessment across varying cell pitch sizes, breakdown voltages and vendors.

Adapter board. The carrier with the SiPMs is connected to an adapter board thanks to a robust Samtec mini edge card connector. This board is engineered to fulfill three primary functions. Firstly, it regulates the voltage bias (Vbias) of SiPMs across eight distinct bias lanes. Secondly, it provides precise polarization bias to each SiPM sensor, using digital-to-analog converters (specifically, the LTC1665) to fine tune the voltage at the anode from 0 to 5 V. Thirdly, it hosts 32 1 nF capacitors for AC coupling with the subsequent front-end board. The control is ensured via a I2C communication with an external board connected to a computer via a RS-232 to USB. The adapter board allows to efficiently supply the Vbias to SiPMs with different overvoltages on the same carrier board, and to individually switch-off noisy channels.

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Front-end board and ALCOR. The front-end board is connected to the adapter through a micro low-profile Samtec connector. Beyond the connector and voltage regulators, the board is equipped with the ALCOR ASIC (developed by INFN Torino), originally designed for SiPMs in cryogenic environments. ALCOR is wire bonded on the board and has a 32-pixel matrix mixed-signal architecture, which integrates amplification, signal conditioning, and event digitization with fully digital input and output capabilities. Each pixel on the chip consists of a regulated common gate amplifier with a 10 Ω/5 nF input impedance, a post-amplifier TIA configurable for four different gain settings, two independent leading-edge discriminators with customizable threshold settings, and four time-to-digital converters (TDCs) featuring 50 ps least significant bit (LSB) resolution at a 320 MHz sampling rate. A schematic representation of the internal architecture is shown in figure 1 (left). ALCOR operates in three triggerless modes: LET for leading-edge threshold measurement with a maximum time stamp rate up to 5 MHz, ToT for Time-over-Threshold measurements, and slew rate measurements for signal characterization. The ASIC provides a fully digital output via four LVDS TX data links, employs SPI-based chip configuration, and generates 64-bit event and status data word. A dedicated Xilinx Kintex-7 FPGA KC705 evaluation board is used to provide the clock to up to 6 ALCORs, program them and receive the LVDS data trough Samtec FireFly high speed cables. The system is controlled by a Linux PC. The fully assembled board is shown in figure 1 (right).

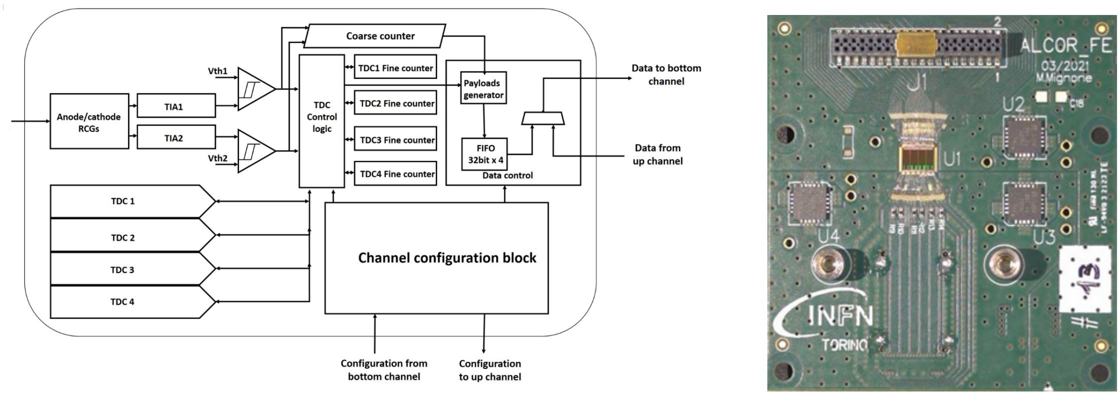

Figure 1. Schematic representation of ALCOR ASIC (left). Front End board with ALCOR clearly visible in U1 (right).

Optical plane prototype. The readout system is assembled as depicted in figure 2. The carrier board connects to the adapter, which is positioned above the front-end board. This configuration reduces the system's form factor and, by mounting the adapter on top of the front-end, the wire-bonded ASIC is kept protected. The optical plane prototype is assembled with four readout systems that have distinct SiPM matrixes (one for each vendor) each previously irradiated with a dose of 10^{10} 1-MeV neq/cm^2 and subjected to a 150 hours annealing phase at 150 °C. To lower the DCR by a factor $\approx$ 100, SiPMs are operated at −30 °C. This is done by using two peltier cells stacked in series connected to each matrix pair. The current delivered to the stack is controlled by a software-implemented PID process, using the LM73 sensor's temperature measurements as feedback. The peltier cell's hot side is connected to a liquid cooled heat pipe (15 °C) using a thermal pad. The setup has 2 L P M of nitrogen gas circulation to prevent moisture and frost, while neoprene is employed to isolate from light the junction between the dRICH and the detector box. Figure 3 (left) shows the system assembled in the detector box with the carrier boards facing upwards and the adapter boards attached to them. The front end boards are located below the adapter boards. Water pipes and cables are on the back as in figure 3 (right), where the prototype is connected to the dRICH described in [7].

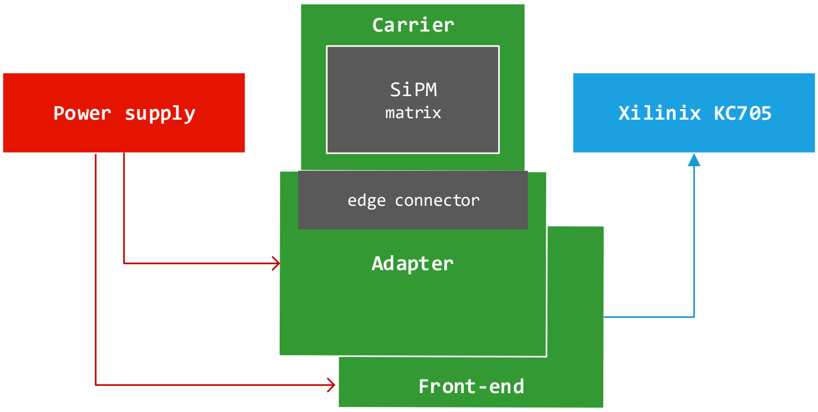

Figure 2. Schematic representation of the readout system. The carrier board hosting the SiPM matrix is connected to the adapter board by using an edge connector. The front-end board is placed below the adapter reducing the form factor and protecting the wire-bonded ASIC. The connection to the power supply and FPGA are also shown.

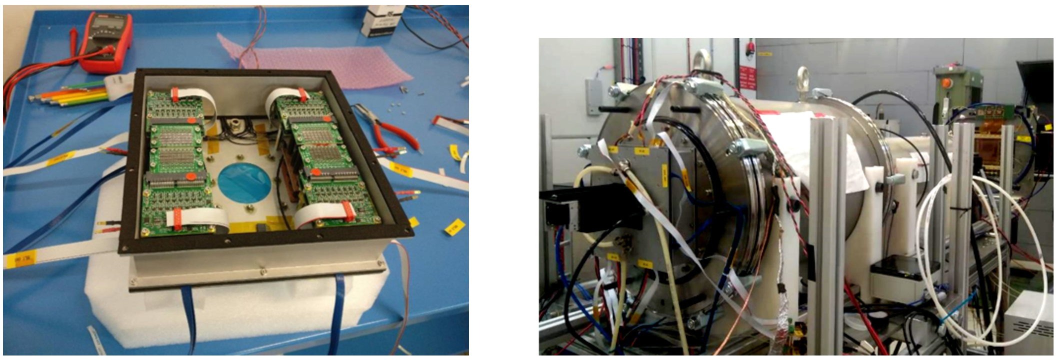

Figure 3. Optical plane prototype (left). Optical plane connected to the dRICH prototype at the T10 beam line of the CERN Proton Synchrotron (right).

3 Results

The readout prototype was used in a climatic chamber kept at $-30\,^{\circ}$C for the studies on the radiation damage on more than 200 SiPMs. The DCR exhibits a linear increase with rising fluence, and it subsequently decreases following high-temperature annealing. The reduction is approximately a factor of $\approx$10 after annealing at 125 °C and about a factor of $\approx$100 after annealing at 150 °C. Both the annealings were performed for 150 hours. All the sensors display a similar trend but Hamamatsu S13360-3050VS consistently demonstrates the lowest DCR across all stages, starting at $\approx$1.5 kHz as brand new and increasing to $\approx$500 kHz for sensors exposed to 10^9 1-MeV neq/cm^2 before annealing. After the annealing the DCR is 15 kHz. The sensors exposed to 10^{10} 1-MeV neq/cm^2 and 10^{11} 1-MeV neq/cm^2 resulted after annealing in a DCR of $\approx$ 1.5 MHz and $\approx$ 150 kHz. In alternative, on-board

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annealing was induced by using direct current to heat up the SiPMs up to 175 °C (10 V and 100 mA per sensor) for 2.5 hours. The temperature feedback is achieved by using a thermal camera and we measured a reduction in DCR of a factor 10 was measured. This is less than what was obtained with the oven at 150 °C but in 1/10 of the time. The photo response of the Hamamatsu S13360-3050VS sensors was measured before and after irradiation and annealing observing no degradation in performance within a 5% margin (further details in [8]).

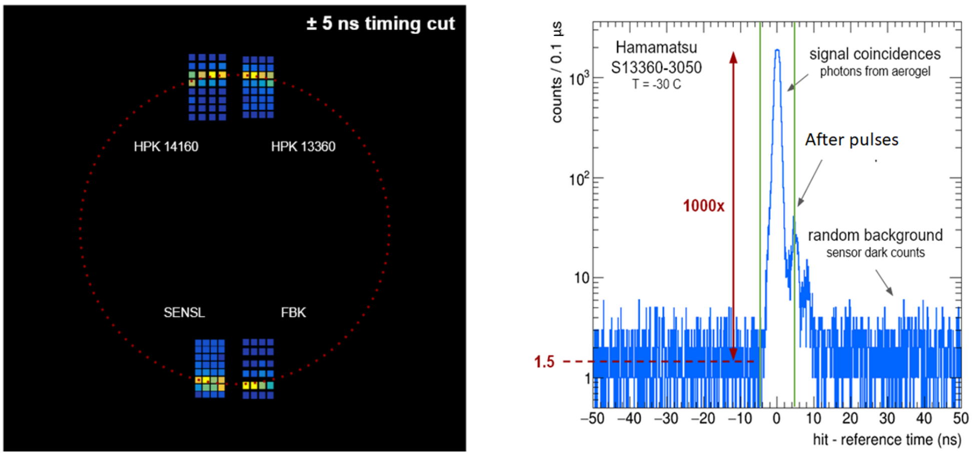

Figure 4. Cherenkov ring obtained in the dRICH prototype by the aerogel with negative 8 GeV/c beam (left). Time coincidence plot for the Hamamatsu S13360-3050VS (right).

Four sensor matrices irradiated up to 10^{10} neq/cm^2 that underwent the oven annealing (150 °C for 150 hours) were integrated in the dRICH optical readout prototype and tested at the CERN Proton Synchrotron. The optical readout prototype is able to detect Cherenkov rings (figure 4 (left)) using a 10 ns time window centered on a trigger signal provided by the same readout connected to plastic scintillators. By looking at the time coincidences (figure 4 (right)) one can see the 15 kHz of DCR in the off-trigger region while a gain in signal of a factor 1000 is detected in coincidence with the trigger. The time resolution for the Hamamatsu S13360-3050VS peaks at 350 ps. After pulses are present and are within the expectation (1/100 probability).

4 Conclusion

In this paper, we have provided a comprehensive overview of the individual components comprising a SiPM-based readout system designed for the dRICH at the ePIC experiment at the EIC. Using this system, we successfully characterized SiPMs that had undergone irradiation and annealing through both indirect heating methods, such as oven annealing, and direct current-induced heating. The latter method serves as a proof of concept, demonstrating the feasibility of achieving in-situ annealing during EIC operation. In-situ annealing, aimed at reducing the dark count rate induced by radiation damage, has the potential to significantly extend the photodetection system's lifespan, by a factor of at least ten. Furthermore, we achieved the measurement of Cherenkov rings generated by the interaction of the beam with the dRICH prototype, showcasing the system's ability to do imaging with 350 ps time resolution with irradiated and annealed SiPMs.

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