national accelerator laboratory

TM-354
0431

BOOSTER AND MAIN ACCELERATOR PHASE-DETECTOR SYSTEM FOR CAVITY TUNING

E. F. Higgins

February 29, 1972

SUMMARY

Each booster and main accelerator rf station receives a low-level (2 W) reference rf excitation signal containing frequency, phase, and amplitude information. The reference signal is amplified by tunable power amplifiers (100 kW) and applied to resonant beam-line cavity gaps. Continuously tuning the cavity to resonate at the reference rf excitation frequency is a requirement for bunch acceleration and is accomplished with a cavity tuning-control feedback loop. The elements of the control loop are configured as a phase-locking system.

The phase sensor in the control loop is a broad-bandwidth large-amplitude dynamic-range phase detector. The phase detector develops a feedback "error" signal proportional to the phase difference between the rf reference signal and the beam-line cavity sample rf signal.

This memorandum contains a brief discussion of the cavity tuning feedback loop, describes the phase-detector circuitry, and outlines a set of procedures for checking the performance of the detector at recommended 4-month intervals.

PHASE-LOCK LOOP

The booster and main accelerator cavity tuning phase-lock feedback system adaptively adjusts each beam-line resonator frequency to an rf-excitation signal transmitted from a fan-out source point in each machine. The source of the rf-excitation signal is a voltage-controlled oscillator, one for the booster and a separate one for the main accelerator. These VCOs are conditioned and controlled in closed-loop operation by computer and/or beam-dependent machine inputs.

Fig. 1 is a functional representation typical of the booster and main accelerator cavity tuning phase-lock loop, and shows the major elements in the loop. The beam-line cavities are tuned by controlling the magnitude of the current supplied to ferrite-loaded tuners physically attached and electrically coupled to each cavity. A 2,500-ampere programmable bias supply functions as a driver for these tuners.

The phase detector, shown in Fig. 1, measures the phase difference between an ANODE (output quantity) rf signal representing the beam-line phase, and a CATHODE (input quantity) signal representing an excitation or reference phase. ANODE and CATHODE signal-monitor devices, together with associated

phase-detector interconnection components and cabling, are carefully equalized to establish a specific signal delay and phase slope throughout the operational frequency band applicable to each machine. Phase equalization is set so as to permit the ANODE-RF signal phase to match the CATHODE-RF reference signal phase only when the beam-line cavity resonant frequency corresponds to the reference frequency. Since the ANODE-RF signal is derived from a Hi-Q single-pole selective circuit, the phase response of this signal exhibits a single "zero" at the resonant frequency of the cavity. Because of the equalization mentioned, the phase detector generates and thereafter introduces a loop tuning voltage which has an odd functional relationship about the "zero" phase response of the ANODE-RF signal. The detector-produced error voltage is transmitted via the programmable bias supply to the ferrite tuners which adjust the resonant frequency until the ANODE and CATHODE-RF signal phase angles are equal.

This feedback process "locks" the beam-line cavity frequency to the excitation reference signal frequency, maintaining the tuned relationship as the excitation frequency follows the proton velocity change during each acceleration cycle.

In addition to the voltage derived by the phase detector through the output/input comparison, a curve generator derived command voltage, representing a "best estimate" of the required frequency vs time function, is also introduced into the feedback loop. The command voltage is summed with the phase-detector

output signal in circuits located within the programmable bias supply. The command voltage markedly reduces the overall system error (deviation of the system output from the desired value) and aids in rapidly "locking" the phase-lock loop. The general effect of the command voltage is to increase the overall loop gain without introducing an unwanted low frequency roll-off which would deleteriously affect loop stability.

Some of the advantages in configuring the beam-line cavity tuning loop as in Fig. 1 are:

1. Under locked conditions, correspondence between the required excitation rf frequency and cavity resonant frequency is achieved automatically.
2. Adaptive frequency tracking of the cavity is achieved by the phase-lock technique without the need for ancillary aids, such as frequency discriminators, comb filters, or frequency switching circuitry.
3. The phase-lock loop functions as a narrow-band tracking filter (cross-correlator) which has inherent high-noise immunity.
4. Since the beam-line cavity is maintained at resonance during tracking (cavity impedance resistive) the possibility of beam-line gap rf voltage phase changes due to a cavity reactive impedance jitter is minimized.
5. The effective locked-loop phase tracking error (difference between excitation signal phase and beam-line gap phase, divided by excitation signal phase) is reduced due to the increased gain provided by the addition of a command voltage.

PHASE-DETECTOR CIRCUIT DESCRIPTION

The phase detector shown in Fig. 1 contains two independent gain controlled rf channels, a phase-sensitive demodulator, circuits which amplify and multiplex the phase-error signal with other signals, and the necessary dc power supplies to operate all modules.

In order to function in the control loop described, the phase detector is designed to maintain a transfer function which is essentially independent of the frequency and the amplitude modulations present at its rf input ports. The phase detector is made to respond to only the phase-modulation content of the rf inputs.

Frequency modulation exists at the phase-detector inputs in accord with the booster or main accelerator requirement for tracking the velocity change of the protons, i.e., the frequency is swept in a nonlinear way between 30 and 52.8 MHz for booster and between 52.8 and 53.2 for the main accelerator. Amplitude modulations at the phase-detector rf input ports are dissimilar in peak amplitude, modulation factor, and spectral content. The detector is designed to maintain its output functional relationship, E_{out} = 10 sin (phase difference angle) volts, throughout the above ranges in the input frequency and also for a 40 dB change in the amplitude of either or both rf inputs. The 40 dB dynamic part of the input range has some latitude in maximum level and can be set anywhere between the rf input signal levels of 25-V P-P and 25-mV P-P. The useful range over which the unit will operate is therefore 60 dB.

Acceleration for both machines takes place only during a portion of the total repetition interval, consequently, the feedback loop will alternately close during acceleration time and open during dead time. For this operational condition it is desirable to remove the phase detectors' control voltage during the dead time in order to exclude the possibility of spurious signals and noise entering the control loop. The dead time, however, is an appropriate interval for the introduction of other possible signals such as clamping, zero setting, initialization, command/control, or diagnostic functions.

The phase detector utilizes a time multiplexer circuit to allow the introduction of signals of the type mentioned. The multiplexer disconnects the phase error signal path at the beginning of the dead-time interval and connects the output port of the unit to another signal path which can contain analog information related to the above functions.

Monitor-signal ports on the front and rear panels of the phase detector permit local and control-room observation of the error voltages within the unit.

A detailed tabulation of the electrical, mechanical, and environment requirements for the phase detector is contained in Engineering Specification ES-5024-0331.00 dated November 20, 1970. A block diagram is shown in Fig. 2.

rf-Input Coupling Devices

The ANODE and CATHODE-RF signals enter the phase detector through 3-way reactive hybrid-junction power splitters. These

splitters furnish rf samples of the inputs to viewing ports on the front of associated RMU modules and to level set attenuators RF-1 and RF-2 on the phase detector. In addition, the ANODE splitter transmits an ANODE signal sample to a multiport fan-back combiner which produces a signal representing the SUM of all cavity gap voltages. The third port of the CATHODE splitter is used for local diagnostics and must be terminated at the splitter by a 50-ohm coaxial terminator. The fan-back SUM signal is used for control-room viewing and operational diagnostics. The 3-way splitters are designed for a 50-ohm system and each split output port is designed to phase track other ports within 0.5 deg throughout the 30 to 54 MHz range.

The level set attenuators RF-1 and RF-2 permit the positioning of the phase detectors' dynamic range between the 25-V and 25-mV levels mentioned and these also set the maximum amount of signal applied to the AGC rf amp. Under operational conditions, RF-1 and RF-2 are adjusted to obtain an rf signal level of 0.25 V P-P at their output ports (input to AGC rf amp) when terminated in 50 ohms.

The technique used to produce attenuation for the RF-1 and RF-2 components is through longitudinal and rotational displacement of two coils wound on 3/8-inch diameter facing ferrite half-cores. With core faces aligned, the cores are separated by an amount to provide a fixed 20 dB insertion loss. The angle made between coil axes is mechanically adjustable. The overall transfer function of the units related to this angle

(smaller angle θ) is:

$$V_{RF\ OUT} = \frac{V_{RF\ IN}\ COS\ \theta}{10}\ Volts.$$

The nominal range of continuous adjustment is 20 dB. Specific attenuation values are indicated by color dot on the body of the unit as follows:

Color	Total Attenuation (dB)
Black	20
Brown	21
Red	22
Orange	23
Blue	26
Brown-Black	30
Red-Black	40

The RF-1 and RF-2 attenuators are designed for a 50-ohm system and are paired so that the insertion phase differences are less than 1 deg, and tracking error with attenuation and frequency variation are less than 1 deg in the 30 to 54 MHz band.

AGC-rf Amplifier

The AGC-rf amplifier units are matched in gain and phase to 1 dB and 1 deg, and gain controlled by separate feedback and feedforward control paths. The 1-dB response points are at 26 and 56 MHz, respectively.

The AGC-rf amplifiers incorporate two vacuum tube gain control stages using RCA Nuvistors, type 7895. One stage is functionally located at the input while the second is located near the

output end of the amplifier. A transistor amplifier using 2N2219 transistors is used between control stages to supply a minimum of 23 dB of fixed gain and a minimum of 30 dB isolation between the Nuvistor control stages. A nominal 20 dB of control range is provided by each Nuvistor stage. Nuvistors are used for the control stages because of the negligible variation in input/ output phase with gain programming. Phase compensation of the control stage phase is necessary, however, to secure some margin beyond the 20 dB value, which necessitates grid bias approaching the cut-off bias of the tube. Phase compensation of the control stages is achieved by a feedforward transformer coupled circuit which adds a grid voltage component to the anode circuit. The added component is just sufficient to cancel the unwanted grid-anode capacitively coupled rf component. The resultant phase of the stage then becomes insensitive (to less than 1 deg) to grid-bias control over a minimum of a 23-dB gain range. Nuvistor cathode followers are used to couple the control-stage rf voltage to the base circuits of the transistor interstage amplifier to minimize control stage loading.

The transistor-interstage amplifier has local feedback in each of four stages to secure broad bandwidth and stable operation. Phase and gain trimming is accomplished in the interstage-transistor section by the adjustment of the input coupling network and by the adjustment of emitter-feedback resistance.

Output coupling of the AGC-rf amplifier to the broad band amplifier (BBA), the next functional module, is through a filter

network designed to attenuate the signal spectrum associated with gain programming, dc-to-3 MHz.

Broad-Band Amplifier

The broad-band amplifier modules shown in Fig. 2 provide 43 dB of fixed rf gain in each signal path. These amplifiers (AVANTEK type 621-B) have a 1 dB bandwidth greater than 100 MHz. The units are used where the slope of the frequency response is small, in the 30-to-54 MHz range. Amplifier pairs have typical gain and phase matching properties of 0.5 dB and 0.5 deg, respectively in the range used. A hi-pass filter, with a cut-off frequency of 22 MHz, is added to the amplifier circuitry at a point ahead of the input stage. A stripline section is specifically provided for this purpose by the manufacturer. Each broad-band amplifier drives a 50-ohm, 3 dB, rf power splitter, which is used to inject signals to the AGC detector and into the fine-gain corrector (FGC).

AGC Voltage-Control Circuits

The desired objective of the AGC circuits is to remove the rf amplitude variations of the signal applied to the phase demodulator so that these variations cannot be interpreted as phase changes by the phase demodulator. Each signal channel in the phase detector is gain controlled by feedback and feedforward voltages.

The rationale for an automatic gain correction rather than hard limiting as a means to remove amplitude modulation is that:

1. Less phase error is obtained for the same dynamic range

through the range of the signals encountered.

2. The errors caused by distortion in the rf signal (zero crossover, dead space, and nonsymmetry of the + and - portion of the signal) are much less severe with an AGC system.
3. The demodulator sensitivity (volts out per unit angle in) is not dependent on the limiter suppression factor which would cause the rf signals to be modulated should noise or spurious signal components enter through a limiter path.

The AGC voltage is developed by peak rectification of the rf signal (AGC DET block, Fig. 2). The rectifier signal is amplified, level set, and then fed back to the Nuvistor control grids. The peak rectifier circuit contains a split secondary, ferrite-core, rf transformer feeding a matched set of PIN diodes in full-wave fashion. The PIN DIODES (HP 2912)* are loaded with an rf filter network and are poled to produce a positive output. A dc bias current is introduced into the transformer center-tap to forward-bias each PIN diode so that a specific AGC operating point is achieved. Sufficient bias current is introduced under closed loop AGC conditions to make the rf voltage appearing at the FGC input port 0.2-V P-P when the rf input to the AGC rf amplifier (see Fig. 2) is 0.2-V P-P. Post-rectifier gain is provided by an inverting operational amplifier having a gain of 53 dB. A feedback-compensation network associated with the operational amplifier provides a 20-dB/decade gain roll-off beginning at 40 kc. The network aids in stabilizing the AGC feedback loop. The closed-loop gain of the AGC

*HP type 2306 may also be used.

system is 29 dB which gives the regulation characteristic (rf output vs rf input) about a 20% droop as the input rf signal is lowered to the lower boundary of the range of interest (see Fig. 3). To further increase the effective loop gain and make the regulation characteristic flatter, the rf signal is transmitted through an additional Nuvistor (FGC) gain controlled stage supplied with a control voltage derived and fed forward from the AGC control line.

The FGC-stage control bias is introduced through a silicon diode (HP 1002) which imparts "delayed action" control characteristic to the overall gain-control system (Fig. 3). The gain of the FGC amplifier is 0 dB and the total control range is 2 dB. No corrections for phase error with gain programming is necessary in this stage due to the small dynamic operating range and because cut-off conditions are not approached. The overall speed of response of the AGC/FGC system is 6 dB/μsec minimum.

Phase Demodulator

The phase-demodulator circuit consists of a quadrature hybrid 4-port (Merrimac type QH 4-53), a balanced difference rectifier, and an error-signal amplifier. The quadrature hybrid is a passive, reactive, lumped-element component which is used to convert phase differences at the input ports to amplitude differences at the output ports. The quadrature hybrid rf input signals, $E_1 = E_2 = E_{in}$, are equal in amplitude; they have the same frequency, but may assume any phase relationship

within bounds of ±90 deg. The two output signals, E_{01} and E_{02}, are related to the rf input signals and the phase difference angle ϕ by:

$$E_{01} = E_{in} \sqrt{1 + \sin \phi}$$

and

$$E_{02} = E_{in} \sqrt{1 - \sin \phi}.$$

The internal losses in the junction are assumed negligible. The E_{in} component in the above expressions is kept constant by AGC action, making ϕ the important variable. The output rf signals, E_{01} and E_{02}, are applied to a matched pair of PIN diodes, connected so as to produce an output voltage proportional to the difference in peak-rectified voltage. The rectifier load circuit is arranged to permit the rectifier having the smaller input to be proportionately forward biased. With this connection and for rf inputs of about 1-V P-P, the diodes operate in a region which is essentially "square law." The dc voltage for each diode is then:

$$E_{dc1} = \left[K_1 E_{in} \sqrt{1 + \sin \phi}\right]^2$$

and

$$E_{dc2} = \left[K_2 E_{in} \sqrt{1 - \sin \phi}\right]$$

where K_1, K_2 are constants related to the rectification efficiency and the load network values; $K_1 = K_2$ for matched diodes and networks. The difference between the rectified voltages, $(E_{dc1} - E_{dc2})$ represents the detector output (E_{det}); thus for $K_1 = K_2$

$$E_{det} = 2KE_{in}^{2} \sin \phi \text{ Volts.}$$

The E_{det} voltage is amplified with an operational amplifier having a gain,

$$G(s) = \frac{20}{1+0.12x10^{-6}s}$$

and applied to BNC connectors labeled DIRECT OUTPUT. These connectors are on the front and rear panels of the phase detector unit. The DIRECT-OUTPUT port voltage, taking into account the constant K, and the detector output network is:

$$E_{\text{DIRECT OUTPUT PORTS}} = \frac{2 \sin \phi}{1+0.12x10^{-6}s} \text{ Volts.}$$

Subsequent amplification in the signal-gate module produces an output voltage at the E_{out} ports as shown in Fig. 4. Note in Fig. 4 that the voltage is not exactly a sine function owing to some internal losses in the hybrid and some departure from "square" diode characteristics in actual components.

Signal Gate Module

The signal gate module of the phase detector permits the $E_{\text{DIRECT OUTPUT}}$ voltage to be further amplified and multiplexed with an externally applied offset voltage, called EXT OFFSET. The control of the multiplexing action is due to TTL logic circuits activated by triggers called TRIG I and TRIG II. These two trigger signals are transmitted in a daisy-chain fashion in the booster and main accelerator and are terminated by 51-ohm resistors located in the signal gate module.

The triggers are received by the HEX inverter (SN7404N). These are several outputs from the HEX inverter. One output

controls the start and stop action of FLIP-FLOP (SN7400N) from which bipolar switching control gates are generated. A second HEX inverter output also supplies front and rear panel buffered triggers corresponding to the TRIG I and TRIG II pulses. The buffered triggers are called TRIG I' and TRIG II'. These triggers are useful as test drivers and in diagnostic applications. Loading rules apply for TTL logic at these ports. Lastly, the HEX inverter supplies a start pulse corresponding to TRIG I time, to ONE SHOT (SN4121N), which is used to control FLIP-FLOP "1" to "0" turn off. The FLIP-FLOP turn off operates in the event that TRIG II is not used, or for special timing conditions requiring a specific time sequence of the multiplexing module.

The bipolar-control gates, obtained by amplification and level shifting of the FLIP-FLOP outputs, are applied to a quad-bilaterial complementary symmetric switch (RCA-4016) through which the DIRECT-OUTPUT and OFFSET signals flow. The switching action of this device together with additional amplification and filtering segments of the output signal (called E_{out}), as follows:

SEGMENTING THE OUTPUT SIGNAL, E_{out}

Time Interval	Signal at E_{out} Ports
Time between TRIG I and TRIG II.	E_{out} = 10 sin ϕ Volts; frequency response depends on plug-in filter, maximum -3 dB bandwidth is 1.1 MHz.
Time between TRIG II and next TRIG I.	E_{out} = Externally applied signal, unity gain path, maximum -3 dB bandwidth is 1 MHz.

Time Interval	Signal at E_{out} Ports
Time between TRIG I and one shot off pulse. Adjustable with time pot and booster/main accelerator switch.	E_{out} = 10 sin ϕ Volts; frequency response depends on plug-in filter, maximum -3 dB bandwidth is 1.1 MHz.
Time between one shot off next TRIG I.	E_{out} = externally applied signal, unity gain path, maximum -3 dB bandwidth is 1 MHz.

The isolation between multiplexed signal paths is 36 dB minimum for signal frequencies to 1 MHz, and switching transients are typically less than 0.15 V peak and less than 1 μsec in duration.

The E_{out} phase error voltage appears at BNC connectors on the front and rear panels of the phase detector unit. The rear and front panel ports are designed for loads not less than 2 kΩ at the end of 20 ft of RG-58 or equivalent cable.

Loop Filter

A removable rf filter is included in the phase detector to aid in stabilizing the local rf station cavity tuning loop. The filter is normally connected in series with the detector's output voltage line by jumping the E_{out} port to the filter IN port. The programmable bias supply cable is normally attached to the filter OUT port. The transfer function for the filter is:

$$\frac{V_{out}}{V_{in}}(s) = \frac{(2.27\times10^{-7}s+1)\ (4.55\times10^{-4}s+1)}{(2.26\times10^{-2}s+1)\ (0.78\times10^{-5}s+1)}$$

This notch-like lead lag function may be altered as required for optimum stability of the feedback loop.

Power-Supply Group

Regulated voltages are used to supply dc power to all circuits of the phase detector, including the heaters of all Nuvistor tubes. Primary ac power is obtained through the rf line filters and a line-isolation transformer having primary/secondary electrostatic shielding. This transformer reduces the noise which would, otherwise, be transferred to internal power lines by capacitive coupling.

Meter Module

Nine circuit points are monitored by a microammeter attached through the isolation resistors. The meter functions are switch selected and provide a local observation of:

1. AGC detector bias.
2. AGC control voltage, 2 channels.
3. AGC offset voltage, 2 channels.
4. OP1, OP2, an error voltage operational amplifier zero balances.
5. FGC control voltage, 2 channels.

The meter indications and circuit adjustments pertaining to the phase detector are discussed in the adjustment procedures that follow.

OPERATIONAL CHECK PROCEDURES

Thirty-two phase detector units have been installed in the booster and main accelerator RMU cabinets during July-August, 1971, time frame. Each unit has accumulated in excess of 5,000* operational hours. During this interval eight instances of component trouble and ten instances of adjustment related troubles have occurred. The component troubles, probably thermally induced, have been related to power supply regulator (±15, and 6.3 V modules) being out of tolerance or inoperative and to operational amplifier failures (Analog Devices 148C). The adjustment related troubles involve either the phase balance (operational amplifier, zero offset) or the output signal level (gain) adjustments, being above or below nominal.

A series of checks and adjustments is suggested to maintain best operation of the phase detector. Experience indicates a 4-month test and adjustment cycle with the unit remaining in the RMU is warranted.

The following ordered sequence of the check procedures are recommended:

Phase-Detector Checks and Adjustments (4 Months)

A. dc Power-Supply Voltage

1. With the phase detector connected for normal operation in the RMU position, the meter module selector switch should be positioned to OFF.

---

*This represents a substantial fraction of the Nuvistor lifetime, estimated to be 10,000 hours. The Nuvistors should be replaced at or near the 10,000-hour time.

2. Check to see if the mechanical zero on the meter corresponds to the 0 μA which is marked at center scale.

3. If an adjustment is needed, turn the mechanical zero screwdriver control on the meter case for the required zero indication.

4. Unscrew the front panel circular access cover to expose the voltage check points and the adjustment points.

5. Using Fig. 5 for terminal location, measure the following voltages with a DVM.

Voltage	Tolerance
+63	-100 +50 mV
+12	±50 mV
+15	±50 mV
-15	Magnitude tracks +15 within 300 mV
+65	±1 V

6. If required, adjust the appropriate voltage controls located on the power supply modules (Fig. 5) for the correct location. The top screen cover of the unit may be removed to make adjustments.

B. AGC Operating Point

1. Set the meter module selector switch to DET and check that the deflection is +15 ±3 μA.

2. If necessary, adjust the DET bias for the required value.

3. Check that offsets OFF A, OFF B, show at least 1 major division +(10 μA) on the meter scale.

C. Operational Amplifier Zero

1. Disconnect the blue TEXSCAN FP-50, 6 dB pads, from the RF-1 and RF-2 (circular) attenuators on the rear panel.

CAUTION: Do not mix up these cables as these are the rf inputs which eventually will establish the output error signal polarity; identify each cable so that they can be mated at a later time with exactly the same input port.

2. Position the meter module selector to OP-1 and note the meter deflection is 0 $\pm\frac{1}{2}$ μA.

3. If required, adjust the OP AMP ZERO trimpot (the identification of the trimpots is per front panel marking) for the zero deflection.

D. Sensitivity, Direct Output

1. Set up a sweep generator, oscilloscope, and a rf power splitter as shown in Fig. 6a, 90° cable included in RF-1 line. The 90° cable for this test is 30 in. of RG-174 cable terminated with BNC fittings.

   a. Synchronize the display by adjustment of the scopes LEVEL and STABILITY controls and adjust the SWEEP-TIME controls of the scope and sweeper for a "flicker-free" scope trace.

   b. For the booster detectors set the swept frequency limits to 29 and 54 MHz, for the main accelerator area set the limits to 50 and 55 MHz.

2. Ground the oscilloscope vertical input to establish a "zero" reference on a scale which will permit observation of a 2-V peak signal; remove the ground.

3. Connect the DIRECT OUTPUT port to the scope vertical input via 3-to-10 feet, RG-58, or equivalent coaxial cable. Note: Scope input impedance not lower than 2 kΩ.

4. Observe that the negative going "raised ramp" signal is 2 V in peak amplitude at the 54 MHz frequency.

5. If necessary, adjust E_{out} gain for the -2 V deflection at the 54 MHz frequency; see Fig. 5 for control location.

6. Reverse the position of the 90° cable, i.e., put the 90° in the RF-2 line and observe that the raised ramp" is positive going and has an amplitude of 2 ±.25 at the 54 MHz point. If the signal does not meet this requirement, or is otherwise basically different in shape, or offset from the reference, unit servicing is required.

E. Phase Signature

1. Set up the sweep generator, oscilloscope, and the rf power splitter as in Fig. 6b, no added phase cables in the RF-1 or RF-2 input lines. Be sure to set the frequency limits of the sweeper for booster or main accelerator to the limits as in the above test.

2. Connect the DIRECT OUTPUT port of the phase detector to the oscilloscope as for the SENSITIVITY test above.

3. Establish a "zero" reference on the scope face and set the VERT sensitivity for observation of signals of 0.2 V peak amplitude.

4. Observe that the signature trace, throughout the 30-to-54 MHz (booster) or 50-55 MHz (main accelerator) range, does not exceed boundary voltage of ±0.15 V about zero.

5. If the conditions of 4 are not observed, take the following action:

   a. For out-of-boundary conditions up to 0.1 V, i.e., for boundary conditions of ±0.25 V about zero, carefully adjust one of the ϕ ADJ trimmers located behind the front panel ALLEN bolt. Use only a screwdriver blade plastic alignment tool. Only a slight, ±10°, adjustment should be required.

b. For out-of-boundary conditions exceeding the limits by more than 0.1 V first check to see that the OP-1 zero is correct and the connecting cables are phase matched. If these two checks indicate no trouble condition, the unit is out of spec. The manufacturers, SECTION 5, tests are required and the unit should receive remedial action.

F. Multiplexer and Final Zero

1. Using the oscilloscope in the RMU, select a sweep time setting of 10 ms/cm, and select the oscilloscope channel which is used to observe the phase error signal (the signal which is transmitted to the bias power supply).

2. Add a small length of cable (1 foot) in series with the RF-1 cable which connects to the power splitter and set the sweeper to 50 MHz, cw, 10 mW.

3. Observe that the phase error signal is positive and exists between the time corresponding to the TRIG I and TRIG II time.

4. Remove the ac power cord of the sweeper from the 120 V outlet.

5. Using the RMU scope, establish a zero reference with the vertical input grounded. Establish this level within 10 mV. Remove the ground.

6. Readjust OP AMP ZERO for a zero reference value between the interval defined by the TRIG I and TRIG II timing pulses, within 10 mV.

7. Remove all sweeper, splitter, and ancillary scope connections and reconnect the rf stations, rf cables. Replace the phase detector circular front panel adjustment cover, and reset the RMU oscilloscope settings for

normal use. This completes the phase detector operational check and adjustment sequence.

For a more general manufacturer's check and adjustment sequence see "DITTMORE-FREIMUTH CORPORATION, Phase Detector Test Procedure."

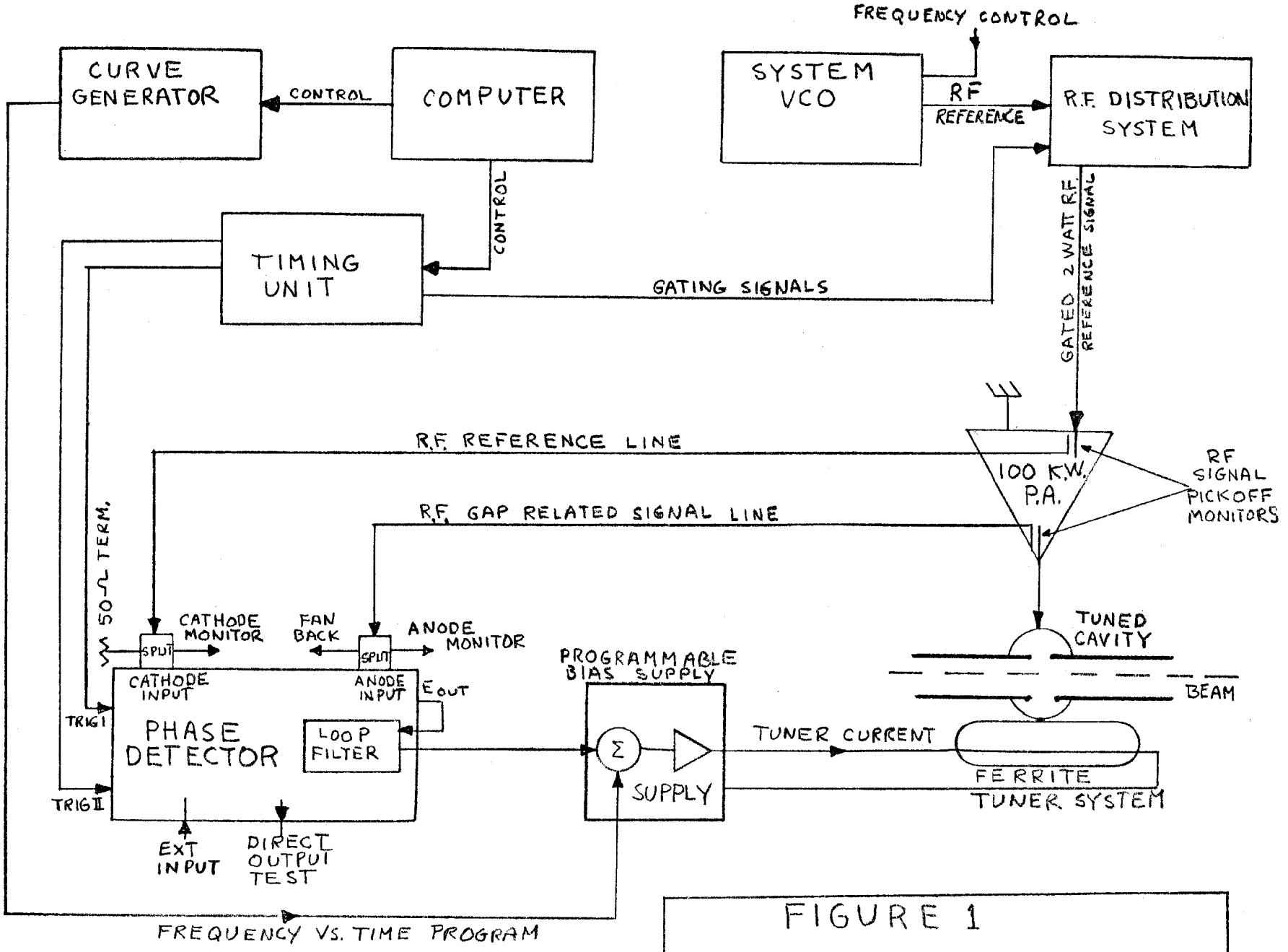


FIGURE 1

PHASE DETECTOR IN RF STATION FEEDBACK LOOP

TM-354
0431

EJH 11/12/71

NATIONAL ACCELERATOR LABORATORY
ENGINEERING NOTE

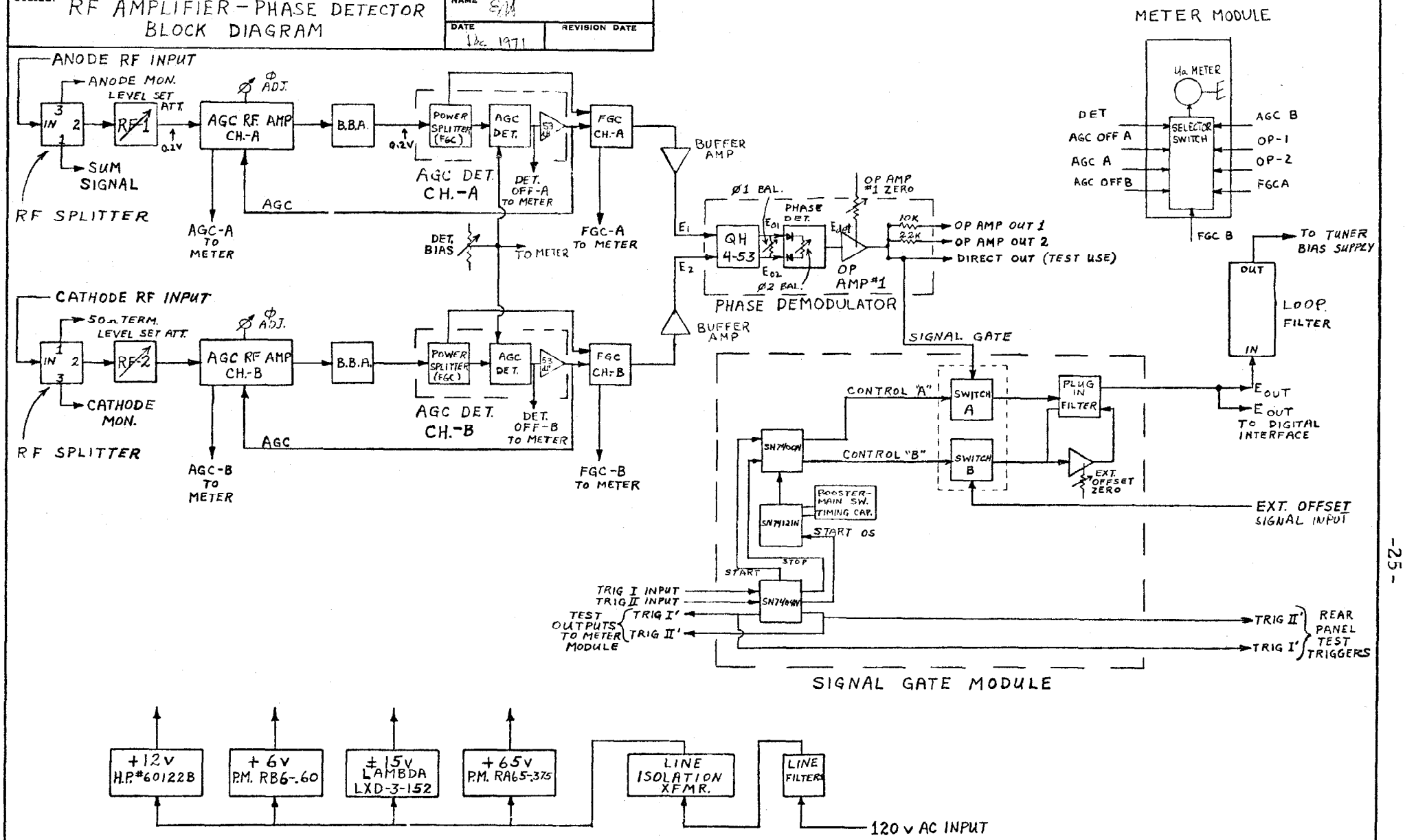
SECTION	PROJECT	SERIAL CATEGORY	PAGE
FIG-2			

SUBJECT: RF AMPLIFIER - PHASE DETECTOR BLOCK DIAGRAM

NAME: GM

DATE: Dec 1971

REVISION DATE:



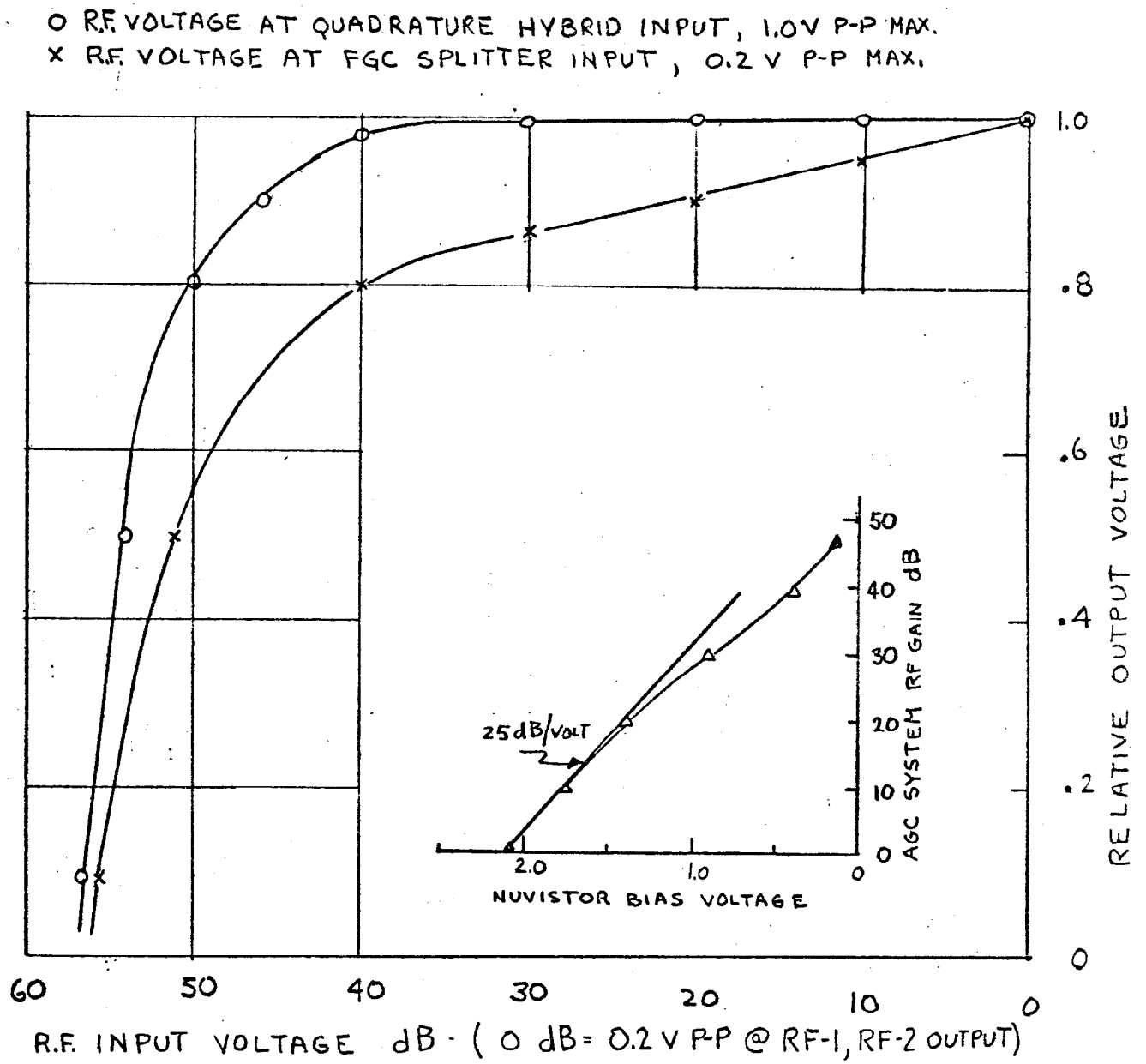


FIGURE -3 AGC REGULATION CHARACTERISTICS AND GAIN VS. BIAS RELATIONSHIP

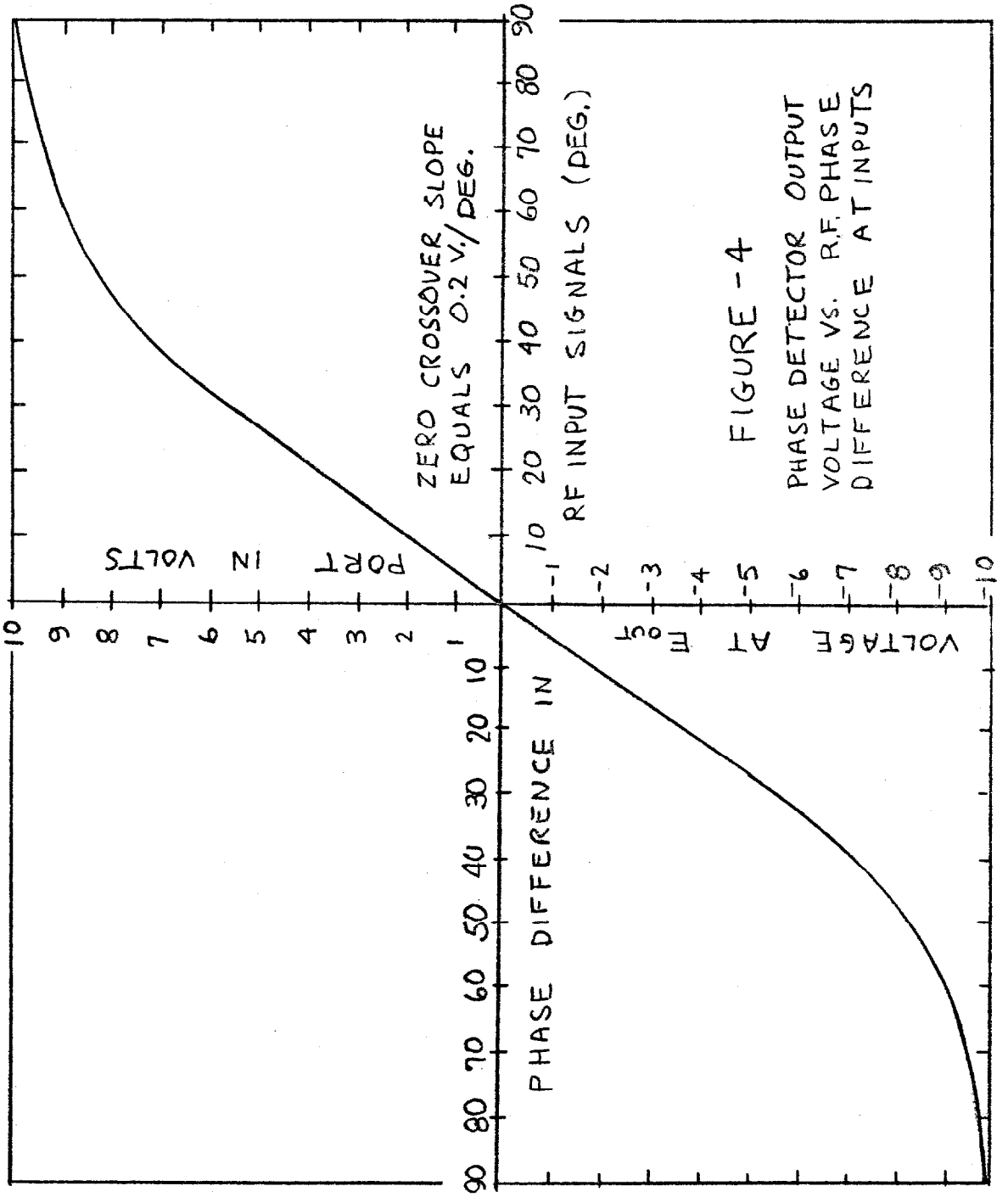
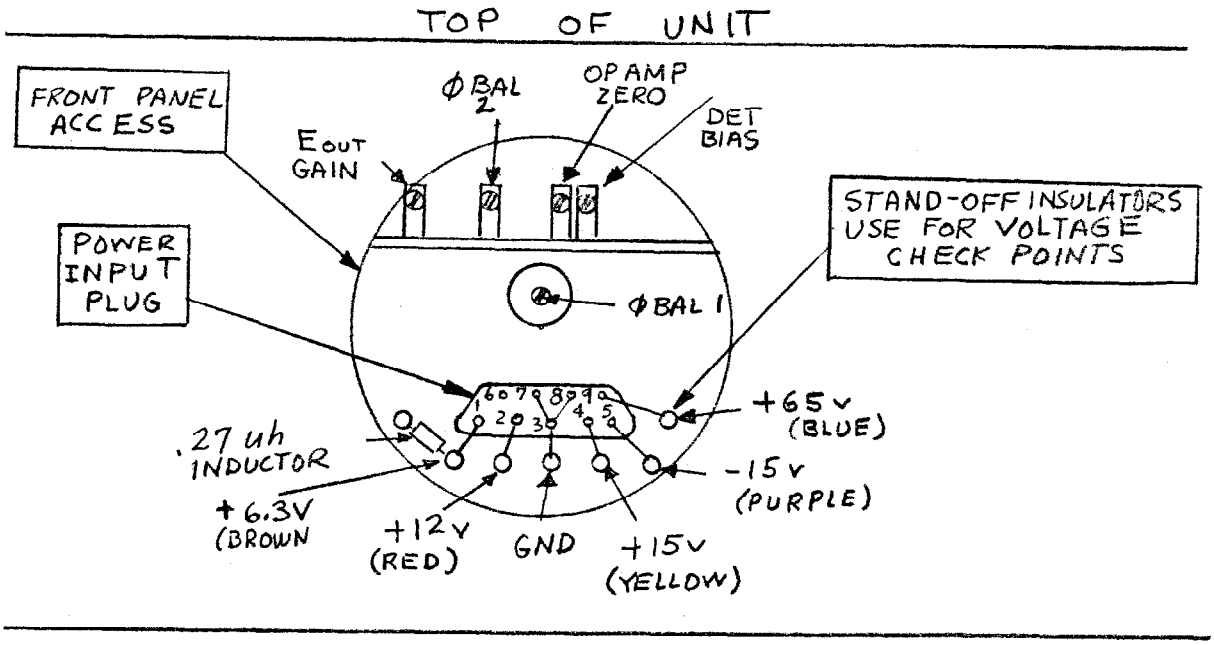


FIGURE - 4

PHASE DETECTOR OUTPUT VOLTAGE VS. R.F. PHASE DIFFERENCE AT INPUTS



LOCATION OF VOLTAGE TEST POINTS AND PHASE DETECTOR ADJUSTMENTS

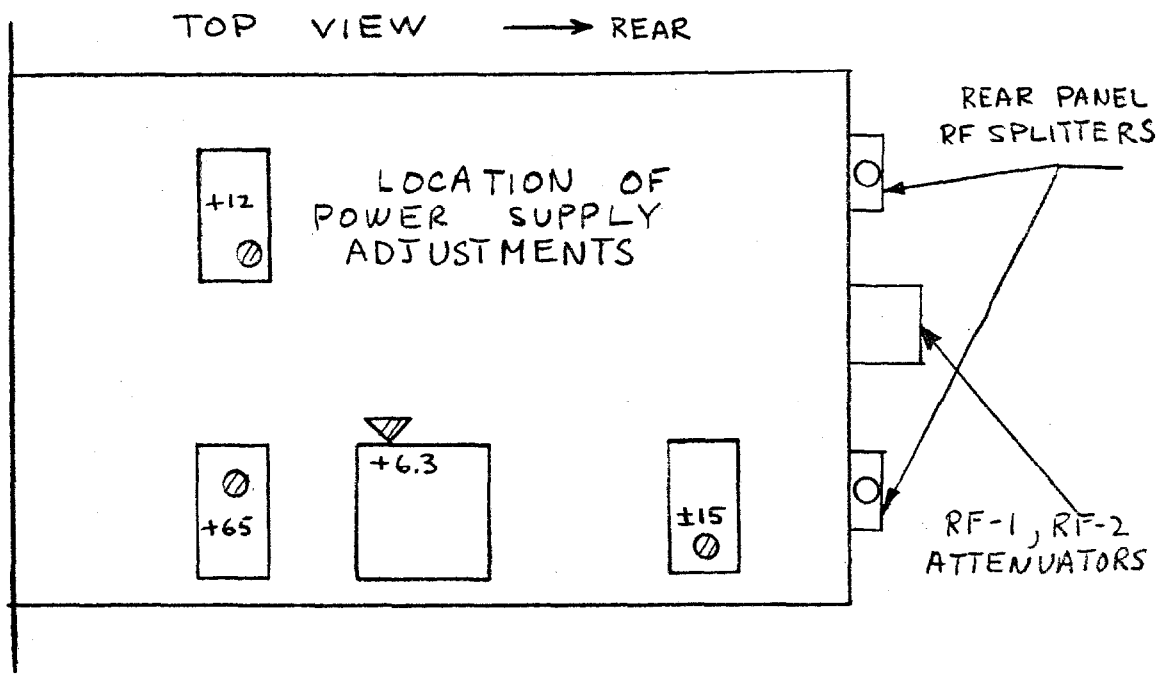


FIGURE-5 - PHASE DETECTOR ADJUSTMENT AND TEST POINT LOCATIONS

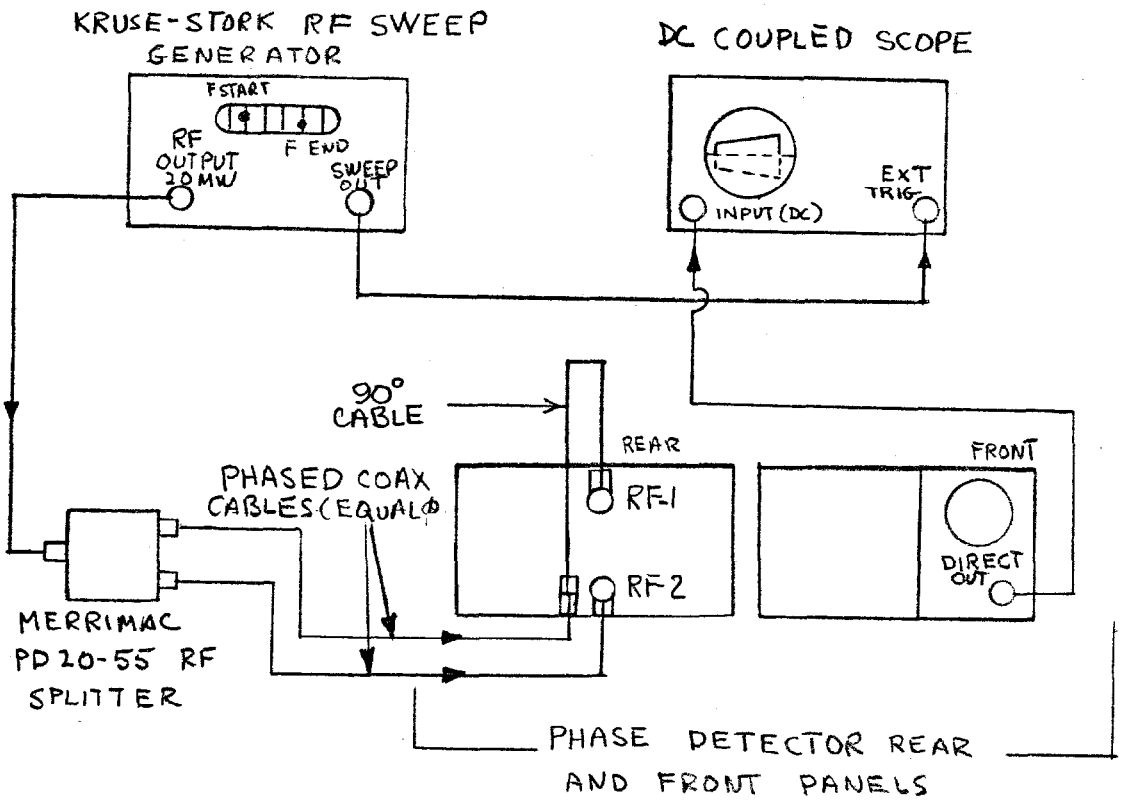


FIGURE-6-a TEST SETUP FOR SENSITIVITY AND GAIN ADJUSTMENTS

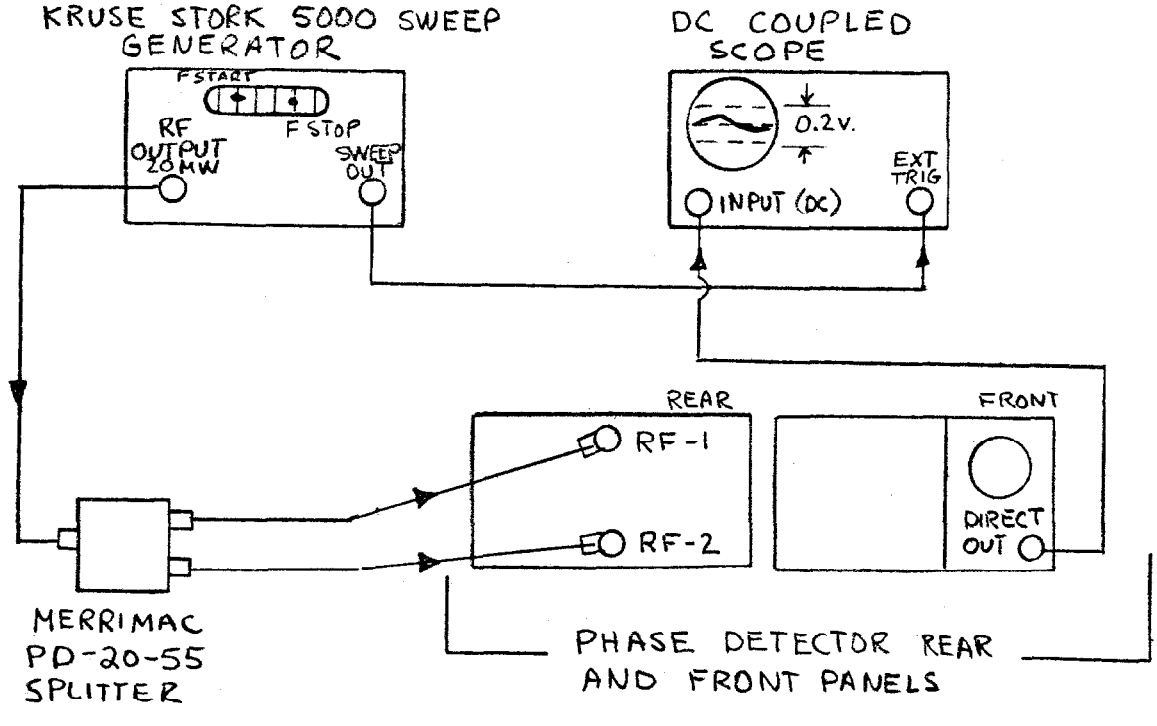


FIGURE 6-b TEST SETUP FOR PHASE DETECTOR OUTPUT VOLTAGE VS FREQUENCY FOR NO INPUT PHASE DIFFERENCE (SIGNATURE)

NATIONAL ACCELERATOR LABORATORY
ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
FIG-2			

SUBJECT: RF AMPLIFIER - PHASE DETECTOR BLOCK DIAGRAM

NAME: EOA

DATE: Dec 1971

REVISION DATE: