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ULTRAFAST HIGH-VOLTAGE KICKER SYSTEM HARDWARE FOR ION CLEARING GAPS*

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Abstract

Ionization scattering of electron beams with residual gas molecules causes ion trapping in electron rings, both in a collider and electron cooling system. These trapped ions may cause emittance growth, tune shift, halo formation, and coherent coupled bunch instabilities. To clear the ions and prevent them from accumulating turn after turn, the gaps in a temporal structure of the beam are used. Typically, the gap in the bunch train has a length of a few percent of the ring circumference. In those regions, the extraction electrodes with high pulsed voltages are introduced. In this paper, we present the design consideration and initial test results of the high-voltage pulsed kicker hardware that includes vacuum device and pulsed voltage driver, capable of achieving over 3 kV of deflecting voltage amplitude, rise and fall times of less than 10 ns, 100 ns flat-top duration at 1.4 MHz repetition rate.

INTRODUCTION

A polarized electron-ion collider (EIC) is a planned tool for gluon microscopy to explore the frontiers of quantum chromo-dynamics [1]. The EIC lepton-hadron collider concept is targeting ultra-high luminosities of 10^{34} cm^{-2} s^{-1}, approaching those in lepton-lepton colliders [2]. In order to deliver such high luminosities, a scheme to use multi-stage electron cooling of the ion beam has been developed by the Thomas Jefferson National Accelerator Facility (JLAB) [3]. In this approach the ion beam is first electron-cooled at low energy to reduce the emittance, and then is accelerated to the collision energy where electron cooling is again continuously reapplied to maintain luminosity during collisions, by suppressing emittance degradation due to non-linear collective effects plus intra-beam and residual gas scattering processes.

However, ionization scattering of the electron beam with residual gas molecules causes ion trapping in the electron rings, both in the collider and electron-cooling system [4]. These trapped ions may cause emittance growth, tune shift, halo formation, and coherent coupled bunch instabilities. Therefore, the beam's temporal structure needs clearing gaps for timely removal of the residual ions to prevent them from accumulating over many turns. Typically, the gap in the bunch train has a length of a few percent of the net ring circumference, so the clearing voltage must be applied within that interval.

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In response to this need, RadiaBeam, in collaboration with JLAB scientists, is developing an ultra-fast high-voltage kicker. The system is designed to kick out 4 of 31 bunches, while keeping the rest in the bunch train, at 43.4 MHz base bunch rep rate to leave a gap of ~92–100 ns, see Figure 1. Both the rise and fall time of the deflecting pulses must be less than 20 ns (<10 ns desirable for rise time), with a sub-ns or better timing jitter. The clearing system does not perturb the quality of the beam pulses injected into the linac; it also avoids creating a substantial halo, which must remain <10^{-5} of the beam current.

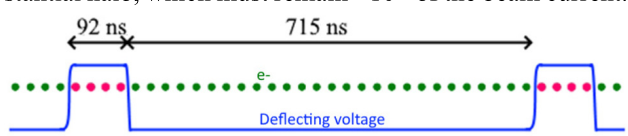

Figure 1: Kicker operation temporal diagram.

This design satisfies the requirements, summarized in Table 1.

Table 1: Kicker System Specifications

Parameter	Value
Deflecting angle	20 mrad
Length	50-60 cm
Electron Beam Energy	7 MeV
Bunch Repetition Rate	43.4 MHz
Bunch rms Transverse Size	σ = 1 mm
Deflecting Pulse Width	100 ns
Pulse Repetition Rate	1.4 MHz
Rise+Fall Time	<20 ns

KICKER DESIGN

The kicker is formed with two parallel electrodes inside a vacuum chamber (Ø47.5 mm pipe matching existing JLAB beamline), see Figure 2. It equipped with four coaxial ports, two of which serve as pulsed power inputs and two are terminated with 50 Ω water-cooled loads.

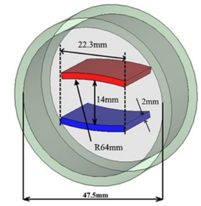

Figure 2: Transverse profile of the stripline kicker electrodes.

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The design process was carried out centrally focused around two main aspects: EM behavior (pulse propagation and minimum power consumption) and beam dynamics (minimum loss of kicked and unkicked beam).

As a 4-port RF device, the kicker must be able to provide matching across a bandwidth of at least 0-300 MHz to ensure no distortion in the form of the 10 ns rise and fall edges. By adjusting the electrodes widths and their curvature radius, we have optimized their shapes to both show 100 Ω characteristic impedance at the odd mode and uniform field around the axis within ±6σ radius (σ=1 mm).

To find an optimal choice for the kicker cavity length, we considered a series of lengths to check on the beam loss over a range of injection beam parameters. Then the length was determined for the case with the lowest corresponding pulsed power. The plot in Figure 3 shows the peak and average power consumption dependence on the kicker length (L_{eff}), with the given electrode profile and load impedance of 50 Ω.

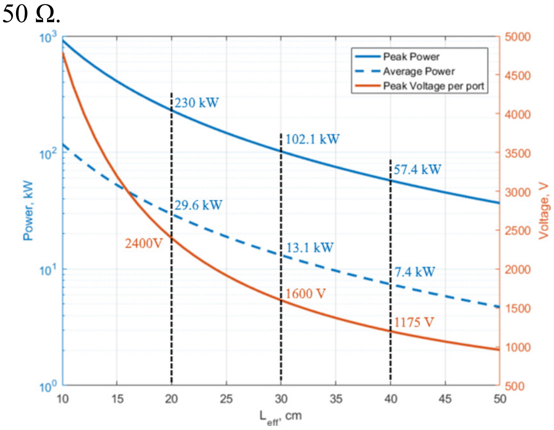

Figure 3: Required voltage and power consumption for 20 mrad deflection in the kicker with 14 mm gap.

Since simulating a range of injection parameters directly would have been very time consuming, we instead calculated an analytical description of the beam trajectories and then bench-marked the simulation results by the CST Particle Studio particle-in-cell (PIC) solver for only a few cases. In particular, the y-offset at the exit of the stripline kicker Y is given as:

$$Y = y_0 + \frac{v_0}{c} L_{eff} + \frac{2eV_p}{gm\gamma c^2} L_{eff}^2. \quad (1)$$

The distance between the edge of the gap and the center of beam, (g/2-Y) defines to beam loss R in Gaussian transverse profile of the beam (only on one side) as follows:

$$R = 1 - \frac{1}{\sqrt{2\pi\sigma^2}} \int_{-\infty}^{\frac{g}{2}-Y} e^{-\frac{y^2}{2\sigma^2}} dy, \quad (2)$$

where σ is transverse rms size of the beam (1mm). This would lead to the beam loss power as:

$$P_{BL} = Q_b f_b \frac{W}{e} R. \quad (3)$$

Here f_b, Q_b, and W are bunch frequency, bunch charge, and electron energy, respectively. For the JLab EIC Q_b=1.6 nC and f_b=43.3 MHz, and W=7 MeV, yielding the required powers, provided in Table 2.

Table 2: Beam Loss With Various Stripline Lengths

Analytical evaluation	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
L_{eff}, mm	200	300	400	600	400	400	600	600
20 mrad kick	yes	yes	yes	yes	yes	no	yes	no
V_p, V	2275	1560	1175	790	1175	1175	790	790
Offset, mm	0	0	0	0	0	0	0	0
Tilt, mrad	0	0	0	0	-5	-5	-6	-6
Beam loss, %	10^{-6}	$9 \cdot 10^{-5}$	$3 \cdot 10^{-3}$	0.21	$5 \cdot 10^{-5}$	$5 \cdot 10^{-5}$	$5 \cdot 10^{-3}$	$5 \cdot 10^{-3}$
P_{BL}, W	0.04	2.4	104.5	8100	2.1	1.8	178	176
P_P, kW	14.5	6.8	3.85	1.75	3.85	3.85	1.75	1.75
CST simulations								
Beam loss, %	$7 \cdot 10^{-6}$	$4 \cdot 10^{-5}$	$1.6 \cdot 10^{-3}$	0.38	$4.7 \cdot 10^{-5}$	$4.7 \cdot 10^{-5}$	$3.6 \cdot 10^{-3}$	$3.6 \cdot 10^{-3}$
P_{BL}, W	0.27	1.55	62	14700	1.8	1.8	140	140

Columns 5 and 6 represent the kicker behaviour with optimal pulse power and beam loss. At this length (L_{eff}=40 cm), the required voltage is 1175 V (3.8 kW of average power per port). The mechanical model of the kicker cavity is shown in Figure 4.

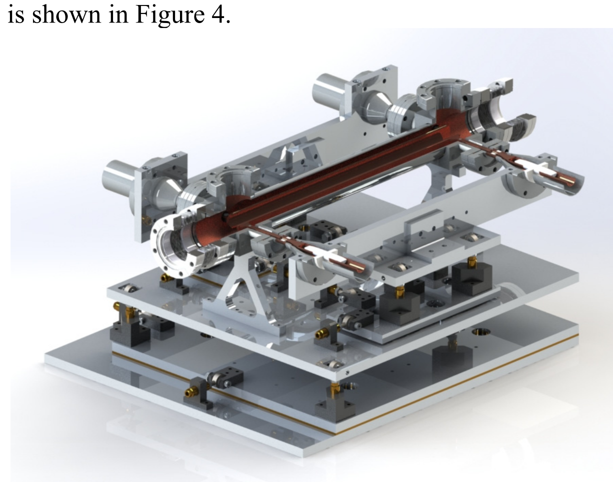

Figure 4: Mechanical design of the stripline traveling wave kicker as a beamline insertion device.

PULSER DEVELOPMENT

After optimizing the kicker cavity dimensions and evaluating the corresponding pulsed power requirement, we began to design of the pulse generator (pulser). At first, two commercial off-the-shelf fast switches were tested at high power: FSWP-51-02 (MOSFET-based) and FSWP-51-06 (GaN-based) from Behlke Gmbh. The MOSFET version showed stable performance, acceptable <7ns rise and fall times, but only showed ~50% efficiency due to a internal resistor for impedance matching. GaN version demonstrated even shorter pulse edges, <5 ns, but was highly unstable and eventually failed when output voltage reached 800V. Eventually, we decided to develop the switch internally at RadiaBeam.

We decided to use GaN transistors as the main element of the switch. A test board was developed with a single transistor, see Figure 5. Its performance was studied under various gate drive voltages and series resistors for both turn-on and turn-off scenarios. It was experimentally determined that low gate resistor values for opening the transistor led to unstable operation during the pulse, necessitating a dual-resistor gate control scheme.

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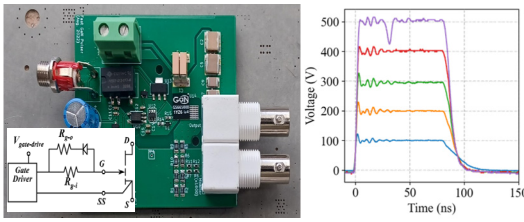

Figure 5: Single transistor test board (left) and measured output waveforms (right).

The first iteration of the pulser was based on three transistors in series (3S1P configuration), shown in Figure 6. The modifications to the driver circuit are introduced to increase the transistor turn-off speed by applying negative voltage to the gate. The EZDrive gate control scheme was implemented, which, with a unipolar power supply for the driver, provided a negative voltage drop to turn off the transistor.

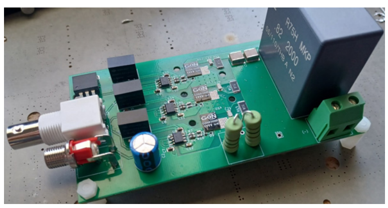

Figure 6: Pulser version 1 developed by RadiaBeam, 3S configuration.

This setup ensured stable transistor operation during testing with an input voltage up to 1200 V, see Figure 7.

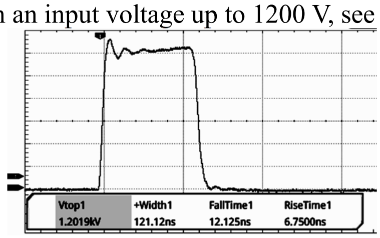

Figure 7: Measured output waveform (version 1).

The pulse rise and fall times were measured at 7/12 ns. However, the pulse top remained unstable, with increasing amplitude oscillations and a voltage spike at the front. A high repetition rate pulse test could not be conducted due to the limited power of the high-voltage power supply, and only the burst pulse mode was tested. The next iteration (version 2) included the water-cooling plate to increase power handling capabilities. During the tests, the PRF was increased until the temperature of the transistor remained below 90°C. Version 2 achieved stable operation with 800 V amplitude, 400 kHz PRF, 100 ns FWHM (500W average), see Figure 8.

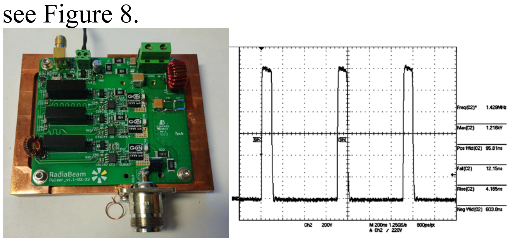

Figure 8: Pulser version 2 (left) and measured output waveforms in burst mode with 1.4 MHz PRF (right).

Consequently, the next version 3 with 4S2P configuration (4 in series and 2 in parallel) was developed. With that configuration we decreased the thermal load by 4 times. Thermal contact was improved by using a 0.635 mm thick AlN ceramic substrate between the transistor and the cooling plate. With this version, we were able to achieve stable operation with 1000 V amplitude, 1.4 MHz PRF, 100 ns FWHM (2700W average), with rise and fall times of 6 ns and 11 ns.

The final pulser iteration (version 4) contained 5S2P configuration, demonstrating 4.7 ns rise, 11 ns fall time with 1200 V, 1.4 MHz repetition rate at 100 ns FWHM, see Figure 9.

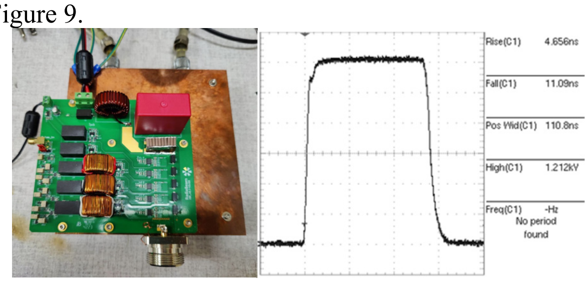

Figure 9: Pulser version 4 (left) and measured output waveforms (right).

The maximum peak voltage achieved 1600 V at PRF of 400 kHz.

CONCLUSIONS

An ion clearing gap for electron cooling system is required to operate the next generation of ultra-high luminosity nuclear physics colliders such as the EIC lepton-hadron collider. In this paper, we presented a HV kicker design, capable of achieving 20 mrad deflecting angle of 7 MeV electron bunch. Based on the optimization of several kicker parameters, we found that its effective length should be 40-50 cm, and the required peak voltage is 1200 V. We developed a GaN-based switch that demonstrated 100 ns-long pulses at 1.4 MHz rep rate with <10 ns rise/fall times.

In addition to being an enabling technology for EIC, the proposed system or its constituent blocks may find various uses in HV switching applications, including fast beam choppers for injector test facilities, the next generation free electron laser light sources, and Inverse Compton Scattering gamma ray sources using ERLs.

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