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# The NECTAr project: a New Electronics design for Cherenkov Telescope Arrays

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**Abstract:** The future international very high energy gamma ray observatory, the Cherenkov telescope Array (CTA), will consist in an array of 50-100 dishes of various sizes. Each telescope will have a camera with photo-detectors installed in its focal plane and the associated front-end electronics. The total number of electronic channels will be larger than 100000. A possible way of optimizing the overall cost and energy consumption is to use an analogue memory based readout design. A similar design was used for the HESS (ARS0 chip) and HESS2 (SAM chip) telescope arrays. The NECTAr project aims at building and testing a full read-out module based on a new NECTAr ASIC. It integrates the functionalities of a up-to 3.2GSample/s analogue memory together with a 12-bit, 20MS/s ADC. A prototype chip, NECTAr0 and a full read-out module have been built and tested. The measured performances of the NECTAr0 chip and the full NECTAr read-out module will be presented.

**Keywords:** Very high energy gamma ray astronomy - Cherenkov telescopes - front-end electronics

## 1 Introduction

Imaging Cherenkov Telecopes detect and record short pulses (5-20 ns) of optical light produced by fast particles from cosmic ray showers in the atmosphere. The flashes of light are detected by cameras located in the focal planes of the telescopes and equipped with hundreds to thousands of pixels. Each pixel is a fast photodetector such as a photomultiplier (PMT). The background light ("Night Sky Background" or NSB) gives a firing rate per pixel of 100-300 MHz [1]. The trigger of Imaging Cherenkov Telescopes is a multi-step process, involving first a camera-level trigger, then a global telescope array trigger. The first levels of trigger occur when several photoelectrons are detected in adjacent pixels during a narrow ($\sim$ 5 ns) time window. Two options for event read-out have been tried in previous generations of Cherenkov telescopes. One possibility is to use Flash ADCs with a sampling rate of at least 250 MHz and a dynamic range of at least 8 bits. The drawback of this solution is the relatively large power consumption and cost. The other possibility is to use switched capacitor arrays ("analogue memories").

In the latter solution, the pulses from the PMTs are sampled and recorded in analogue memories, used as circular buffers, at rates of few GS/s and read back and digitized on demand with lower frequency when a trigger occurs. Analogue memories are used by the HESS IACT array [1] (ARS0 chip) and in the HESS2 (SAM chip [2]) and MAGIC II telescopes (DRS4 chip [3]).

The next generation of Cherenkov telescope arrays, the CTA (for ""Cherenkov Telescope Array") [4] will have tens of telescopes with more than 100000 read-out channels. The read-out system of CTA has to be as simple as possible to ease production and give high reliability with low maintenance requirements. The current systems used in the recent generation of Cherenkov telescopes (H.E.S.S., MAGIC and VERITAS) do not fulfil these requirements, as they were only designed for the order of 5000 channels and require constant maintenance.

The Nectar design (New Electronics for the Cherenkov Telescope Array) is a fully integrated, reliable low cost electronics for the CTA. Functionnalities such as the amplification of the PMT signals, storage in analogue memories and analogue to digital conversion (ADC) are integrated into a single low-cost ASIC, the NECTAr chip. One or several NECTAr chip (depending on the number of channels on the chip) ymounted on the front-end board. Several PMTs (a "cluster") are read-out by the same front-end board. An important feature of the NECTAr chip is the simplicity of the calibration of electronic channels. Each camera

1. The NSB rate quoted is the single pixel firing rate of the telescopes of the H.E.S.S array

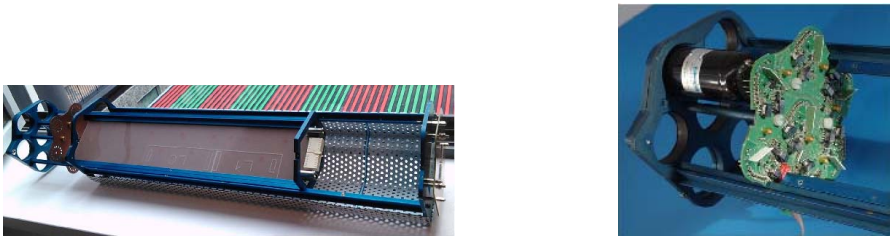

Figure 1: Camera module designed for the read-out of a cluster of 7 pixels. Left panel: the module consists in 3 parts (from left to right): a PMT high voltage control board, the front-end board, and a connector with an Ethernet interface. Right panel: The PMTs are plugged directly on the PMT high voltage control board.

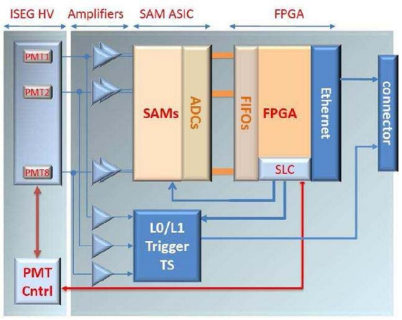


Figure 2: Data flow on the front-end board. See text for details.

thus consists of a number of independent, easily replaceable modules used to read-out clusters of pixels.

## 2 Camera module and front-end board

The camera module designed by the NECTAr consortium is shown on figure 1 (left panel). The PMTs are grouped in clusters of seven pixels and plugged to the PMT high voltage control board (on the left). These seven pixels are read out by a single front-end board. The interfaces to the front-end board are the PMT high voltage control board on one side and a 80-pin connector on the other side. The latter provides a connection to Ethernet. The high voltage of the photomultipliers is generated directly on the PMT high voltage control board (right panel).

The layout of the front-end board is shown on figure 2. The output signals of the PMTs is separated into a data path and a trigger path.

As mentionned above, the trigger of the Cherenkov telescopes is a multi-step process. The telescope trigger is obtained in 2 steps: first a cluster level trigger ( or "Level 0" trigger), then a camera level trigger ("Level 1 trigger") which looks for time coincidences of several cluster triggers. The Level 0 trigger and possibly the Level 1 trigger will be implemented on the front-end board. They are shown on the bottom part of figure 2.

The cosmic photon showers will produce single pixel signals ranging from one to 5000 photoelectrons. A read-out system with at least 12 bits is thus required to avoid saturation. In addition, the calibration of a single photoelectron signal implies a larger dynamic of $\sim$ 16 bits. The full dynamic range can be obtained either by sending the signal to 2 channels with different gains or by using a non-linear amplification in front of the analogue memories. After the amplification stage, the data are written into the analogue memory of the NECTAr chip. The NECTAr chip is described in more details in section 3. The write operations are stopped when a trigger signal is sent to the front-end board by the telescope trigger system. The analogue memory is then frozen until an array trigger starts the data acquisition. The data are then read out and sent to a FPGA.The FPGA performs some operations on the data, such as computing the total charge, then transfers the data to the acquisition farm through an Ethernet link. The same FPGA, shown on top right of figure 2 is also in charge of controlling and monitoring the front-end and PMT high voltage boards.

## 3 The NECTAr0 chip

The NECTAr0 chip is the first version of the final NECTAr chip. It performs the sampling, memorization and digitization of only two differential channels, whereas it will be 4 in the final one. As shown on the block diagram of figure 3, it integrates two analogue memories, similar to those of SAM, but with depths extended to 1024 cells to be compatible with a longer trigger latency. After a trigger signal, the cells corresponding to a small window of $\sim$ 16 ns around the trigger time are read-out and digitized by a 12-bit ADC operating at 20 MHz. The data are then serialized and sent to the on-board FPGA.

The expected performances of the NECTAr chip are listed on table 1. They are similar to the performances of the SAM chip. In particular, the dead-time penalty in the read-out and digitization process of 16 cells is expected to be $\sim 2\mu$s.The dead-time is roughly proportionnal to the number of read-out cells. As for HESS2, the read-out system should handle trigger rates up to 100 kHz. The total noise is

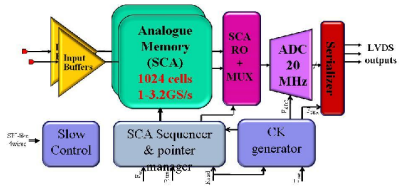


Figure 3: Block diagram of the NECTAr0 chip

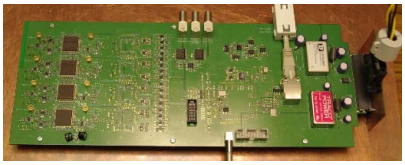

Figure 4: Test-board for the NECTAr0 chip. Four NECTAr0 chip are soldered on the top of the board (on the left) and four more are soldered under the board.

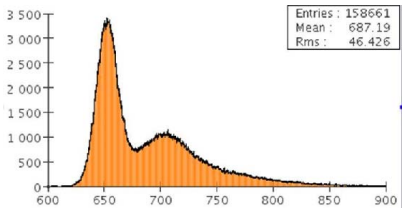


Figure 5: Single photo-electron distribution. The PMT is a XP2960 operated at a gain of $2 \times 10^5$.

expected to be 0.7 mV rms with a maximum input voltage of 2 V, giving a dynamic range of 11.5 bits.

## 4 Tests of the NECTAr0 chip and the read-out module

A prototype of read-out module is now under test. The NECTAr0 chip has also been tested with a special test board (see figure 4).

The test setup used a pulsed light source which was detected with a PMT. The signal was amplified and stored continously on the NECTAr0 chip. After an external trigger was sent to the test board, the data were transfered to the FPGA and then to a PC through an Ethernet connection. The Ethernet link has been operated succesfully with rates as high as 1 GBit/s. The intensity of the pulsating source could be attenuated by a filter so as to obtain the equivalent of a single photo-electron. The spectrum obtained is shown on figure 5.

Preliminary results on the chip linearity, analogue bandwidth, noise and cross-talk have been obtained. A noise value of less than 0.8 mV rms was measured. The dynamic range is thus over 11.3 bits. The analogue bandwidth was measured to be larger than 400 MHz.

| Specification | Value |
|---|---|
| Power consumption | $< 300$ mW |
| Sampling frequency range | 0.5-3 GHz |
| Analogue bandwith | $> 300$ MHz |
| Read-out time (16 cells) | 2 $\mu$s |
| Total noise (uncorrected for fixed pattern noise) | 0.7 mV rms |
| Maximum signal | 2 V |
| Dynamic range | 11.5 bits |
| Cross-talk | $< 3 \times 10^{-3}$ |
| Integral non-linearity | $< 10^{-2}$ |

Table 1: Main specifications of the Nectar chip

## 5 Conclusion

A camera module for the data acquisition of the next generation of Imaging Cherenkov Array, CTA, has been designed and is being tested. The module reads 7 photodetectors with the same front-end board. The front-end board incorporates a new ASIC, NECTAr, which has both functionnalities of analogue memory and analogue to digital conversion. Preliminary measurements on the NECTAr0 prototype show that it has an analogue bandwith of more than 400 MHz, a dead time of $2\mu s$, a dynamic range of more than 11.3 bits, close to the expected performances. A single photo-electron spectrum has been obtained.

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