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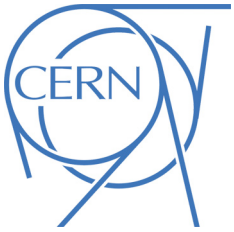

Design and assembly of double-sided silicon strip module prototypes for the ATLAS upgrade strip tracker

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Abstract

The LHC foresees a peak luminosity increase of up to $\sim 5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ from ~2022 with an integrated luminosity of $\sim 3000\,\mathrm{fb}^{-1}$ before 2030. The current ATLAS Inner Detector will not stand the predicted radiation levels nor the expected large increase in the hit occupancy rates. A new inner tracker must therefore be designed, built and installed in a relatively short time-scale. The current layout assumes an all-silicon tracker with pixel detectors for the innermost layers and strip modules at higher radii. Major constraints are the requirements of radiation-hard sensors, efficient power distribution, minimum material budget, affordable cost, and fast and reliable production.

This note reports on the design of double-sided silicon strip modules for the short-strip region of the upgraded ATLAS inner tracker. The different components of the module are described. The thermal performance is discussed. The assembly sequence of first module prototypes is explained in detail.

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Contents

1 Introduction

The ATLAS detector [1] is a general-purpose experiment designed to fully exploit the physics programme offered by the Large Hadron Collider (LHC) accelerator at CERN. The Inner Detector (ID) is the ATLAS inner charged particle tracking detector, providing precise vertex and momentum measurements and particle identification (electron/pion separation) up to $|\eta| \leq 2.5$. The ID is composed of the Pixel detector, the Semiconductor Tracker (SCT) and the Transition Radiation Tracker (TRT). Both the Pixel and SCT are silicon-based detectors, while the TRT is a gaseous straw-tubes detector. A central superconducting solenoid magnet surrounding the TRT provides a 2 T axial-field.

During 2010 the LHC has provided proton-proton collisions at a centre-of-mass energy of 7 TeV, with total integrated and peak instantaneous luminosities for ATLAS of ~48 pb^{-1} and $\sim 2 \times 10^{32}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ respectively. Some of the issues that appeared during the initial commissioning phase of detector (related with the ID evaporative cooling system and the off-detector optical links of the Pixel and SCT detectors) were successfully fixed [2]. Since then, the ID has shown excellent tracking performances and stability during the different data-taking periods, with more than 99% of the channels being fully operational [3]. This is certainly the result of many years of R&D and design iterations before the production, the integration, the installation and the commissioning phases were successfully accomplished.

A major luminosity upgrade for the LHC is being considered for ~2022. The target is to reach $\sim 5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ with $\sim 3000\,\mathrm{fb}^{-1}$ total integrated luminosity at the end of the LHC lifetime around 2030. Given the fact that the performance of the current ID will be continuously degrading with accumulated radiation damage and ageing, a new ATLAS tracker must be designed and constructed. At the expected luminosities, the huge increase in the particle multiplicities mainly coming from overlapping inelastic proton-proton collisions, will produce higher radiation damage in the detectors with fluences of up to $\sim 10^{16}\,1-\mathrm{MeV}-\mathrm{n_{eq}}/\mathrm{cm}^2$ for the smallest radii close to the beam-pipe. In addition to radiation hardness, the new tracker design must ensure low detector occupancy to guarantee good tracking capabilities in a extremely dense particle environment (~100-200 pile-up events).

The current baseline layout for the new ATLAS inner tracker is shown in Fig. 1. It is an all-silicon tracking system with an acceptance of $|\eta| \leq 2.5$, with the innermost region covered by pixel detectors and the intermediate and outer radii by micro-strip detectors. The four pixel barrel layers extend to a radius $R \sim 20$ cm. The innermost pixel b-layer is integrated with the beam-pipe to be as close as possible to the interaction point. The forward region is covered with six pixel disks up to $|Z| \sim 131$ cm. In addition to the planar detectors that are used in the current ATLAS Pixel detector, more recent extremely radiation tolerant detector technologies (3D-detectors, thin silicon sensors, diamond detectors) are being investigated as valid options to be used for the pixel modules. Five silicon micro-strip layers surround the pixels. The innermost three layers are made of short-strip (SS) sensors (24 mm strip length) that allow low hit occupancy while long-strips (LS) detectors (95 mm strip length) are used for the two outermost layers. Most probably the same readout chip will be used in both cases. Each of the strip end-caps is made of five discs, with detectors arranged in petals. The strip barrel and end-cap layers extend up to $R \sim 100$ cm and $Z \sim 280$ cm respectively.

One integration concept for the barrel SS-region is the so-called *stave* concept [5]. The stave is a ~ 1.2 m long object that has a central core composed of a spacing material (carbon-foam or honeycomb) and carbon fiber facings glued on both sides. A bus cable for the electrical signals is laminated on top of the facings. Single-sided silicon micro-strip detectors are glued on the bus cable and hybrids carrying the front-end electronics are glued on top of the sensitive side of the sensors.

The *super-module* is another, more conservative, integration concept in which double-sided silicon micro-strip modules are mounted in a local support structure. In this case, a module is considered to be the minimal detecting unit. The heat generated from the front-end electronics is transferred to the cooling pipes located in the lateral sides of a light-weight local support frame. The local support is designed to

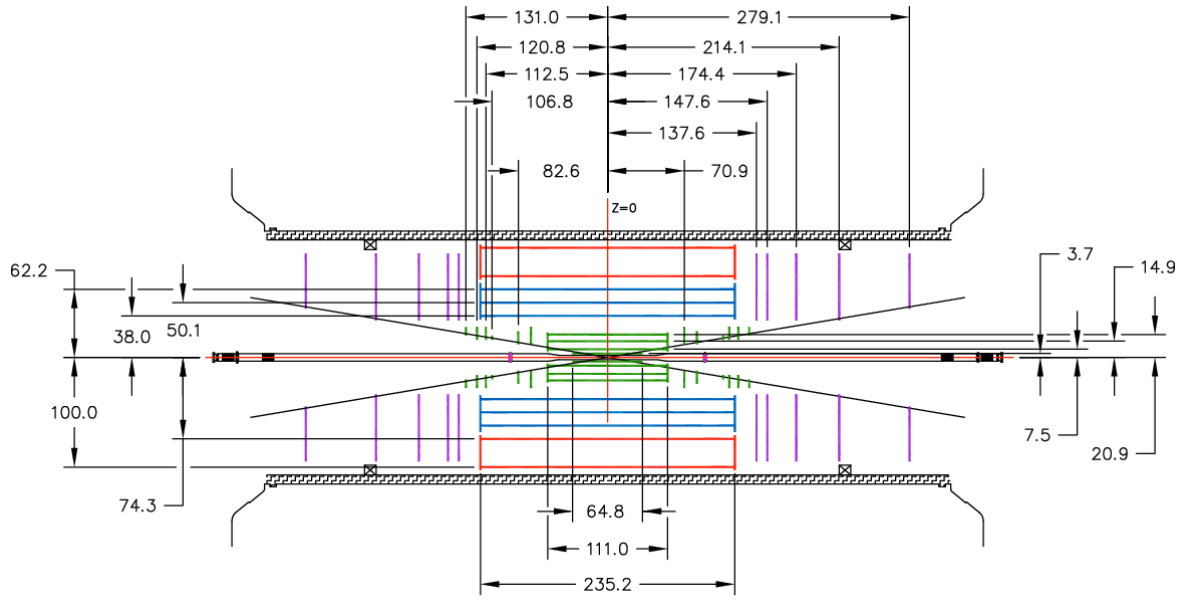


Figure 1. *RZ*-view of the *Strawman* layout for the new ATLAS inner tracker [4].

hold 12 modules enabling a full coverage in both ϕ and Z for the barrel region. This approach allows the end insertion of the support into the overall barrel structure and has been fully adopted because of its flexibility for integration, commissioning and rework. It is also easy to adapt to possible future design changes, for example longer barrel regions.

Based upon the super-module approach, this paper reports on the design and fabrication of first module prototypes for the upgraded ATLAS tracker. An overview of the module design, the main motivations that lead to pursue such integration concept and the material budget estimates are discussed in section 2. The different module components are described in section 3. Results from finite element analysis thermo-mechanical simulations are shown in section. 4. Several modules have already been constructed in two different assembly sites, the University of Geneva (Switzerland) and KEK (Japan). The list of modules built so-far together with a description of the assembly jigs and of a step-by-step mounting sequence are given in section 5. Finally, a summary is made in section 7. The electrical performance of the modules as described in this note is reported extensively in [6].

2 Double-sided silicon micro-strip module design

2.1 Overview

The layout of the double-sided module concept is shown in Fig. 2. It is composed of two $\sim 10 \times 10$ cm^2 n-on-p silicon micro-strip sensors glued to a central Thermo-Pyrolitical-Graphite (TPG) baseboard. The TPG provides mechanical stability and ensures excellent thermal contact for optimum heat dissipation. Two aluminium-nitride (AlN) facing plates are located at each far-end of the baseboard. Four hybrids, two per module side, are bridged on top of the facings using a carbon-carbon sheet underneath the flex circuit so that the hybrids remain electrically and thermally decoupled from the silicon sensors. Precision washers accurately position the module on the support structure. A picture of a fully-assembled module is shown in Fig. 3.

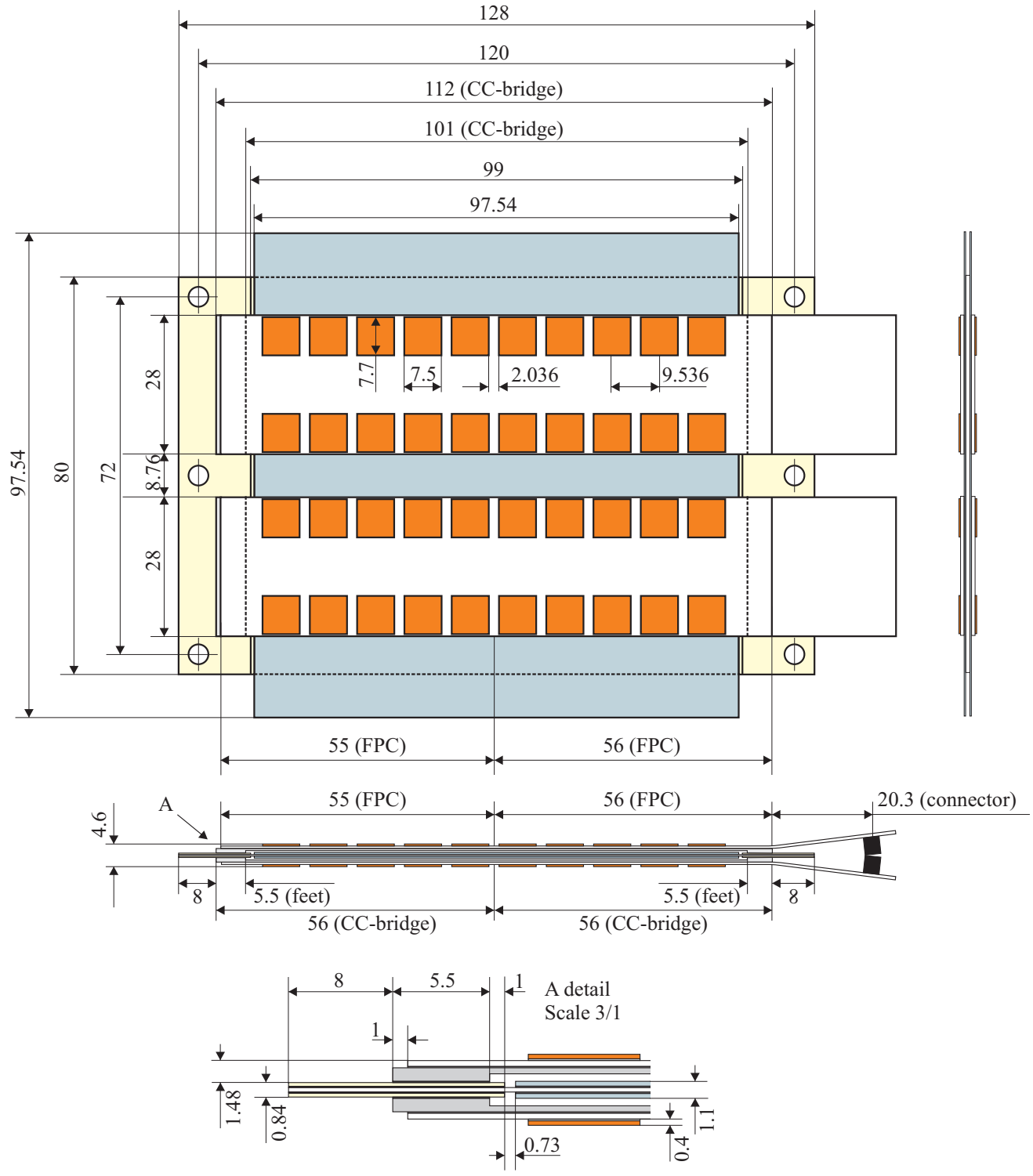


Figure 2. Double-sided silicon micro-strip module (FPC stands for Flex Printed Circuit; CC stands for carbon-carbon).

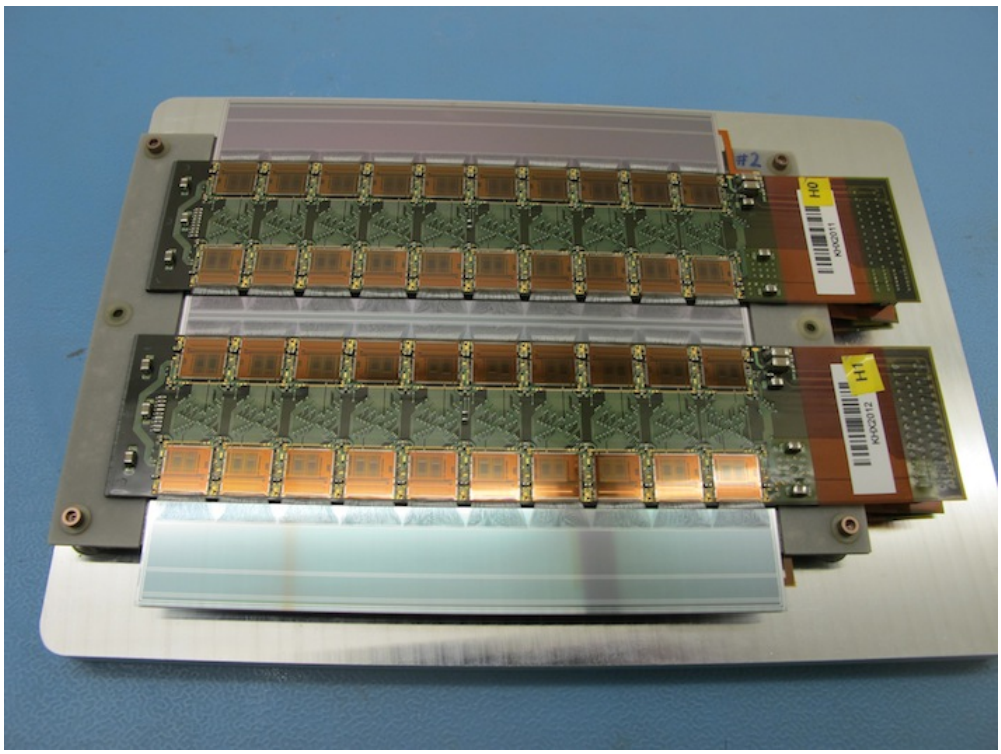


Figure 3. Picture of a double-sided silicon module.

The module concept that is being proposed in this paper is largely inspired by the SCT barrel module used in the current ATLAS ID. That design has proven to be a clear success given the excellent performance of the SCT sub-detector during the LHC data-taking [3]. In addition to the experience already acquired with the assembly of a large fraction of the SCT barrel and end-cap modules, the authors think that a modular approach for a very large area silicon detector for the upgraded ATLAS tracker inherently offers clear advantages that can be profitable for the success of such a large-scale project. These can be summarized as:

- Repairability, repleaceability and design evolution.

  The modules would be assembled individually and directly onto a local support structure containing a cooling circuit. The local structure allows the end insertion of the support into the overall support barrel structure using a rod guiding tool. The end-insertion concept is being adopted because its flexibility for integration, commissioning and rework. Given the fact that the module functionality is decoupled from the support structure, repairability and repleaceability operations are possible up to the last stage of the integration in either the support elements (*e.g.* cooling-loop problems) or individual modules (*e.g.* data communication failures). In those cases where repairs would not be successful, the failure is limited to the loss of a single module.

  Obviously, during the R&D phase for a future strip tracker, there must be regular evaluations of the performance of the whole system (testbeams, system-tests, etc.). The development and design optimization of major components such as the detector modules, support structures (including cooling) and services (electrical connections to a service bus cable, powering schemes, off-detector connectivity, etc.) can be pursued independently (thus optimizing resources). For example, the evaluation of different cooling options (C_3F_8, CO_2, etc.) has little impact on the design of the local support structure or the silicon module itself.

- Space-points for pattern recognition.

  Space-points are three-dimensional points created from the intersection between the $R\phi$ and stereo measurements coming from the two planes of the same double-sided module. In the current ATLAS track reconstruction software *New Tracking* [7], space-points are of great importance since they are used in the pattern recognition stage of the track reconstruction process to seed track candidates before track fitting. The space-point is currently calculated as the intersection between the lines connecting the primary vertex (used as a reference point) and the cluster positions of the $R\phi$ and stereo measurements. The true space-point coordinates lie in a rhombus-shaped region whose axis depend on the strip-pitch and the stereo angle. One can naively assume that the uncertainty associated with the space-point position decreases with shorter separation distances between measuring planes (around 500 μm in the case of the double-sided modules).

  Even if a L0/L1 track-trigger is finally implemented in the upgraded tracker to define *Regions-Of-Interest*[1], space-points are thought to still play a key role in order to reduce hit combinatorics when creating track candidates in a very high track density environment.

- Complete hermeticity.

  The module concept allows to achieve full coverage by maximizing the hermeticity of the strip tracker with detector overlaps in both azimuthal ($R\phi$) and longitudinal (along the beam-axis or Z) directions. The overlaps aim to avoid dead regions which are sources of tracking inefficiencies. The azimuthal overlap is achieved by tilting the modules at a fixed radius, ideally at an angle to compensate for the Lorentz angle that deviates the collected charge within a magnetic field. The longitudinal overlap is obtained by alternating modules at slightly different radii and should be optimized taking also into account the spread in the primary vertex: it is desirable to obtain a uniform projected overlap for particles coming from within $\sim 2\,\sigma_Z$ with respect to the nominal interaction point in order to ensure a reasonable Z-resolution since the ~100-200 expected vertices will have the largest separations along the beam-direction. In the case of having full active-edge micro-strip sensors, the modules would be able to be placed edge-to-edge without dead areas.

  Overlaps are also of particular importance for detector alignment. Both $R\phi$ and Z-overlaps are used to correlate adjacent modules and thus allow to constrain their relative positions. The overlap residuals help to improve the quality of the alignment since multiple scattering effects can be safely neglected (the extrapolation radial distance to adjacent modules is small and thus both hits are highly correlated). The current baseline approach for ATLAS is the Global-χ^2 method, a track-based alignment algorithm that minimizes a χ^2 based on track-hit residuals. The alignment is performed at different levels, starting from large structures (Levels 1 and 2) up to individual modules (Level 3). Profiting from the large statistics available during the 2010 proton-proton collisions, the alignment could be performed up to the module level. Due to the large number of degrees of freedom, the local χ^2 algorithm (a method in which the correlations between alignable objects are recovered through iterations) was used at Level 3. Overlap residuals were used to enhance the hit-correlation through the track fit. The precisions achieved for the Pixel and SCT barrel modules are 4 and 10 μm respectively [8].

[1] The current ATLAS trigger has a hardware-based Level 1 system that is used to make an early event selection of objects of interest above programmable thresholds. The so-called *Regions-Of-Interest* (ROI) include information on the position and transverse momentum of candidate objects (high p_T-muons, e, γ, hadrons/τ, jets) and transverse energy sums. The RoI's are used to seed further trigger decisions (Level 2).

- Distributed mass-production and quality assurance.

  The upgraded tracker would require $O(10^4)$ silicon modules. The production of such a large number of modules will need to be shared among all the collaborating institutes spread around the world. Based on the experience of the macro-assembly of the ID, the integration of the modules into the final support structures is likely to be made at one or two institutes, or even at CERN. It seems reasonable to assume that during the module production phase an easier and more cost-effective parallelization of tasks (assembly, metrology, electrical tests, etc.) would be achievable with objects of reasonable size ($\sim 12 \times 12$ cm^2). This especially applies to the extensive tests expected within the quality assurance programme (*e.g.* thermal cycling) needed to ensure that the modules fulfil the required specifications (still to be defined formally).

- Testeability

  In addition to a design extensively validated in terms of mechanical, thermal and electrical performance, the prototype modules need to be evaluated under realistic conditions (real particles in a testbeam environment, irradiation to the expected fluences, etc.) as well as their integration with the support structures (system-test to study sensitivity to noise pickup, different grounding configurations, interplay with the cooling circuit, etc.). Special emphasis should be put in the tracking capabilities, ensuring that the required signal-to-noise performance is achieved with high track reconstruction efficiency. Once more, relatively small and modular detecting units seem to be more appropriate to perform these kind of mandatory tests.

2.2 Material budget

The estimated material budget for the double-sided module ("as-built" first module prototypes) is summarized in Table 1 and Figs. 4 and 5. The numbers shown in the pie-charts are in percent of radiation length X_0 and they have been normalized to the area of the barrel sensor (9514.0516 mm^2). The reader may refer to appendix C for additional details.

The total radiation-length of the module is 2.44% X_0, being the total estimated weight of 58.7 g. For a hybrid fully populated (including SMD components and ASICs), the calculated radiation length is 0.326% X_0 with a total estimated weight of 7.073 g. A stuffed-hybrid with SMD components but without readout ASICs is estimated to weight 5.92 g. The measured weight is 5.96 g, being the discrepancy with respect to the calculations of less than 1%. Table 2 shows the measured weights of four completed modules. The difference with respect to the estimated weight is around 7% for the first three modules, where no accurate control of the glue dispensing was applied during the assembly. In module GMX-2008, a dedicated mask pattern was used for dispensing the glue over the TPG (see sec. 5.3). The measured weight is closer to the estimations, but it is still 3% higher. This difference is thought to be due to an underestimate of the thickness of the (parylene+TPG+parylene) set, assumed to be (20+600+20) = 640 μm in this case.

The two micro-strip sensors and the 80 front-end ASICs (ABCN-25) of the double-sided module represent respectively 28% and 7% out of the total module material budget. The four stuffed hybrids, each including passive components and the carbon-carbon (CC) bridge, correspond to 1.041% X_0, which is almost 43% of the total of the module. The TPG baseboard and the facings represent respectively 13% and 5% of the total material budget. There is clearly a large room for improvement in what concerns the sensors, hybrid, baseboard and facings. Fig. 5 shows a chart of the estimated material budget for the current KEK hybrid. The major parts contributing to the material budget in this case are the main flex-circuit (35%), the CC-substrate (22%), the readout ASICs (20%), the SMD passive components (14%) and the Samtec connector (5%).

Component	**Rad. length** [% X_0]	**Mass** [g]
Silicon sensors and adhesives		
• Silicon sensors	0.6830	14.181
• High-voltage tongues	0.0004	0.004
• Adhesives	0.0022	0.083
	0.6855	14.268
Baseboard and facings		
• TPG baseboard	0.3027	12.302
• Parylene layers	0.0150	0.468
• AlN facings	0.1175	3.070
• Washers	0.0051	0.203
	0.4403	16.042
ASICs, adhesives and wire-bonds		
• ASICs (ABCN-25)	0.1585	3.292
• Adhesives	0.1019	1.230
• Wire-bonds	0.0042	0.082
	0.2647	4.604
Hybrids, passive components and adhesives		
• Hybrids (w/passive components)	1.0411	23.687
• Adhesives	0.0038	0.145
	1.0449	23.833
TOTAL "AS-BUILT" DOUBLE-SIDED MODULE	**2.4354**	**58.747**

Table 1. Estimated material budget for the "as-built" double-sided silicon micro-strip module. The total radiation length is normalized to the detector area 97.54 mm $\times$ 97.54 mm = 9514.0516 mm^2. Details can be found in appendix C.

Module	**Measured weight [g]**	**Difference wrt estimation**	**Mask for glue dispensing (TPG)**
GMX-2002	62.91	7.1%	no
GMX-2004	63.00	7.2%	no
GMX-2006	62.33	6.1%	no
GMX-2008	60.72	3.4%	yes

Table 2. Measured weights of four double-sided modules. The third column shows the relative difference with respect to the estimated weight of 58.747 g. The last column indicates if a mask pattern was used to dispense the glue on the TPG (sensor-to-baseboard gluing).

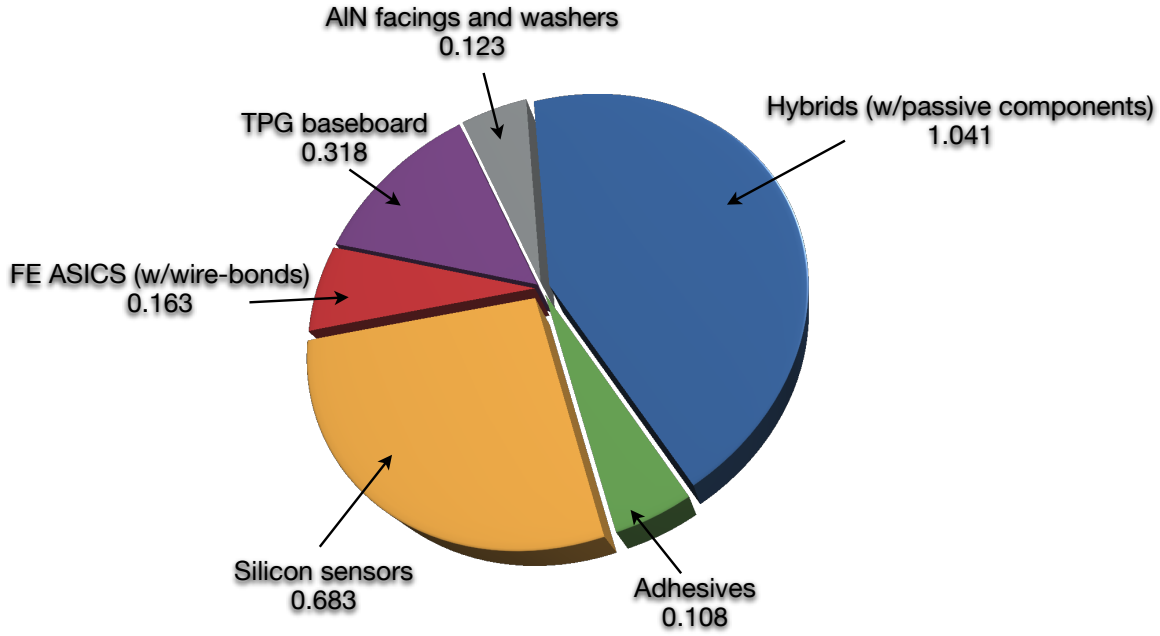


Figure 4. "As-built" double-sided module material-budget (% X_0). The total radiation length is normalized to the detector area 97.54 mm × 97.54 mm = 9514.0516 mm^2. *Silicon sensors* (320 µm-thick) include the two HV-tongues. *TPG baseboard* includes the top and bottom parylene cover layers. *Adhesives* include all (thermal and conductive) adhesives within the module.

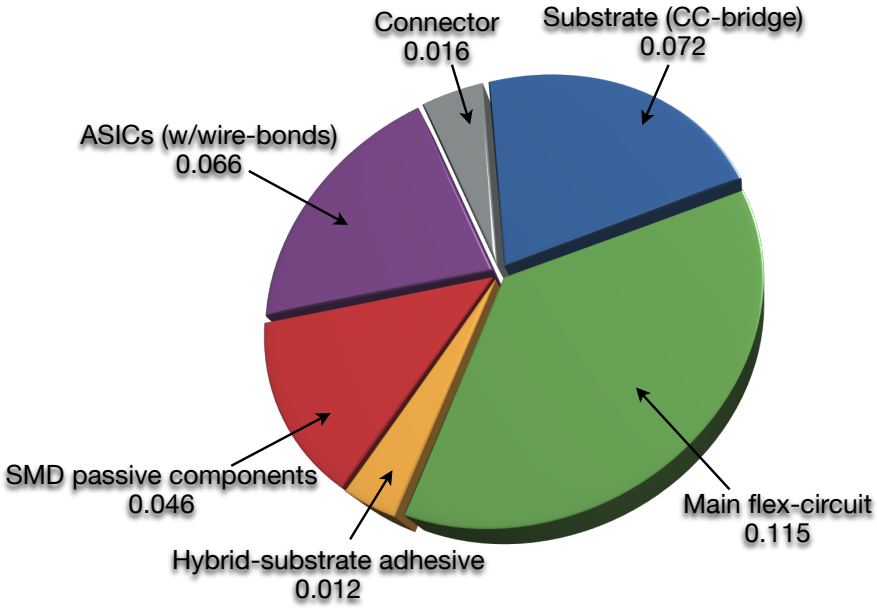


Figure 5. KEK hybrid (v2) material budget (% X_0). The total radiation length is normalized to the detector area 97.54 mm × 97.54 mm = 9514.0516 mm^2.

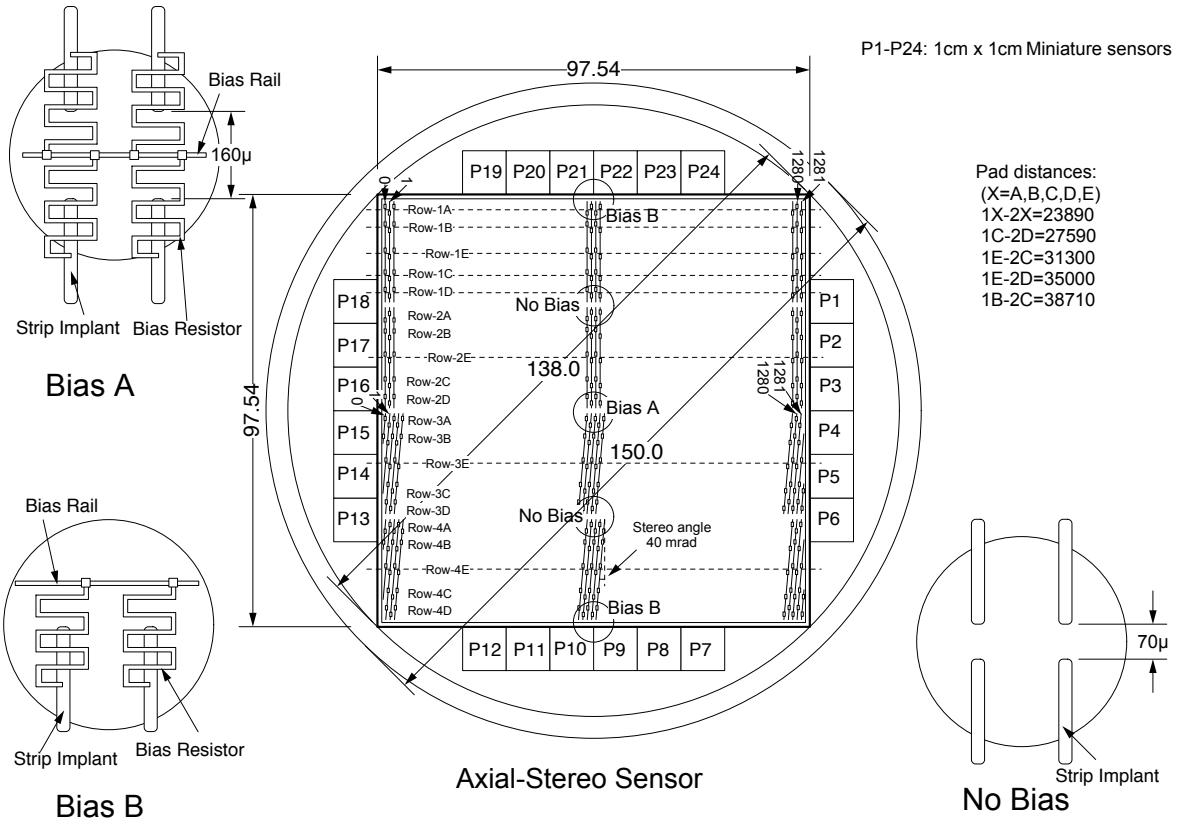


Figure 6. Mask layout of the ATLAS07 sensor. The main sensor (largest area in the mask) is divided into four segments. The top and second from top segments have axial strips; the bottom and second from bottom segments have stereo strips. The 6-inch wafer also contains 24 miniature sensors (P1 to P24) with different isolation structures each (p-stop, p-spray, etc.). The miniature sensors (100 mm^2 total area, 104 axial readout strips with a strip pitch of 74.5 µm) are used for pre and post-irradiation performance studies.

3 Module components

A complete double-sided strip module has been shown in Fig. 3. Its major components, the silicon sensors, the readout ASICs, the hybrids, the baseboard and facings, are described in the following sections.

3.1 Silicon sensors

The ATLAS07 detectors [9] are novel radiation tolerant silicon micro-strip sensors with *n*-type readout strips in a *p*-type bulk developed by the ATLAS R&D group *"Development of n-in-p silicon sensors for very high radiation environment"* [10] and manufactured in 6-inch (150 mm diameter) wafers by Hamamatsu Photonics [11]. These large area n-on-p detectors have the benefits of not suffering type-inversion after irradiation (the sensors would still be operative even if biased under full-depletion voltage) and of being single-sided (significantly lower cost if compared with double-side processing).

The layout of the mask of the ATLAS07 detector is shown in Fig. 6. The large area sensor has a size of 97.54 × 97.54 mm^2 and a thickness of 320 µm. The distance from the sensitive region to the physical cut edge is 980 µm. The detector comprises four segments, two with *axial* strips parallel to the

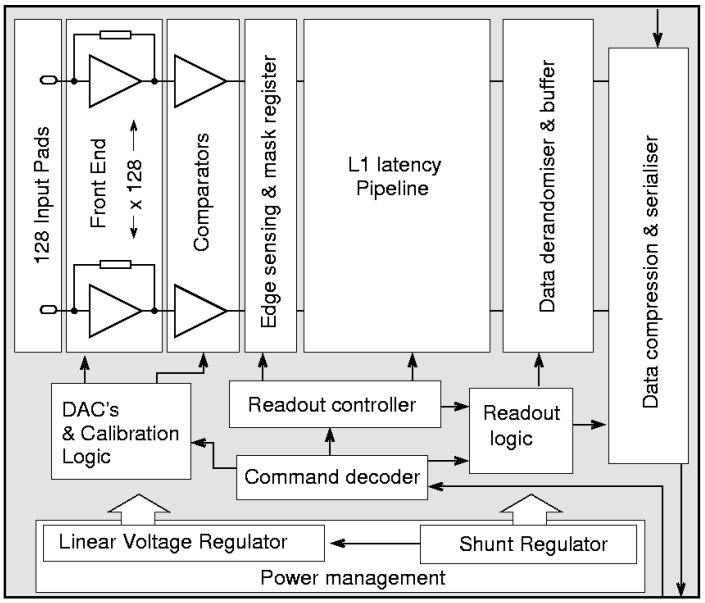


Figure 7. ABCN-25 ASIC block diagram.

sensor edges and two with *stereo* strips inclined by an angle of 40 mrad. The average strip length and pitch is 2.38 cm and 74.5 μm respectively. There is a total of 1280 read-out strips per segment. The bulk substrate is float zone (FZ) p-type with a crystal orientation ⟨1 0 0⟩. The n^+ implants are 16 μm wide, with a maximum resistivity of 200 kΩ · cm. The implants are biased through polysilicon resistors and AC-coupled to 22 μm wide aluminium readout strips that are electrically isolated by a common p-stop trace.

Extensive tests are being been performed by the ATLAS R&D collaboration to study the characteristics of the sensor prototypes in terms of bulk and strip characteristics before and after irradiation. The sensors are found to fulfil all the electrical pre-irradiation specifications, specially in terms of full depletion voltage and leakage current[2] [12]. The sensors are safely operated up to a maximum bias voltage of 1000 V. The performance of the detectors irradiated to the fluences expected for the SS-region (around 10^{15} 1-MeV-neutrons/cm^2) is evaluated in terms of surface and bulk damage, charge collection and signal-to-noise ratio with very good results so far [13, 14].

3.2 Readout ASIC

The Atlas Binary Chip Next (ABCN) is a custom front-end ASIC that has been designed to evaluate the read-out and electrical performance of strip module prototypes for the ATLAS tracker upgrade. The current version has been produced by IBM in the 0.25 μm technology (hence the chip will be referred hereafter as ABCN-25). A new chip (ABCN-13) to be fabricated in 0.13 μm is currently under design. The chip handles 128 read-out channels with a binary architecture and it is conceptually very similar to the ABCD3TA chips used in the current ATLAS SCT [15]. The simplified block-diagram of the ABCN-25 chip is shown in Fig. 7. The per-channel analogue stage comprises pre-amplification, shaping and differential discrimination. The front-end has been optimized for short strips (input capacitances of 5 pF) and it accepts both input signal polarities (compatibility with both p and n-type strips). The binary data at the discriminator output is latched at every clock cycle to the input register and then buffered in a 256-cell

[2]For non-irradiated ATLAS07 sensors, the full-depletion voltage is required to be less than 500 V and the leakage current must not exceed 20 mA at 20 °C.

Register	Length	Type	Read	Write	Purpose
Configuration 1	16	Cached	√	√	Configuration
Configuration 2	16	Cached	√	√	Configuration
Threshold	16	Cached	√	√	Discriminator threshold setting
Bias 1	16	Cached	√	√	Preamplifier currents
Bias 2	16	Cached	√	√	Shaper currents
Bias 3	16	Cached	√	√	Differential and comparator currents
L1 Delay	16	Cached	√	√	L1 trigger latency information
Status 1	16	Read-only	√	-	Status and configuration information
Status 2	16	Read-only	√	-	Status and configuration information
Fuse	16	Read-only	√	-	Unique chip identifier
CalDelay	16	Serial	√	√	Amplitude and delay of the calibration pulse
Trim DAC	16	Serial	√	√	Individual channel threshold correction
Mask	128	Serial	-	√	Disable bad/noisy channels

Table 3. List of registers in the ABCN-25 chip. The length is given in bits.

(6.4 μs) pipeline. Upon the reception of a L1 trigger, the data corresponding to three bunch-crossings is transferred to a second-level derandomizer buffer with 128 bits depth (43 events). Data is then transferred to the readout buffer and compressed according to a given selection criteria. The specifications of the ABCN-25 ASIC can be found in [16].

The configuration of the different chip parameters is made by means of several registers (see table 3). The registers are controlled by the command decoder, which is in charge of interpreting the commands and the control data sent to the chip. The command decoder sends the relevant decoded information to the appropriate functional block for further actions. Most of the serial access registers are of type *cached*, holding Single Event Upset (SEU) information. All cached-type registers allow write/read access. The chip configuration and status (including SEU bits) can be read through a couple of serial read-only Status registers. A 128-bit Mask register is used to disable bad or noisy channels to avoid an increased data rate due to false hits. A chip is uniquely identified by a 16-bit Fuse register (set at the foundry). The ABCN-25 has been designed for a maximum data readout speed of 160 Mbits/s to avoid deadtime. Multiplexing the data of several modules into a single optical link can easily increase the rate to the order of several Gbits/s (with current technologies).

The chips are grouped together in a token chain. There are two possible read-out modes: *standalone* and *module controller* mode.

- In standalone mode (see Fig. 8), the first chip of the chain is configured as “Master”, the last chip as “End” and the rest as “Slave”. When the Master chip receives a L1 trigger (and if its readout buffer contains data), the readout sequence starts immediately. The Master sends a *preamble* bit sequence, its own data and a token signal to the adjacent Slave chip. The latter sends its own data and then delivers the token to the next chip. The data-readout plus token-passing mechanism is repeated from chip to chip up to the one declared as End which issues a specfic *trailer* bit pattern to indicate the end of the readout sequence.

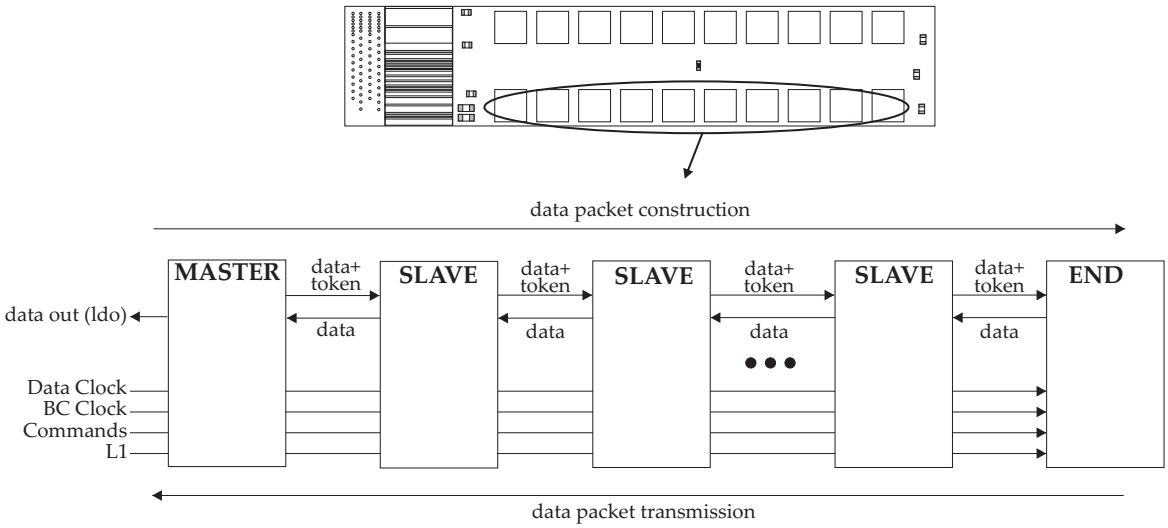


Figure 8. Standalone readout mode of a token chain of several ABCN-25 chips. A chip can be configured as Master, Slave or End (see text for details). The input signals are BC clock, Data clock, Command and L1. The data is serially transmitted off the chain through the Large Drive Outputs (LDO) of the Master chip.

- In module controller mode there is no Master chip, all the chips but the End are configured as Slave. A local Module Controller Chip starts the token-passing mechanism and at the end it gathers the data from all the chips in the chain.

For the future ATLAS inner tracker it is foreseen an increase in the number of electronic readout channels by a factor of ~10. Individual power for each module is simply not affordable due to the number of cables needed, and therefore new powering distribution solutions are required. Two different powering schemes are currently being developed: serial powering and parallel powering using DC-DC voltage converters. In the serial powering scheme, several modules are supplied with a common current source and the required voltage levels are provided by shunt and voltage regulators. In the parallel DC-DC scheme, a unique high input voltage line supplies the modules, and the operating low voltage is obtained typically through an inductor-based buck converter with high conversion ratios and high efficiency [17]. The ABCN-25 chip implements a new power management block with two prototypes of distributed shunt regulator circuits for the serial powering scheme, and a low drop voltage regulator to supply the analog front-end voltage from the digital input. The nominal consumption of the analogue front-end is 0.7 mW per channel. The digital supply current typically is ~90 mA at 2.5 V[3] (40 MHz).

Each channel of the front-end has an internal calibration circuit that can be used to inject a test charge into the analogue chain. Upon reception of a specific command, the voltage pulse is generated by a chopper circuit and injected into the channel through a calibration capacitor. The test charge can be injected in one of the four available calibration input lines, thus every four channel in the chip are tested simultaneously. Measurements of the basic analogue front-end parameters have been performed by mounting ABCN-25 chips on different test board PCBs and prototype hybrids (see section 3.3). Fig. 9 shows a PCB developed to test single ABCN-25 ASICs. Two different data-acquisition systems have been successfully used. One is based on the SCTDAQ test-system (custom VME hardware and ROOT-

[3] ~ 1 V for ABCN-13

based software used to test SCT modules) with extended functionalities to deal with the ABCN protocol. The other one, called ABCNIDAQ, is based on a commercial PXI/PCI high-speed digital input/output card from National Instruments and custom LabVIEW-based software (see [6] for further details). Fig. 10 shows the measured gain and noise at the differential discriminator input for a single ABCN-25 chip. These measurements are based on threshold scans (the discriminator threshold is varied) performed for different charge amplitudes. The input noise is ~400 equivalent noise charge (ENC) and the gain is in perfect agreement with the designed value of 100 mV/fC.

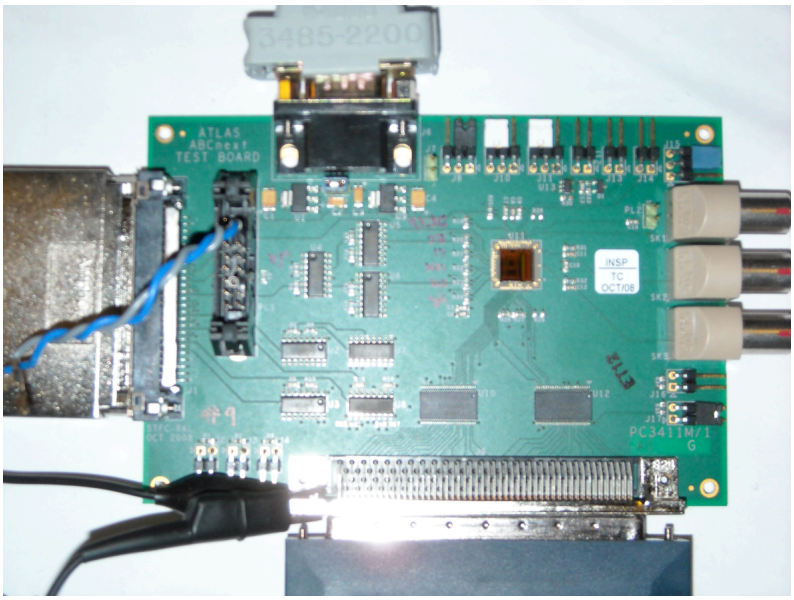


Figure 9. Single chip test PCB [18].

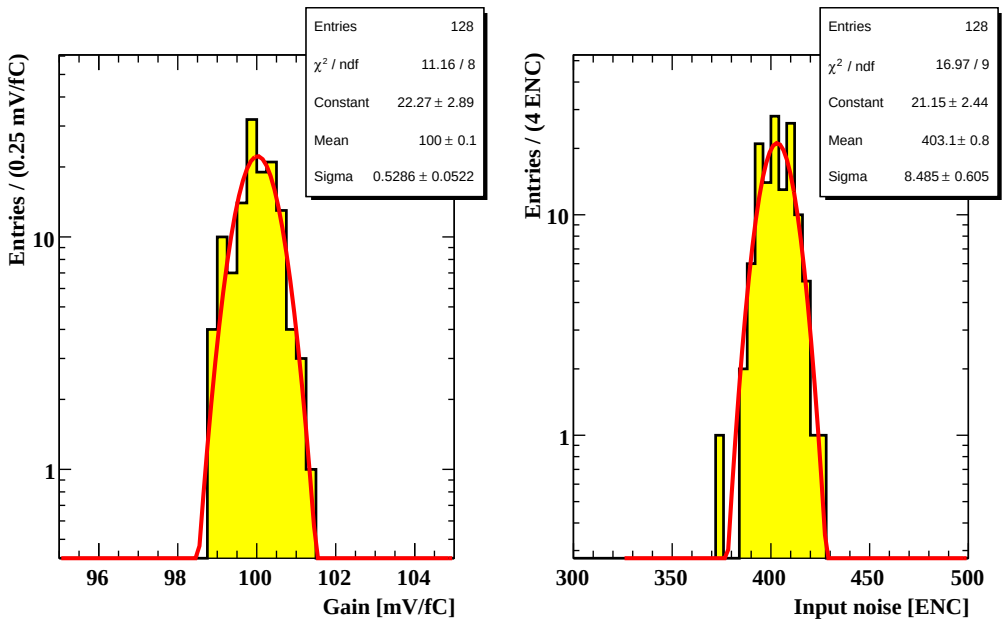


Figure 10. Gain (left) and input noise (right) of the ABCN-25 ASIC. In each case, the statistics box shows the result of a Gaussian fit to the distribution.

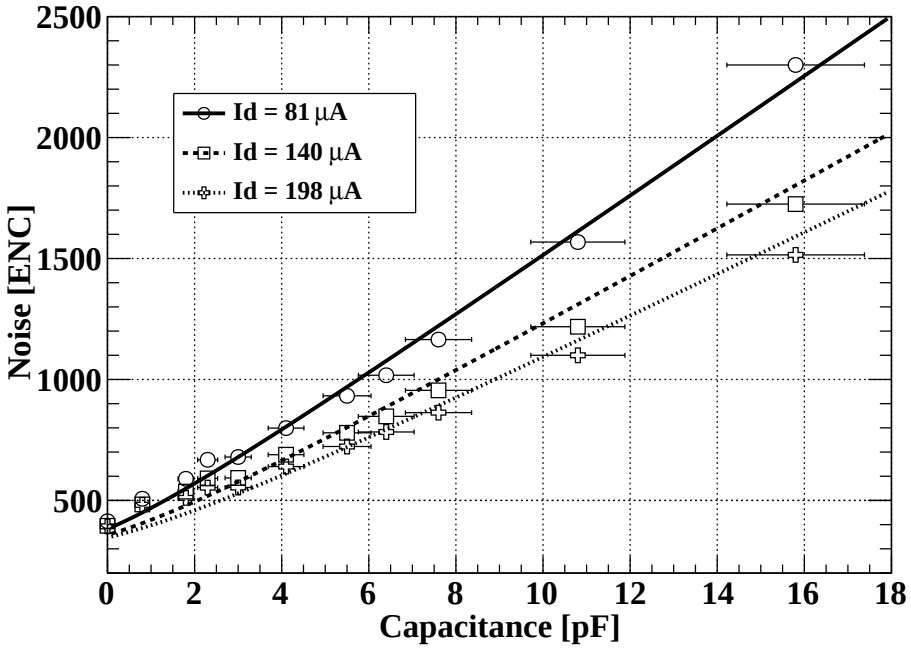


Figure 11. Input noise as a function of input capacitance. Both measurements (markers) and predictions from a theoretical model (lines) are shown. for three different input transistor currents (minimum, nominal and maximum values).

The front-end noise has been measured as a function of the input capacitance. External SMD capacitors were added to two different channels of a single ABCN-25 chip mounted on a test PCB and the input noise was measured. The capacitance of the setup has been estimated to be around 0.8 pF (stray capacitances in the PCB). The external capacitors were varied up to 15.6 fC. Fig. 11 shows the average noise values for the two channels loaded with the extra capacitances and for the measurements performed at two different sites. Three different input transistor currents were used (minimum, nominal and maximal values: 81, 140 and 198 μA respectively). There is a very good agreement between the measurements and an analytical EKV model tuned for the 0.25 μm CMOS technology in which the ABCN-25 chip has been produced [19]. Since the strip capacitances for short and long strips are expected to be around 2.5 and 10 pF respectively, the ABCN ASIC can be even used for long-strip silicon modules with acceptable noise figures by increasing the input transistor current. For the short-strip region, the measured noise is around 600 ENC.

3.3 Hybrids

A four-layer copper-polyimide (Cu/PI) flexible circuit hybrid has been designed by KEK and produced by Taiyo Industrial Co. [20]. The hybrid layout is shown in Fig. 12 and a schematic cross-section along the hybrid length is depicted in Fig. 13.

The size of the flex-circuit is 136×28 cm^2. The first two layers, L1 and L2, carry the main circuit patterns for the front-end chips including redundancy lines, while layer L3 and L4 are used for power distribution and grounding respectively. All Cu/PI sheets are made with adhesive-less technology, being the thickness of the polyimide and copper sheet being 25 and 12 μm respectively. Electrical connections among different layers are realized by either through-holes, penetrating all layers, or laser-cut via-holes between two adjacent layers. The usage of the button plating technology (plating in a limited area around

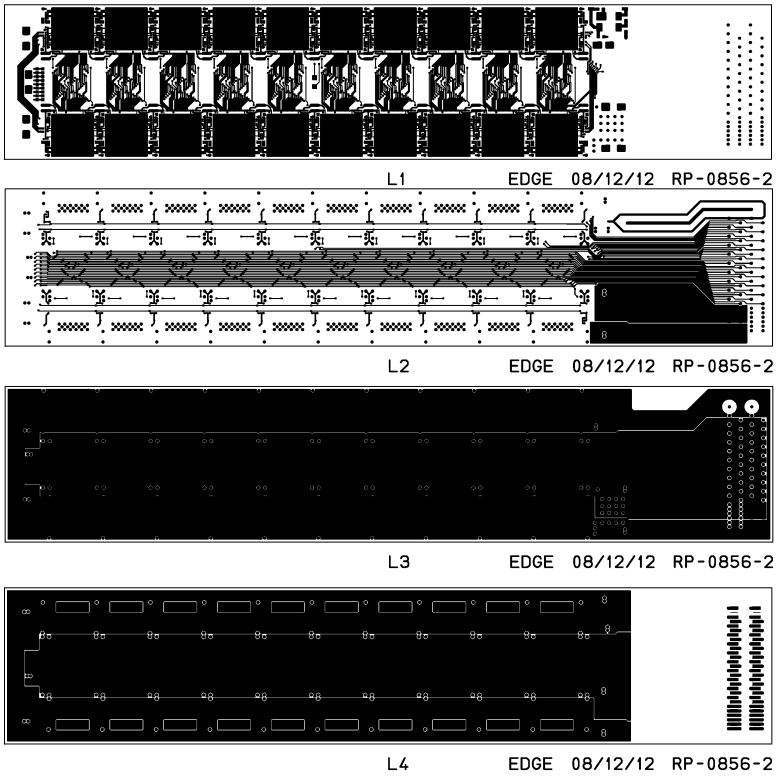
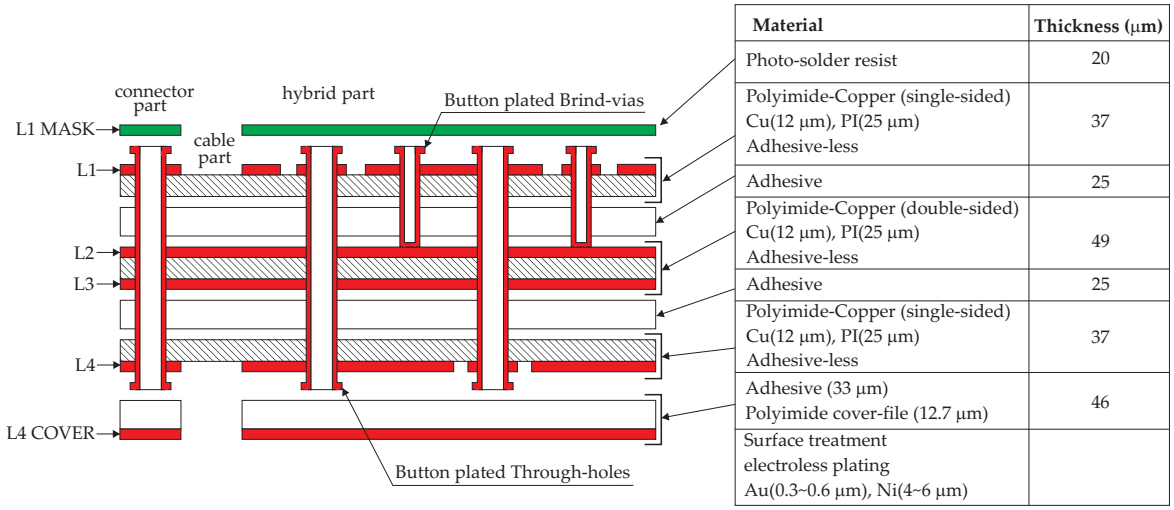


Figure 12. Layout of the KEK hybrid. The four circuit layers are labelled L1 (top) to L4 (bottom).



Material	Thickness (μm)
Photo-solder resist	20
Polyimide-Copper (single-sided) Cu(12 μm), PI(25 μm) Adhesive-less	37
Adhesive	25
Polyimide-Copper (double-sided) Cu(12 μm), PI(25 μm) Adhesive-less	49
Adhesive	25
Polyimide-Copper (single-sided) Cu(12 μm), PI(25 μm) Adhesive-less	37
Adhesive (33 μm) Polyimide cover-file (12.7 μm)	46
Surface treatment electroless plating Au(0.3~0.6 μm), Ni(4~6 μm)	

Figure 13. Schematic cross-section of the KEK hybrid along its length.

the holes instead of having a whole plated surface) allowed to reduce by ∼ 40% the weight of the bare flexible circuit with respect to the standard panel plating technique, achieving a final weight for the hybrid of 1.90 g. Fig. 14 shows the design rules adopted for the various interconnect elements within the hybrid and a close view of the trace layout between chips.

Interconnect element	**Min. value** [μm]
Through-hole:	
• diameter	300
• land diameter	500
Brind-via:	
• diameter	150
• land diameter	300
Line:	
• width	90
• gap	90

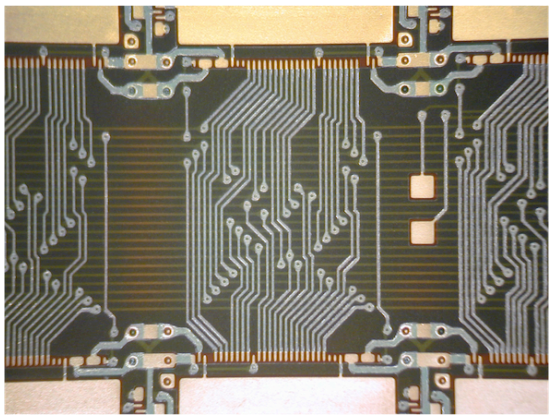


Figure 14. Design rules with minimum values for the different interconnect elements in the hybrid (left) and detail of trace layout between opposed chips (central region of the hybrid) (right).

A 400 μm thick and 112 mm wide carbon-carbon (CC) sheet made of uni-directional fibres is glued underneath the flex circuit to bridge the hybrid over the silicon sensor avoiding any interference with the detector surface. Fig.15 shows pictures of the bare flex circuit top and bottom sides, and after including the CC-sheet on the bottom side. The main functions of the CC bridge is to provide to the hybrid mechanical rigidity and to improve its thermal performance. Seventeen thermal through-holes are added underneath the analogue part of each ASIC. These vertical copper holes are filled with thermally and electrically conducting glue. This ensures thermal and electrical connections between each chip and the CC bridge. The effective thermal conductivity of these pillars is ~ 40 W/m K. The large thermal conductivity of ~ 670 W/m K of the CC-sheet allows the efficient transfer of the heat generated by the readout chips to the heat sink located at the bridge legs. At the last stage of hybrid assembly, a 0.8 mm pitch miniature connector is mounted at one end of the circuit layers to route the LVDS signals towards the data acquisition system. The total weight of the hybrid, including flex-circuit layers and CC-bridge but excluding electrical components (connector, SMDs, ASICs) is 5.03 g, corresponding to 0.002 X_0 equivalent radiation lengths (normalized to the sensor area).

3.4 Baseboard and facings

The baseboard acts as the thermo-mechanical core of the double-sided module. Its design must ensure an optimal heat path allowing an efficient flow from the parts acting as heat sources (front-end chips through the hybrid bridge feet, silicon sensors) to the ceramic facings that will be in contact with the cooling block via thermal grease. The materials to be used should therefore have a high thermal conductivity to help in the power dissipation, in addition to a low coefficient of thermal expansion and a low mass. The Thermal Pyrolytic Graphite (TPG) is a pyrolitic carbon-based anisotropic material with a high in-plane thermal conductivity of ~ 1800 W/m $\cdot$ K and low radiation length. The TPG baseboard is used in direct contact to the silicon sensors. It is sandwiched between four aluminium-nitride (AlN) ceramic pieces which have a relatively high thermal conductivity ~ 180 W/m $\cdot$ K for an electrical insulating ceramic. Furthermore, the use of the AlN facings increases the module stiffness that is reinforced later-on once the two silicon sensors are glued to the baseboard during the assembly process of the module. As seen in Fig. 16, the baseboard is designed with six holes that are intended for the kinematic precision mounting of the module to the support structure and for pressing the module on the cooling blocks. Before the

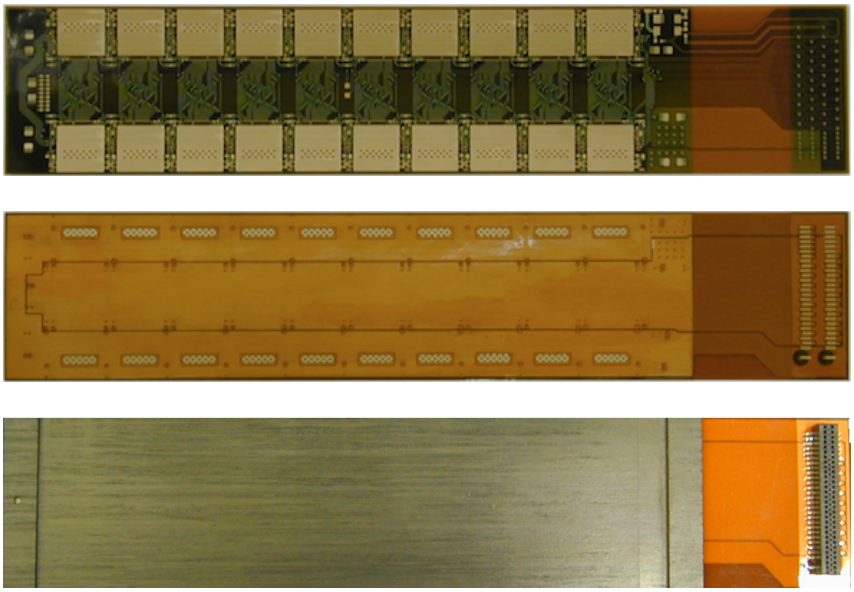


Figure 15. Pictures of the bare flex printed circuit front (top) and back-side (middle), and after mounting the carbon-carbon sheet and the 0.8 mm-pitch miniature Samtec (CLE-130-01-G-DV) connector (bottom). The thermal through-holes underneath the readout ASICs are visible in the middle picture.

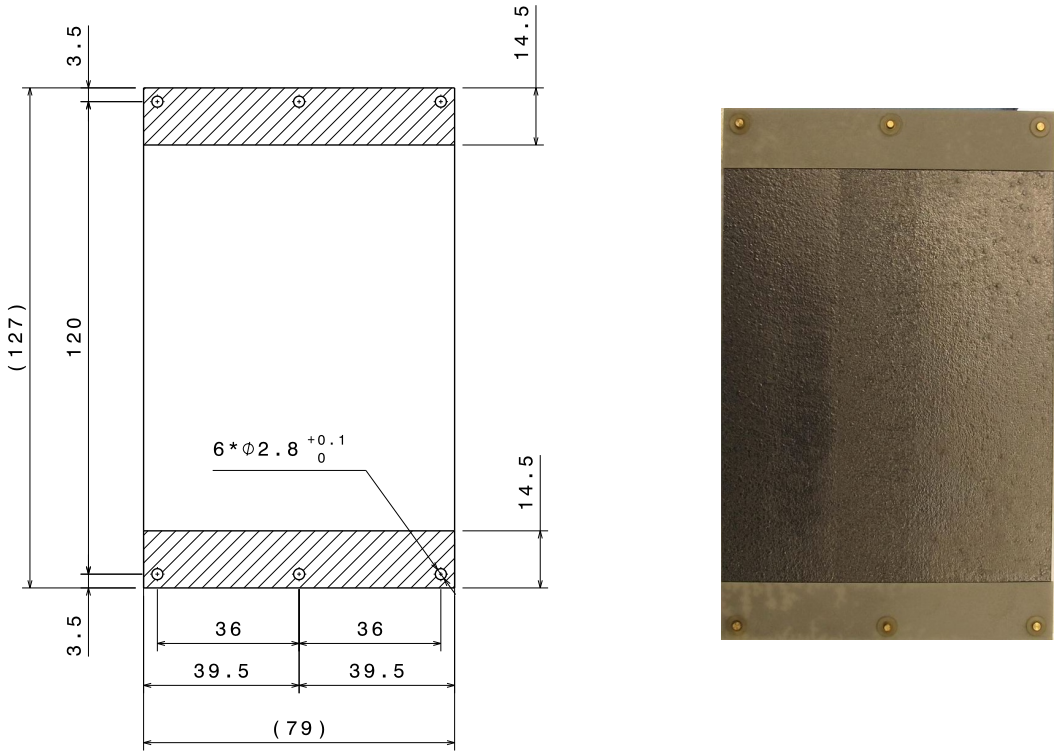


Figure 16. Baseboard design (left) and picture of finished baseboard with facings (right).

assembly of the baseboard, the TPG is sent to a company for a thin film Parylene coating of 10 to 20 µm which allows a complete electric insulation with respect to the HV sensor backplane.

4 Thermo-mechanical performance

The harsh radiation environment expected in the upgraded LHC scenario increases the radiation damage on both the silicon sensors and the FE electronics as a function of the integrated fluence. The defects induced by radiation in the silicon bulk originate a linear increase of the leakage current with the fluence $\Delta I = \alpha \cdot V \cdot \Phi$, where α is the damage constant factor [21] for a fluence Φ inside a volume V. A higher leakage current produces a higher power dissipation in the detectors, an increase of the shot noise and of the integration time of the signal by the electronics. A higher current also increases the power consumption, leading to a higher heat load of the detectors. Since the dependence of the leakage current I_{leak} with the temperature T is exponential,

$$I_{\text{leak}} \propto T^2 \exp\left(-\frac{E_g}{2k_b T}\right)$$

where E_g is the effective gap energy and k_b is the Boltzmann constant, an efficient cooling must be provided to prevent the thermal-runaway, a non-recoverable catastrophic thermal behaviour. The module design must ensure that the maximum heat load is dissipated keeping the module safe against the thermal runaway. The detectors need to be maintained at a uniform low temperature to reduce the reverse annealing and to compensate for the increase of leakage current with fluence.

In addition to radiation hardness, the main mechanical requirements for the tracker are the precision, the stiffness, the stability and the low material budget. Such achievements can be only based on an optimized design with the best material choice (within acceptable cost) taking into account that the detector will operate at several tens degrees below the assembly temperature. Thermal and thermo-mechanical studies based on Finite Element Analysis (FEA) simulations are essential to optimize the module design. The maximum temperature before runaway must be estimated for the expected fluences to ease the selection of basic components (coolant, thermal grease, etc.). The correct choice of materials for the module itself is essential to anticipate the thermo-mechanical behaviour at the operating cooling temperatures.

4.1 Module design and material properties used in the FEA simulations

The thermal management on the module is mainly dependent on the module design, the material selection and the dissipated power. The three-dimensional FEA calculations have been made from a module design implemented in CATIA [22] and then imported into ABAQUS [23]. In the simulated geometry, the two far-end cooling plates and the module itself form a unique structure with a carbon-carbon cover embedding the cooling pipe (see Fig. 17). The module remains a symmetric object, with the cooling circuits running on the two sides along the strip direction aiming to provide a uniform temperature across the silicon detector. A thermal grease compound provides the thermal path between the pipes (with sliding joins) and the cooling plates. The glue (both electrically and thermally conductives) and grease interfaces have been also taken into account. The meshing is based on solid elements using a linear formulation.

Each material has its own thermo-mechanical properties and the main three parameters (in addition to the geometry) that account for the behaviour of an item exposed to temperature changes are:

- the Thermal Conductivity
- the Coefficient of Thermal Expansion Coefficient (CTE)
- the Young Modulus (or elasticity modulus)

In absolute, when considering temperature variations in a given material, the lower its CTE the better. However, more important is the relative difference of CTE between all assembly parts that will build up

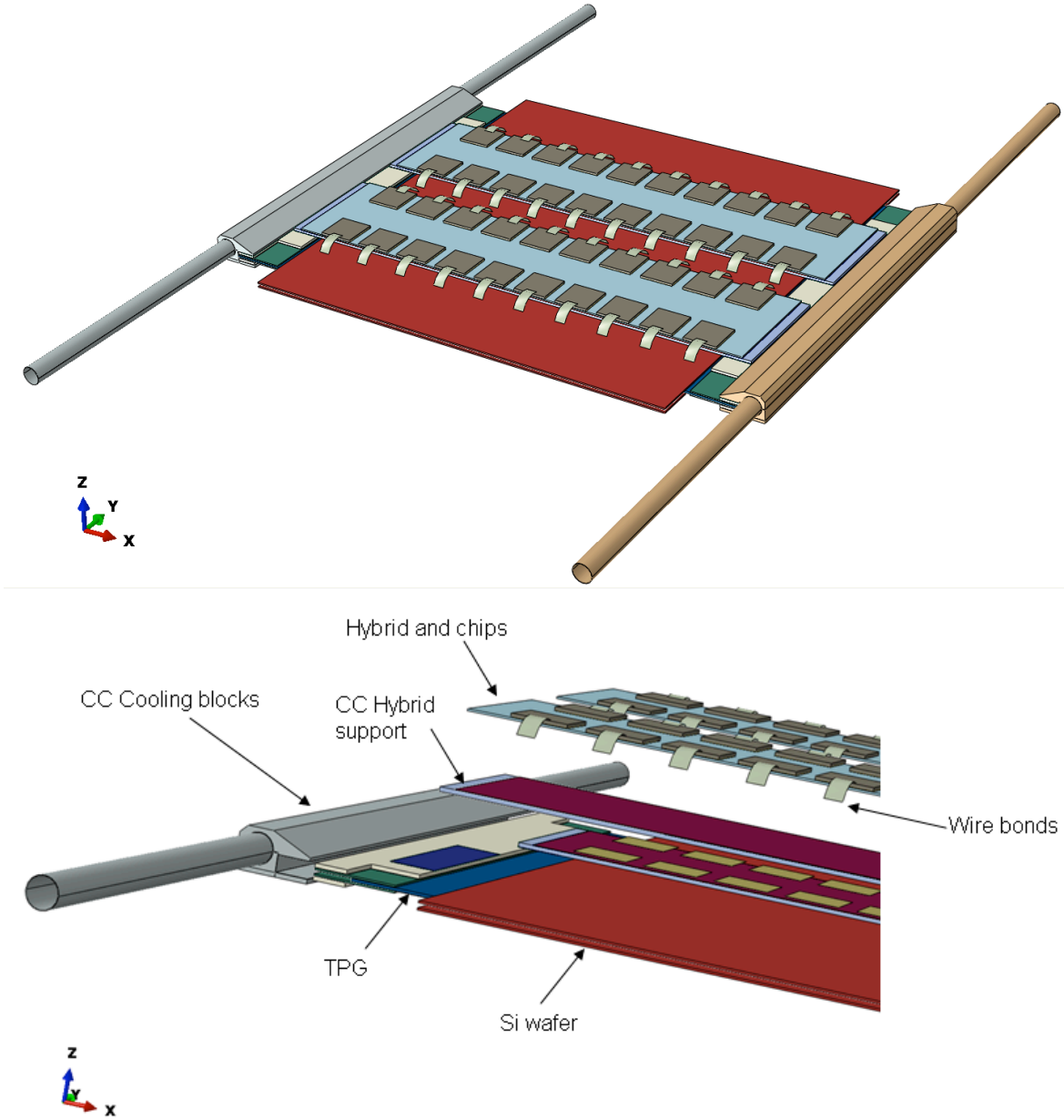


Figure 17. Module geometry used in the FEA simulations.

the internal stresses. The mesh used for the FEA calculations has been optimized in terms of the number of nodes to have reasonable CPU processing times. No big discrepancies have been observed in the stresses due to CTE mismatches between materials (below 20% difference between quadratic and linear elements). Tables 4 and 5 list the thermal and mechanical properties of both isotropic and anisotropic materials used in the simulation.

Table 6 shows the different load-cases that have been simulated. The power load applied (cases 1, 2 and 4) is 0.3 W per chip (24 W per module). A coolant temperature of -30 °C with a Heat Transfer Coefficient (HTC) of 4000 W/m^2 K [24] and an inner pipe diameter of 4.0 mm have been used (other coolants are discussed in section 4.2). The HTC has been implemented as a film exchange coefficient that depends upon the fluid type, the vapour quality inside the pipe and the mass flow [25]. Radiation effects have not been included but their contribution is expected to be small.

Material	**Thermal conductivity**	**Temp**	**Young modulus**	**CTE**
	[W/m · K]	[°C]	[GPa]	[ppm/°C]
AlN 180 ceramic facing	180	-	340	3.1
CuNi pipe	23	-	150	16.2
Cu-kapton polymide	0.2	-	11	25
Sensor (silicon)	210	-40	112	3
Chip (silicon)	130	+40	112	3
Electric conductive glue	2.8	-	7	25
Thermal glue	2.0	-	7	25
Thermal grease	1.6	-	0.01	-
Al wire-bonds	195	-	0.01	23

Table 4. Thermal and mechanical properties of *isotropic* materials used in the FEA simulations (CTE stands for Coefficient of Thermal Expansion).

Material	**Thermal conductivity**	**Temp**	**Young modulus**	**CTE**
	[W/m · K]	[°C]	[GPa]	[ppm/°C]
	x, y, z		x, y, z	x, y, z
CC uni-directional	700, 35, 35	-	294, 70, 70	-1, 10, 10
CC bi-directional	200, 20, 20	-	200	2
TPG	2010, 2010, 6	-40	83	-1, -1, 27
TPG	1530, 1530, 6	+40	83	-1, -1, 27

Table 5. Thermal and mechanical properties of *anisotropic* materials used in the FEA simulations (CTE stands for Coefficient of Thermal Expansion; CC stands for Carbon-Carbon).

Load-case	**Power**	**Convection**
1	ENABLED (chips from both top and bottom-sides powered)	ENABLED (0 °C)
2	ENABLED (chips from both top and bottom-sides powered)	DISABLED
3	DISABLED	ENABLED (0 °C)
4	ENABLED (chips from only top-side powered : **dissymmetry**)	ENABLED (0 °C)

Table 6. Load-cases considered for the FEA studies.

The FEA model also allows to simulate the air-gap transfer between close components, such as the interaction between the top part of sensor and the bottom part of the hybrid support bridge. Here it has been considered as a stationary air-gap, *i.e.* a poor thermal exchange between closely adjacent surfaces, the exchange being characterized by the Thermal Conductance Coefficient k (k=conductivity/gap). An air conductivity of 0.026 W/mK, and a gap of 0.5 mm have been chosen. Thus there was no need to add an extra-meshing to model the air, which is delicate in terms of stress distribution and is CPU time consuming.

4.2 Thermal FEA simulations

Several simulations have been performed with different HTC values for the natural convection exchanges, and several sink temperature (0 °C, -10 °C, 10 °C). The comparative studies showed no big thermal variations on some critical components such as the silicon wafers or the hybrids (variations in the sensor temperature of 0.3 °C for different sink temperatures). The HTC values that have finally been used for the top and bottom parts of the horizontal planes are respectively 5 and 1 W/m^2 K.

Fig. 18 and 19 show respectively the heat flux across all solid elements and the temperature distribution in the module and sensors (load-case 1). Table 7 summarizes the thermal results for all four load-cases. The results show that 60% of the heat flow goes through the hybrid feet to the facings, 30% and 10% to the sensor via the air gap and wire-bonds respectively. The maximum temperature obtained for the hybrid and sensor is -13.5 °C and -22.1 °C respectively. A uniform temperature in the sensor has been obtained, within 1.0 °C. This is found to be acceptable for a chip power consumption of 0.3 W. When considering a future ASIC in 130 or 90 nm technology, the maximum power is expected to be $\sim$ 1 mW per channel, leading to a power reduction by a factor of $\sim$ 2.5 with respect to the current FEA simulations.

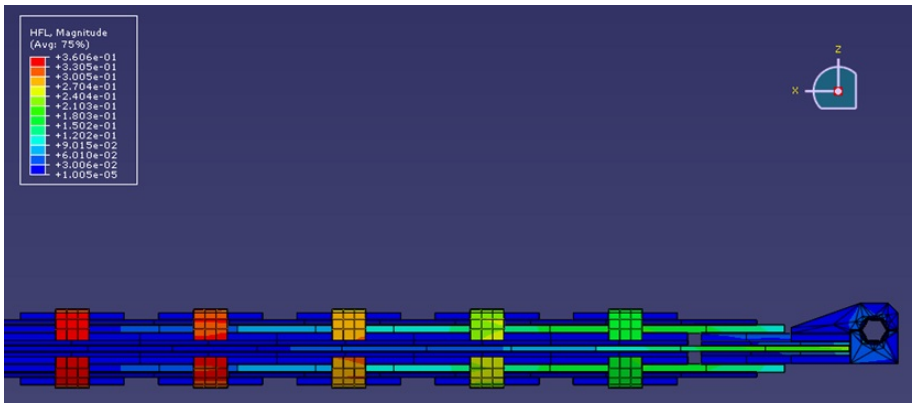


Figure 18. Cross-side view of the module with heat flux distribution.

	Load-case			
	1	2	3	4
Max T on sensor (°C)	-23.0	-23.2	-29.7	-26.4
Max T on hybrid (°C)	-13.5	-13.9	-29.2	-16.3
ΔT on sensor (°C)	1.0	1.0	0.03	0.5

Table 7. Maximum temperatures obtained for the sensor and hybrid, and maximum temperature variation across the sensor for all four load-cases.

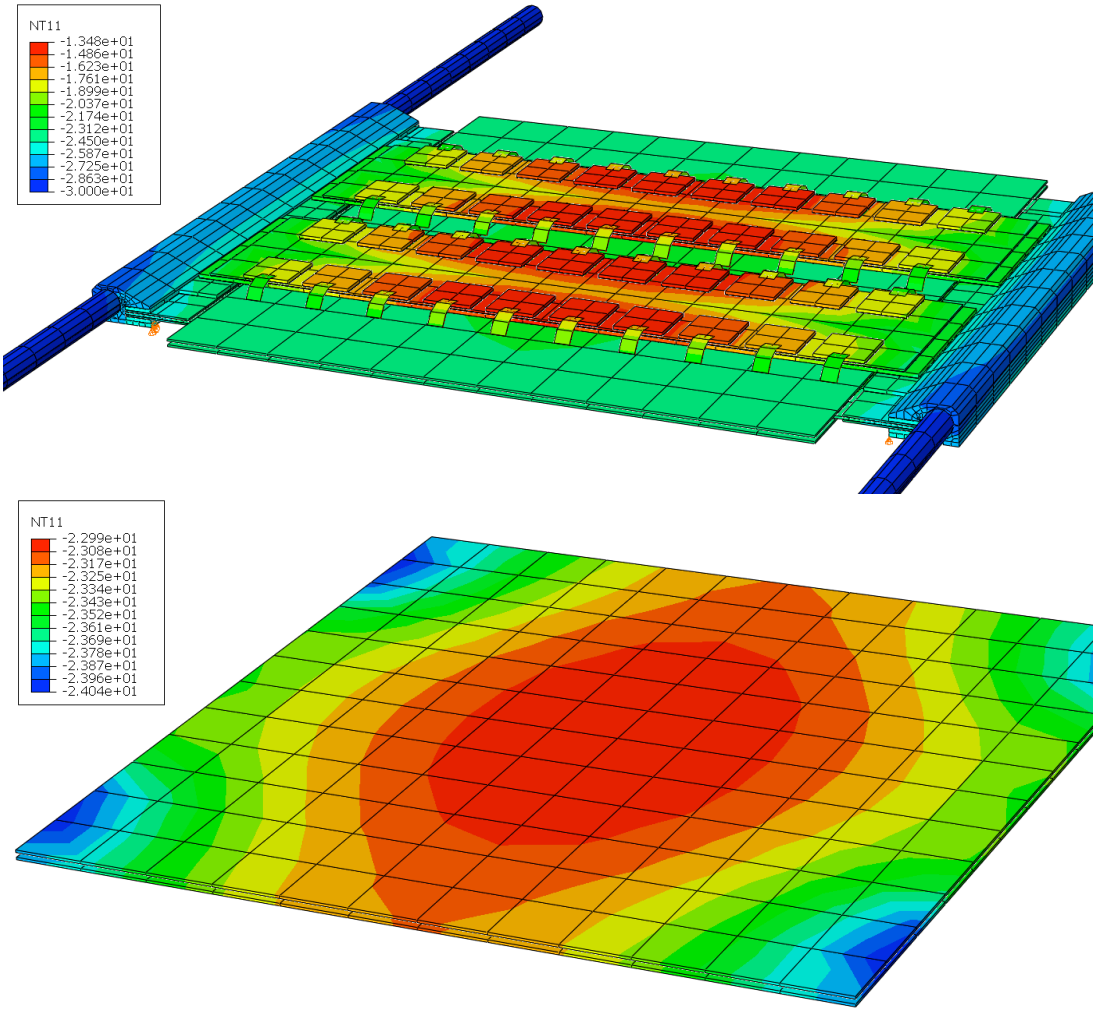


Figure 19. Temperature distribution across the module (top) and across the silicon sensors (bottom) for load-case 1 (see table 6). In the case of the module, the temperatures range between -30 and -13.5 °C; for the sensors, the range is from -24 to -23 °C.

Two types of evaporative cooling systems have been compared:

- C_3F_8 (as used in the current ATLAS Pixel and SCT sub-systems) assuming a HTC of 4000 W/m^2 K [24] and an inner pipe diameter of 4.0 mm.
- CO_2 assuming a HTC of 8000 W/m^2 K [26] and an inner pipe diameter of 1.8 mm.

In both cases, a coolant temperature of -30 °C has been set. The simulation results show a similar thermal performance for the two types of coolants. That is explained by the fact that the reduction of the HTC in C_3F_8 with respect to CO_2 is compensated by an increase of the pipe exchange surface. The advantages of CO_2 are clear, as it provides a reduced material budget and a higher safety margin provided by the minimum temperature that can be achieved[4].

[4]Even if -30 °C has been taken in the FEA, an evaporation temperature of -35 °C can be reached with a CO_2-based cooling system.

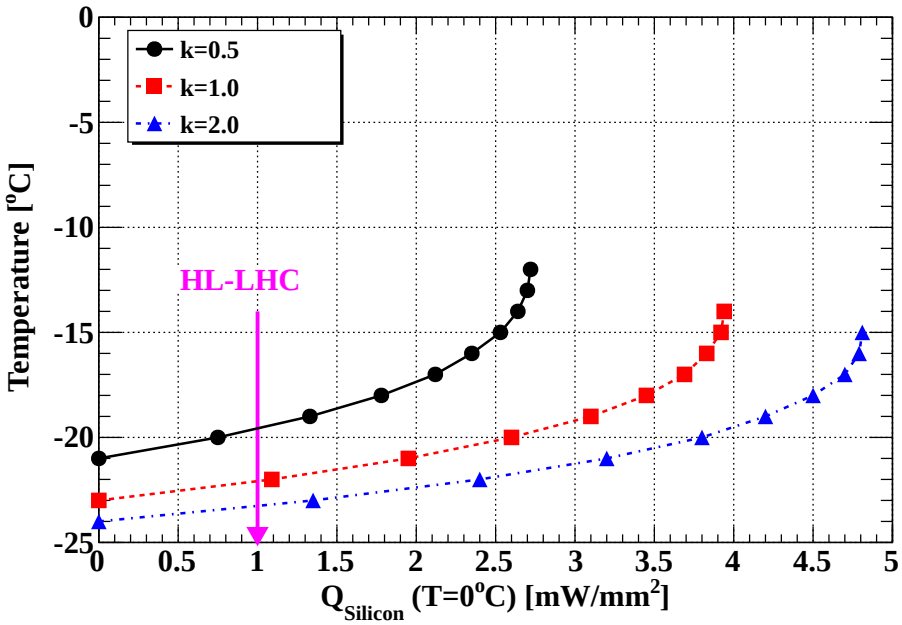


Figure 20. Thermal runaway curves computed for three different values of thermal grease conductivity.

Additional FEA calculations could be performed by easily changing the material thicknesses and conductivities and the boundary conditions, therefore allowing an optimization of the design by evaluating the effect of a given parameter in the thermal performance. For example, the grease layer compound, which has to be qualified in terms of thermal conductivity, radiation hardness and assembly practicality, is a key material since it allows a modular assembly with reduced stress between the cooling pipe, the local support and the module. Depending on the provider and on the loaded compound, the thermal grease conductivities range from 0.5 to 2.0 W/mK. Based on the FEA simulations and the dependence of the leakage current with the temperature, thermal runaway curves can be extracted. Fig. 20 shows the maximum silicon temperature as a function of the silicon power density normalized at 0 °C. Three different values of thermal grease conductivity, 0.5, 1.0 and 2.0 W/mK, have been considered. The power density expected for a maximum fluence of 1.5×10^{15} $1-\text{MeV}-\text{n}_{\text{eq}}/\text{cm}^2$ at 30 cm from the interaction point is 1 mW/mm^2. This module design is shown to have a safety margin of at least a factor of two to the runaway point for the large range of thermal conductivities simulated (thermal grease layers of 70 µm thickness).

Detailed studies have been also performed using different thermal grease compounds [27]. A dedicated setup was used to determine the thermal conductivity of samples before and after irradiation with a measurement error of the calibrated temperature sensors of 0.1 °C. Known fluids (water, glycerol, silicon oil) were used as control samples to assess systematic uncertainties. The thermal conductivities obtained were found to be compatible with datasheet values within a 5% error. A very good agreement was found with the FEA calculations after inclusion of convection and radiation effects into the simulation (convection coefficient of 5 W/mK). It was found that the thermal conductivity of the samples tested were not significantly affected by fluences up to 1.0×10^{15} $1-\text{MeV}-\text{n}_{\text{eq}}/\text{cm}^2$. The silicon-based DC340 compound [28] suffered polymerization, and therefore silicon-based compounds should be discarded when sliding grease joints are required.

4.3 Thermo-mechanical FEA simulations

When a module is at room temperature (assembly and machining temperature), the internal stresses between the different materials should be low or even null. The correct choice of the materials and the conceptual design itself, are essential to anticipate the thermo-mechanical behaviour when operating at temperatures of the order of -35 °C. Internal stresses are distributed to all mechanically joined parts. The final figures of merit are the mechanical displacements and the maximum stress that the material can stand with its mechanical properties not being affected. For example, a stress that leads to plastic deformation (yield point) of a solid is prohibited. If in addition the temperature cycles are occurring many times during the life-time of an item, the fatigue will end-up damaging the whole assembly.

Bonded joints provide a more uniform stress distribution than other methods of joining which rely on single joint contacts, such as bolting, riveting and spot welding, where high stress concentrations occur. Polymeric adhesive or glue joins are therefore often used in the assembly for modules and other structural parts. But the static and fatigue properties of polymeric adhesives can be influenced by environmental conditions such as temperature, moisture, chemical agents and radiation environments. For the double sided strip module, the glue joints are located at different interfaces, for example between the sensor and the TPG baseboards and between the hybrid bridge feet and the AlN facing. The complete double sided module will have kinematic mounting bolt screws. One screw allows a precise location for the origin of the module and another one for the alignment while the remaining two will allow a free displacement in the plane (see Fig. 21).

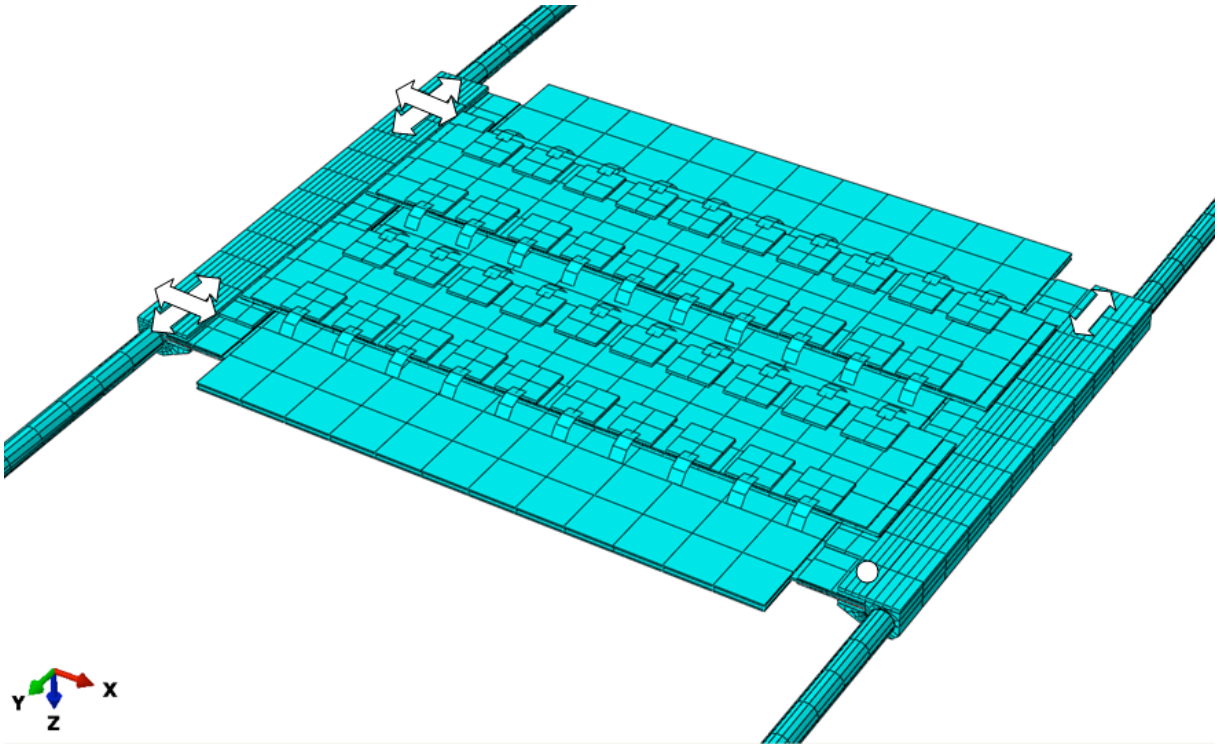


Figure 21. Meshing of the module with its four mounting points, where 2 are kinematic mount bolts.

The local support structure on which the 12 double sided modules are mounted is made of composite material with low CTE. Each local support will then be mounted on a barrel structure of the same kind of material, which means almost no induced thermo-mechanical stresses. Therefore, the only significant thermo-mechanical stresses that can be anticipated with the FEA simulations are on the module itself.

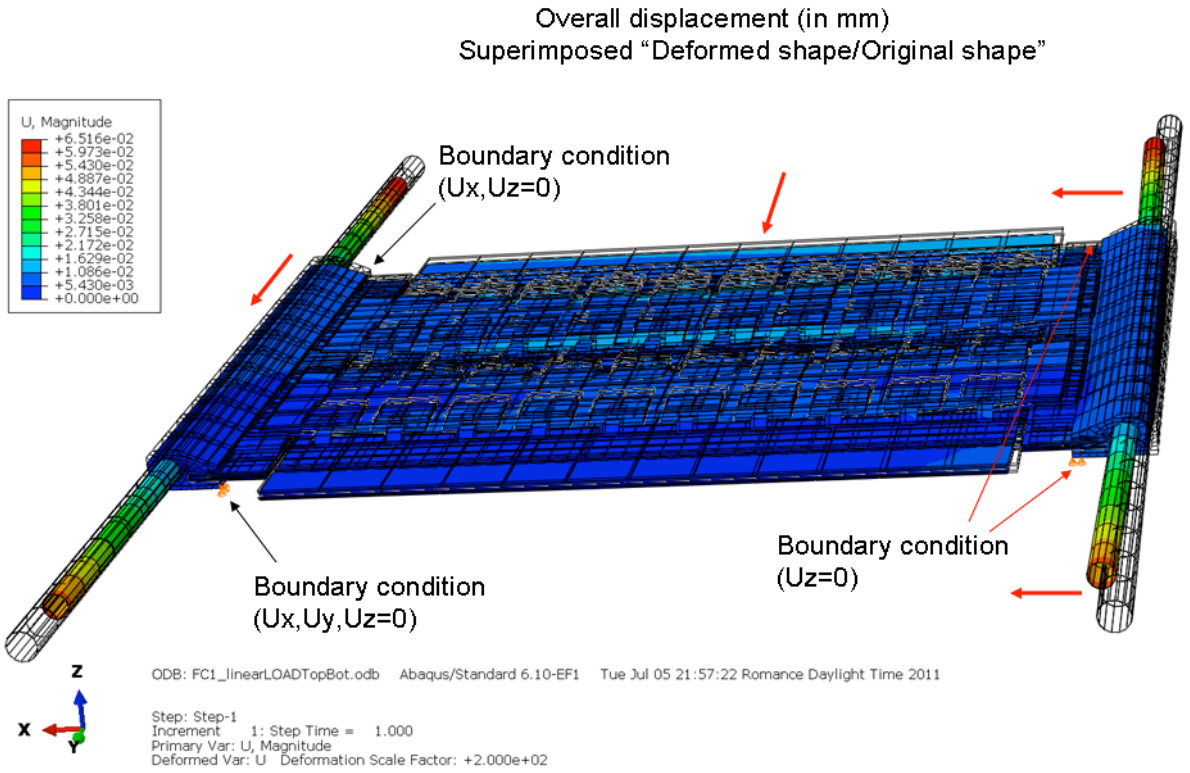


Figure 22. Mapping of the overall displacement (load-case 1, see table 6). For clarity, the deformation scale factor has been set to 200.

The thermo-mechanical simulation uses a special "interaction" to connect the different components (*e.g.* the connection between the glue and the TPG or the silicon wafer), where not only the temperature is transferred from one node to the next, but also the three translational degrees of freedom when fixing mechanically the components. Figs. 22 and 23 show respectively the displacements and the internal stress distribution on the full module. In the former case, the displacements have been magnified by a factor of 200 for illustrative purposes. The pictures reflect the high quality of the model, with all components being connected by dedicated nodes/meshes.

In this analysis, the Von Mises (VM) yield criterion is used. The VM stress is a scalar value computed from the 3×3 stress tensor[5] that allows to predict the Yield strength of the stressed material (elastic limit). Fig. 24 shows the distribution of VM stresses for a particular load-case (values have been averaged per mesh to avoid edge effects). The maximum stress is about 14 N/mm^2, which is quite acceptable as yield-point for the silicon. Some refining of the meshes have been performed but no significant variations in terms of VM stress distributions have been observed.

Figs. 25 and 26 show respectively the related three-dimensional deflection and the sagging effect or bowing (out of plane deflection along the Z-axis) of the silicon sensors. The maximum deflection (opposite corner) is of the order of 12 µm and the maximum sagging deformation is ~3 µm.

One of the most critical regions in terms of mechanical stress is located on the TPG baseboard.

[5]The stress tensor is a symmetric tensor with six degrees of freedom (3 normal stresses and 3 shear stresses), that is used to specify the stress at any point of the object

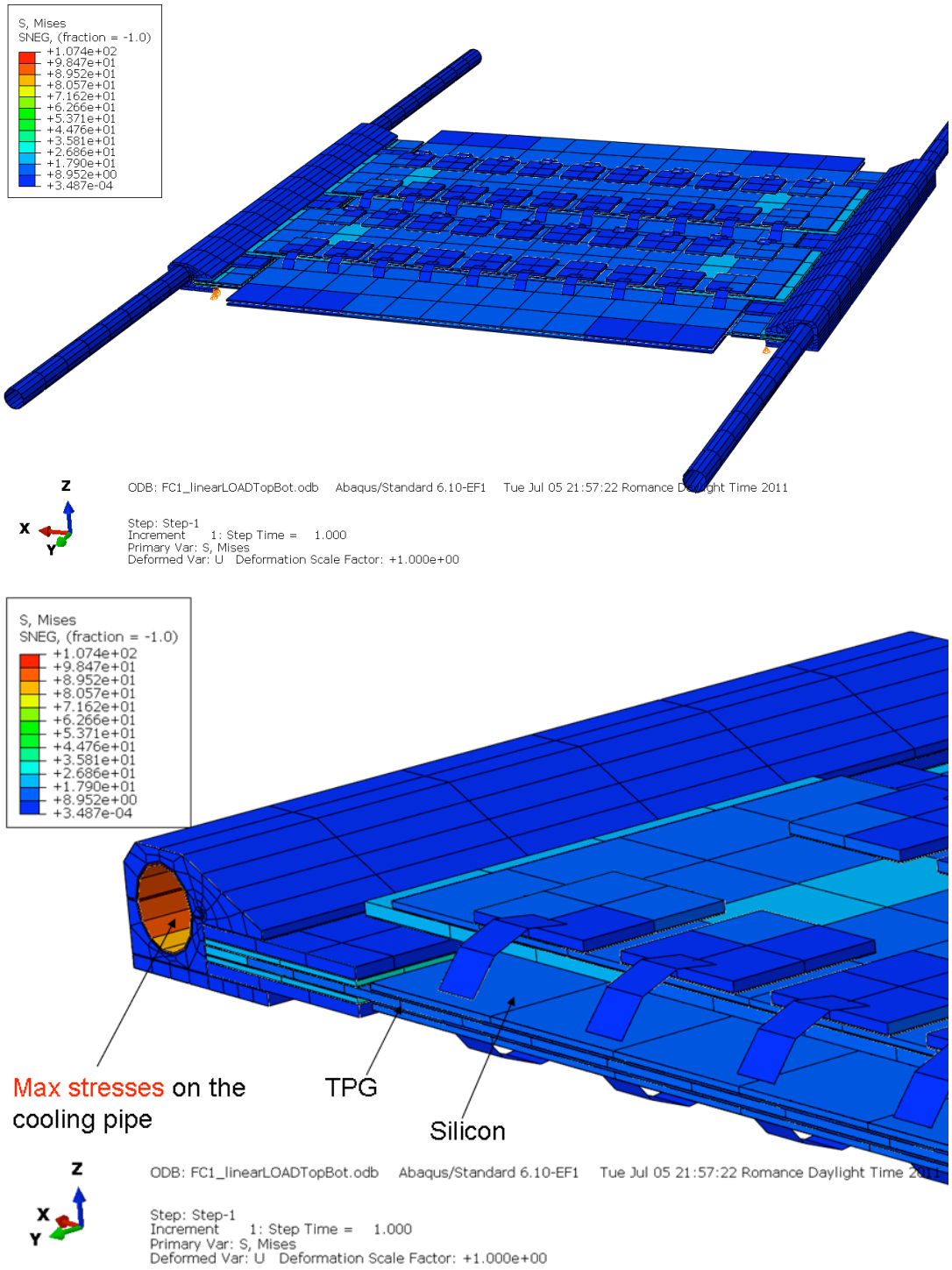


Figure 23. “Von Mises” stresses mapping (top) and close-up on the cooling pipe (bottom).

Fig. 27 shows the stress mapping at the interface between the silicon and the TPG (the parylene cover layer has been neglected in terms of thermo-mechanical analysis). The results show a relatively good safety margin (factor of 2) against the TPG yield point (~40 N/mm^2), with stresses in the most relevant region (edge) of the order of 20 N/mm^2.

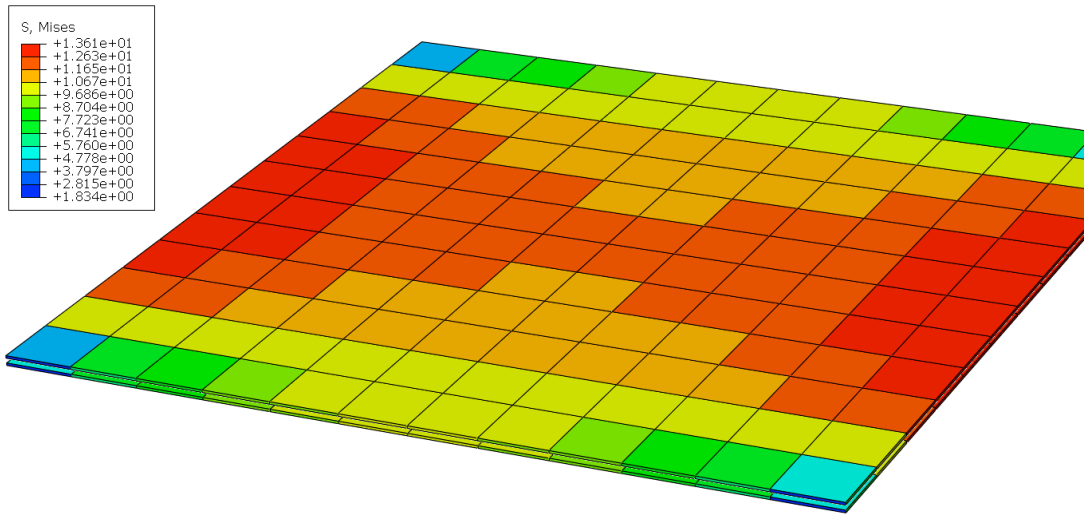


Figure 24. Distribution of Von Mises stresses on the silicon wafers (load-case 1, see table 6).

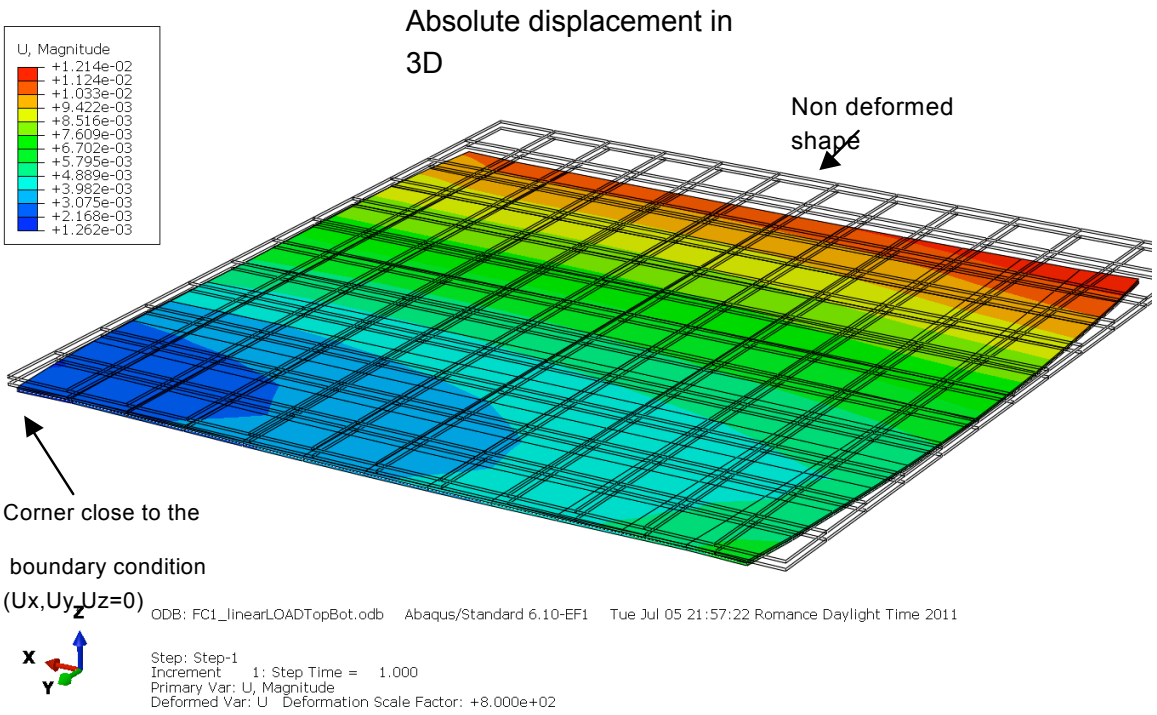


Figure 25. Three-dimensional deflection on the silicon wafers (load-case 1, see table 6).

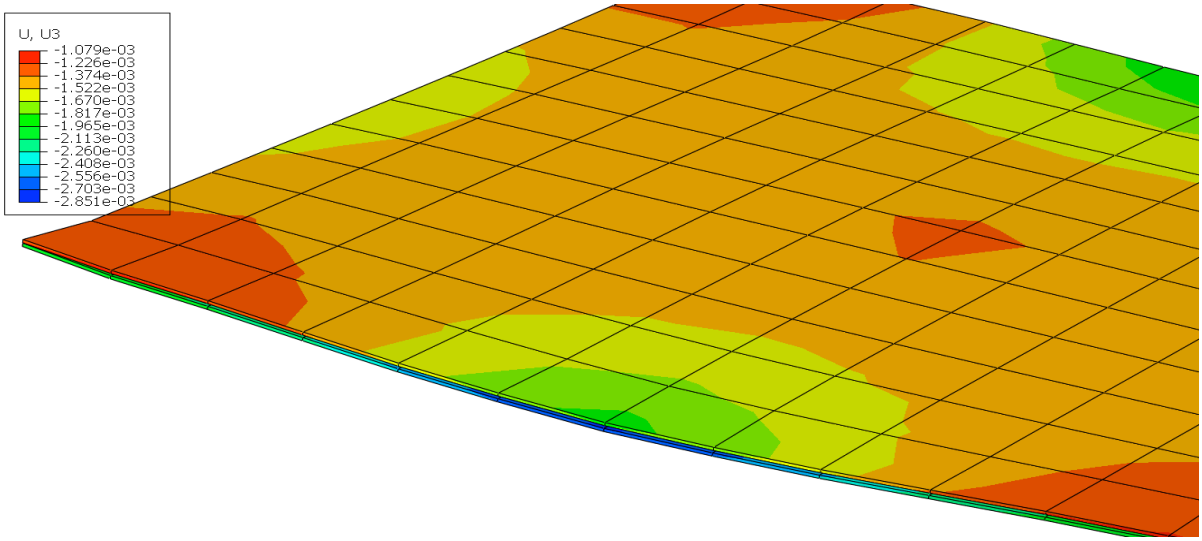


Figure 26. Sagging deformation of the silicon wafers (load-case 1, see table 6).

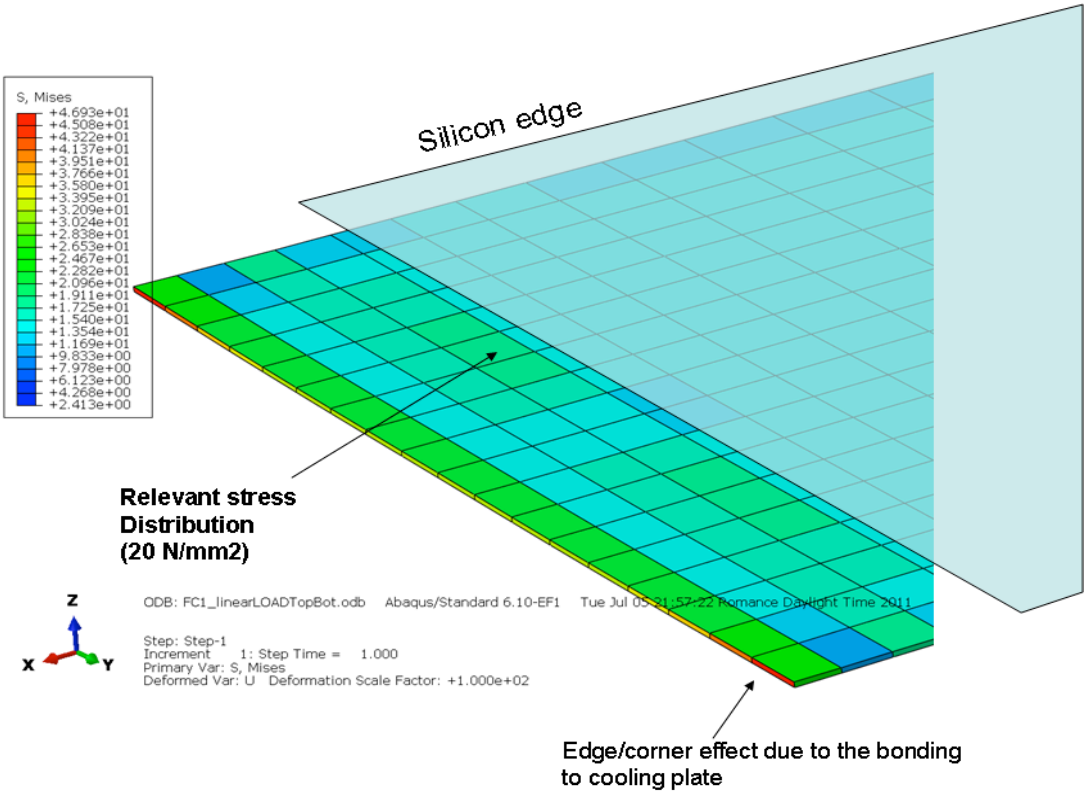


Figure 27. Von Misses stress map at the junction sensor/TPG (load-case 1, see table 6).

	Load-case			
	1	2	3	4
Max VM stress on sensor [N/mm^2]	13.6	13.7	15.9	14.7
Max VM stress on TPG [N/mm^2]	~20.0	~20.0	~21.0	~21.0
Max bowing on sensor [μm]	-2.8	-2.8	-2.9	-2.7

Table 8. Maximum stress and bowing for all four load cases (VM stands for Von Mises). A thermal grease conductivity of 1.65 W/mK has been taken in all cases.

Table 8 summarizes the results obtained with the thermo-mechanical FEA simulations in terms of maximum Von Mises stress for the sensor and TPG, and the maximum bowing in the detector. As expected, the convection has almost no impact in the stress analysis. The VM values obtained give good safety margins with respect to the yield strength of silicon (~150 N/mm^2) and TPG (~40 N/mm^2). The maximum out-of-plane displacements are of the order of 3 μm.

5 Module prototypes

Following the module design explained in section 2 and using the components described in section 3, both the University and Geneva and KEK have built a number of double-sided module prototypes (see tables 9 and 10). The modules are categorized depending on the version of the KEK hybrid (version 1/2 for GMX/KMX-100x/200x modules). All modules used so far float-zone 1 (FZ1) sensors with or without p-stop. Module KMX-2003 was the first being produced in industry, and hence hybrids with some dead chips known beforehand were used for the assembly in any case. The electrical performance of these modules is reported extensively in [6].

5.1 Problems and lessons learned from the first module GMX/KMX-1000

The first module prototypes built at each site (GMX/KMX-1000) were mainly intended to exercise the assembly procedures, to spot problems in the production of some of the components and to determine possible weaknesses in the module design. They provided an invaluable experience in terms of the identification and understanding of fundamental issues inherently bounded to both a first hybrid batch production and to a first module assembly. Important lessons were learned and solutions to the problems found were adopted for subsequent assemblies. The main problems found and how they were corrected (if applicable) are described below.

- *Metallization problems.*

  In some cases, a poor metallization was found in some bonding-pads of the hybrid (see Fig. 28), making the wire-bonding operations difficult. An improved metallization process and stricter quality assurance tests were requested to the flex-circuit manufacturer company. No more problems of this kind have been detected (as of today) in subsequent hybrid batches.

- *Wire-bonding overlap.*

  In the first version of the KEK hybrid, a specific pad layout was at the origin of a wire-bonding overlap in the data-token lines (between chips) and in some ground bonds (from chip to hybrid), increasing the probabilities of shorts due to touching cross-bonds. The bonding pad layout was modified in the second hybrid version, solving the overlap problems (see Fig. 29).

Assembly site	Module id	Sensor			Hybrid		Comments
		wafer	serie	type	serial	version	
Geneva	GMX-1000	W50	S2	FZ1	GHX-1002	1	• Irradiation "half-module"
					GHX-1003	1	• Manual assembly of SMDs
Geneva	GMX-1001	W17 (t)	S1	FZ1	GHX-1004	1	• Manual assembly of SMDs
					GHX-1005	1	
		W18 (b)	S1	FZ1	GHX-1006	1	
					GHX-1007	1	
Geneva	GMX-2002	W51 (t)	S2	FZ1 p-stop	KHX-2007	2	
					KHX-2008	2	
		W69 (b)	S2	FZ1 p-stop	KHX-2009	2	
					KHX-2010	2	
Geneva	GMX-2004	W63 (t)	S2	FZ1 p-stop	KHX-2015	2	
					KHX-2016	2	
		W64 (b)	S2	FZ1 p-stop	KHX-2017	2	
					KHX-2018	2	
Geneva	GMX-2006	W265 (t)	S3	FZ1 p-stop	KHX-2011	2	
					KHX-2012	2	
		W287 (b)	S3	FZ1 p-stop	KHX-2013	2	
					KHX-2014	2	
Geneva	GMX-2007	W25 (t)	X3	FZ1 p-stop	KHX-2019	2	• Electrical coupling between HV and V_{dd}
					KHX-2020	2	
		W267 (b)	S3	FZ1 p-stop	KHX-2021	2	
					KHX-2022	2	
Geneva	GMX-2008	W302 (t)	S3	FZ1 p-stop	KHX-2028	2	
					KHX-2029	2	
		W306 (b)	S3	FZ1 p-stop	KHX-2030	2	
					KHX-2031	2	

Table 9. Double-sided module prototypes built by the University of Geneva.

- *Adhesives excess.*

  When gluing the aluminium-nitride facings to the baseboard there was an overflow of adhesive into the facings vacuum chucks due to an excess amount of glue. The glue pattern under the facings was modified to avoid such problem.

Assembly site	Module id	Sensor			Hybrid		Comments
		wafer	serie	type	serial	version	
KEK	KMX-1000	W23	S1	FZ1 p-stop	KHX-1001	1	Long strip test module
KEK	KMX-1001	W32 (t)	S1	FZ1 p-stop	KHX-1004	1	
					KHX-1005	1	
		W33 (b)	S1	FZ1 p-stop	KHX-1006	1	
					KHX-1007	1	
KEK	KMX-2002	W42 (t)	S1	FZ1 p-stop	KHX-2002	2	
					KHX-2003	2	
		W44 (b)	X3	FZ1 p-stop	KHX-2005	2	
					KHX-2006	2	
KEK	KMX-2003	W273 (t)	S3	FZ1 p-stop	KHX-2001	2	• KHX-2001: two dead chips
					KHX-2004	2	• KHX-2004: two dead chips
		W271 (b)	S3	FZ1 p-stop	KHX-2038	2	
					KHX-2039	2	• KHX-2039: one dead chip

Table 10. Double-sided module prototypes built by KEK.

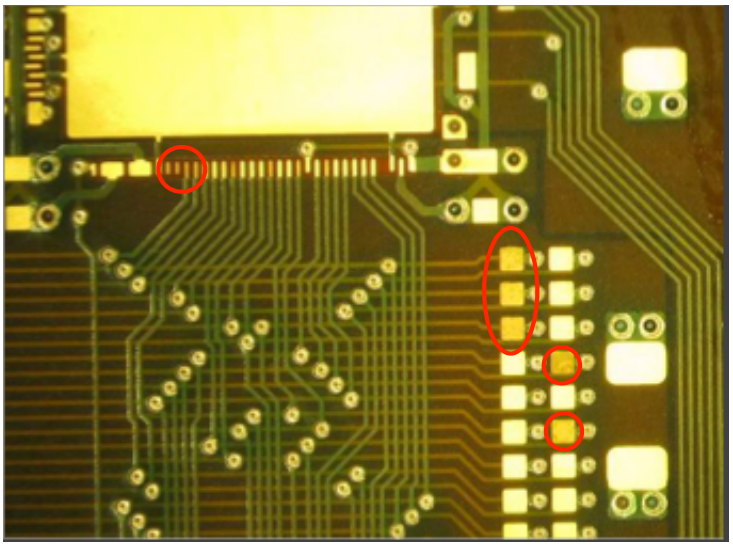


Figure 28. Metallization problems in some of the hybrid bonding-pads.

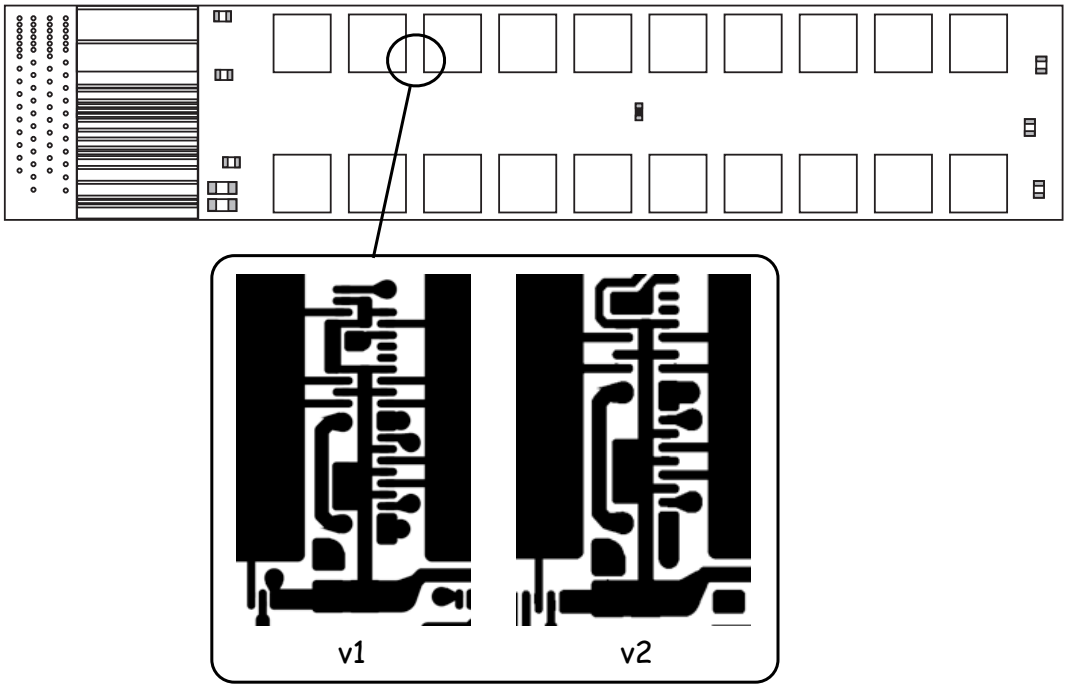


Figure 29. Top trace layer of the flex circuit (L1) for KEK hybrid versions 1 and 2.

- *High-voltage back-plane contact.*

  The tongue used for the sensor high-voltage bias was not really integrated into the original module design. Due to time constraints, the first HV-tongue was manually machined and this was at the origin of some difficulties while positioning it with a specific alignment jig. Furthermore, the electrical contact to the detector back-plane was made non-optimally with a conductive epoxy, and this was suspected to be the cause of very low currents (below 40 nA) while being monitored at low temperature.

  In the following modules, the HV-tongue was precisely shaped with an automatic machining process, with a main kapton-core and copper-nickel-gold (CuNiAu) sheets on its both ends. The electrical connection to the sensor back-plane was improved by using four wire-bonds.

- *High-voltage breakdown.*

  While measuring the IV-characteristics of the sensor of the GMX-1000 module at room temperature, high-voltage discharges were observed at around 300 V. No breakdowns appeared while re-measuring with nitrogen flushed inside the test-box containing the micro-probe needles. The low breakdown voltage was due to an intermediate floating pin between the HV and HV-GND pins in the miniature Samtec 0.8 mm pitch connector located at the far-end of the flex-circuit pigtail (see Fig. 30). Since the pin diameter is 0.3 mm, two consecutive pins are separated by 0.5 mm in a bare connector, and down to $\sim$ 0.3 mm if considering the soldering joints. Since the dielectric strength of humid air is $\sim$ 1 kV/mm, the presence of the extra floating pin close to the HV-pin would explain the breakdown observed. That pin was of course removed while assembling the following hybrid connectors, to increase the distance of the HV-pin to the next pin. No further low-voltage breakdowns have been observed, even without dry air.

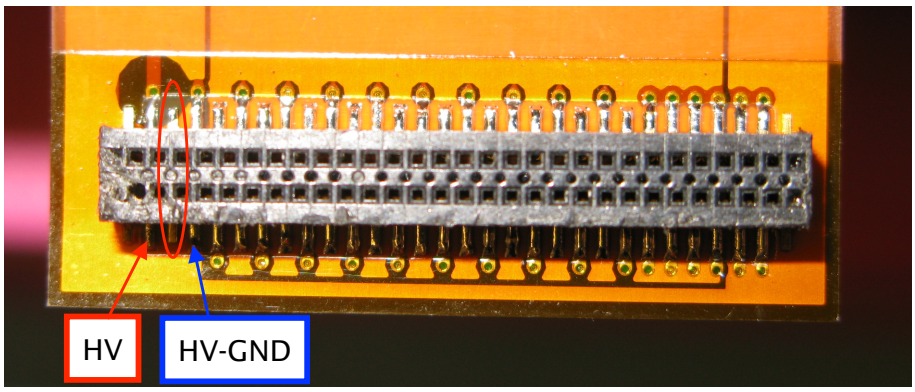


Figure 30. Close-view of the miniature Samtec 0.8 mm pitch connector (model CLE-130-01-G-DV) at the end of the flex-circuit pigtail. The left-most pin is the high-voltage pin. The circle indicates a floating pin between the HV and the HV-GND pins that was not removed while assembling the hybrid. The presence of that conducting pin is suspected to be at the origin of very low (300 V) voltage breakdowns observed in the GMX-1000 module. See text for further details.

5.2 Assembly jigs

A set of jigs has been developed to assemble the silicon module prototypes as presented in this note. Since tight mechanical tolerances were not a major requirement for these prototypes but proving the double-sided module concept in terms mainly of electrical performance, the jigs have been produced following a design that is simple and low cost cost. The different jigs used for the module assembly are shown in Figs. 31-34 and described below.

- The *baseboard assembly plate* (Fig. 31) consists of an aluminium plate with two linear vacuum grooves, four alignment plungers and four guiding pins. The plate is used to position and glue one side of the TPG baseboard to two AlN facings. Two additional identical vacuum chucks will put in place the two remaining facings on top of the baseboard.

- The *detectors' vacuum chucks* (Fig. 32a and b) are used to hold with vacuum the sensors while assembling them to the TPG baseboard. Each chuck consists in a teflon plate bolted on top of an aluminium plate. In both cases, a squared vacuum groove is centered in the teflon plate, and three alignment pins are used to place the detector with respect to its cutting edges. Six holes, three on each side with respect to chuck center, are used to hold plungers to align the baseboard and facings to the sensor. One of the chucks (Fig. 32a) has two additional vacuum channels to fix the facings while assembling one of the module sides. Lastly, two alignment pins are used to place one chuck on top of the other while sandwiching the set of silicon detectors, facings and baseboard. A different chuck is used to assemble the high-voltage tongue to each sensor (Fig. 32c).

- The hybrids are positioned with a special *placement jig* (Fig. 33a) which is longitudinally aligned with the sensor central axis. Once a first module side has been completed, it is transferred to the *hybrids assembly plate* (Fig. 33b), an aluminium plate with two large symmetric apertures that provide the required space for the front-end electronics. The *hybrids pressing jigs* (Fig. 33c) are used to press the hybrids against the facings while glue-curing.

- After assembly, the module is stored in a *multi-purpose holding box* (Fig. 34). The box is also used as bonding jig, and thus it remains a very convenient container to store and transport the module before, during and after bonding operations.

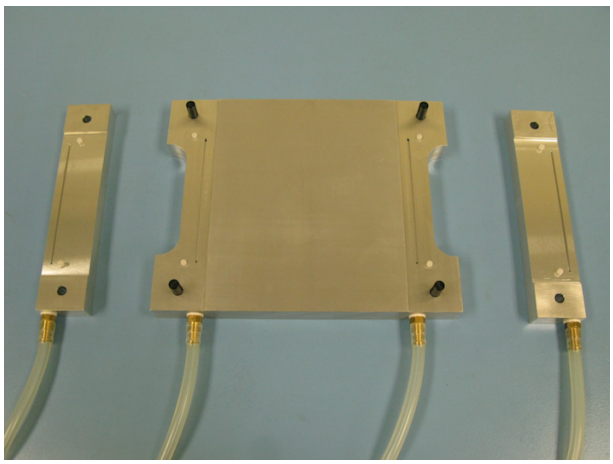
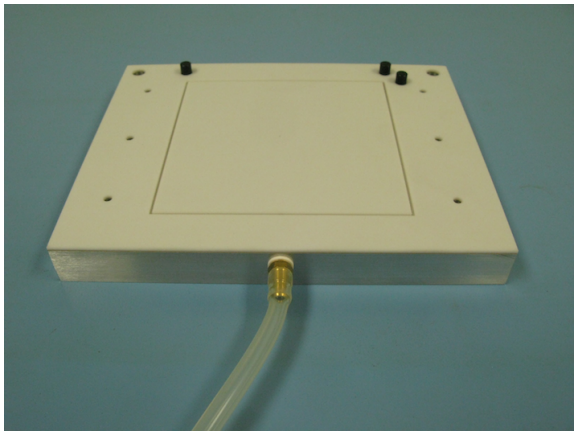
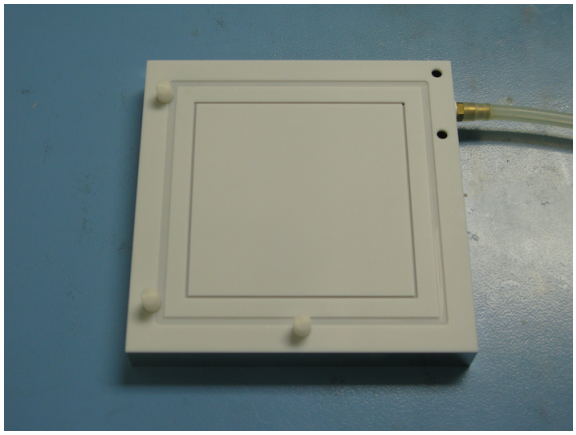


Figure 31. Baseboard assembly plate and facings vacuum chucks.

(a)

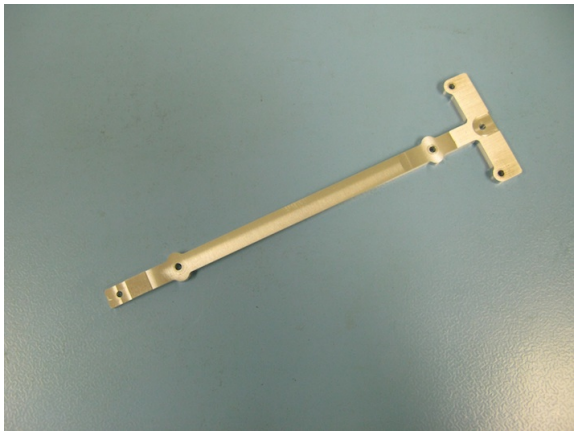


(b)

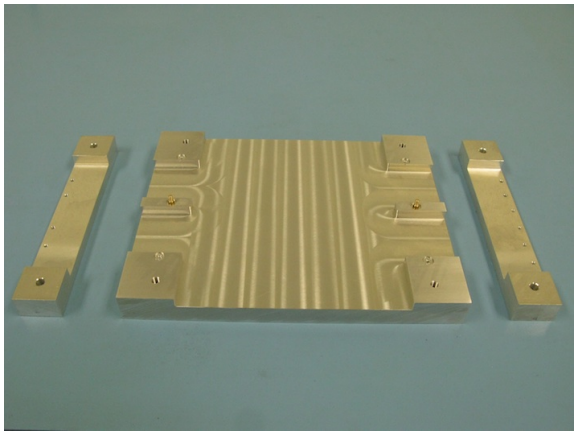


(c)

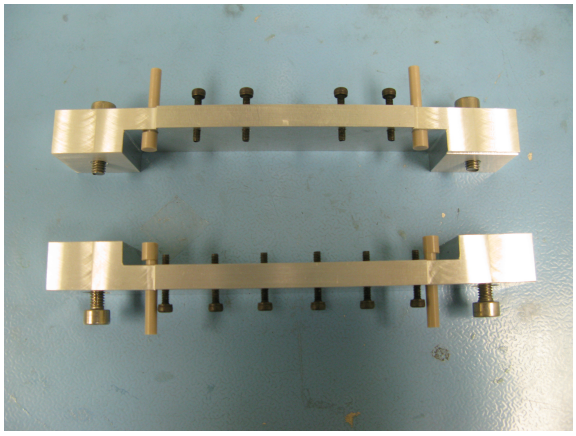
Figure 32. Vacuum chucks for detector (top) and high-voltage tongue assembly (bottom).



(a)



(b)



(c)

Figure 33. (a) Hybrids placement jig, (b) assembly plate and (c) hybrids pressing jigs.

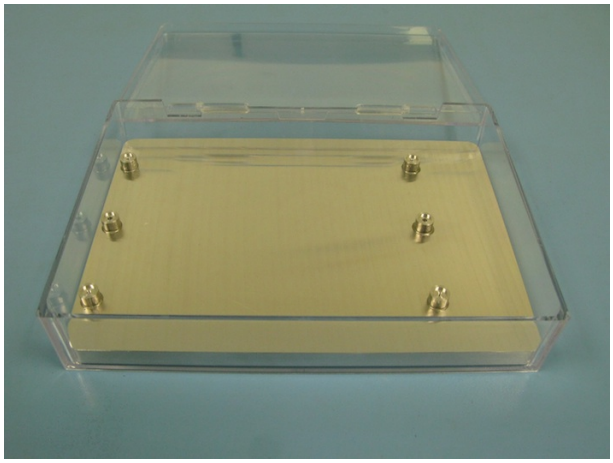
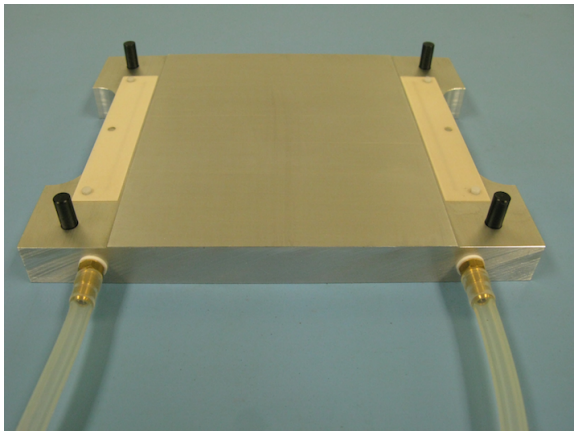
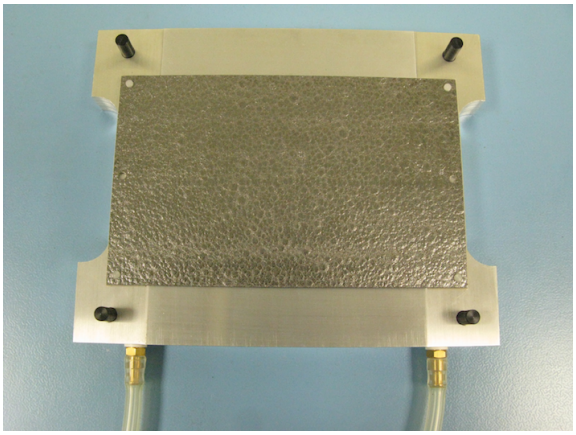


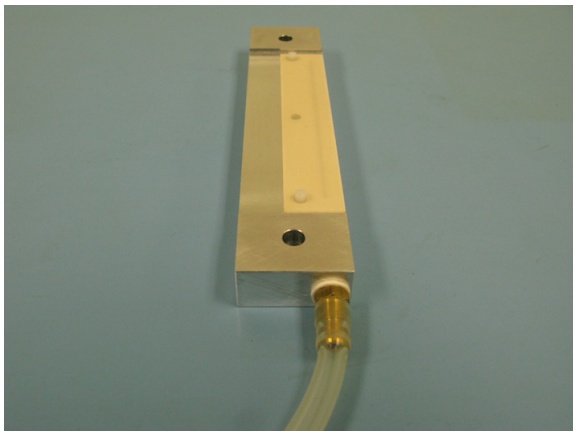
Figure 34. Transport/storage/bonding box.



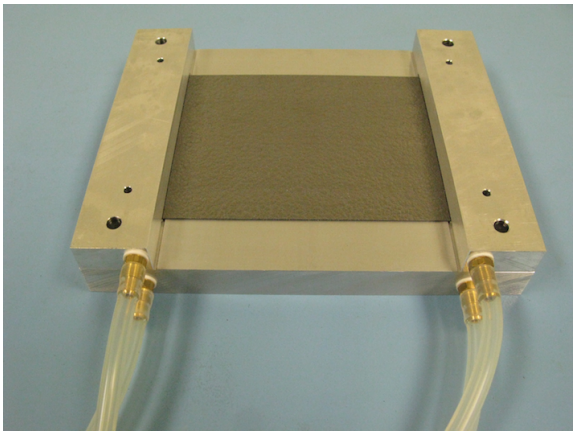
(a)



(b)



(c)



(d)

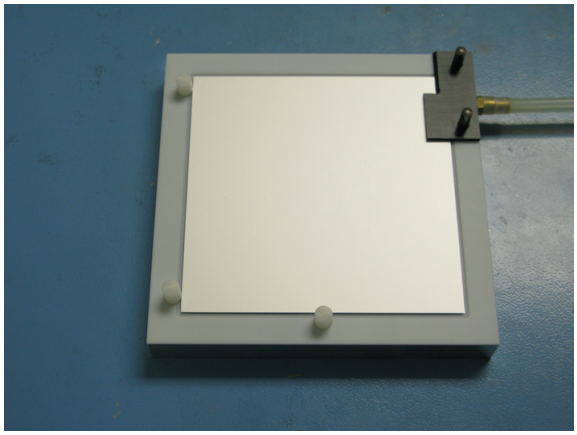
Figure 35. Baseboard and AlN facings assembly sequence.

5.3 Assembly procedure

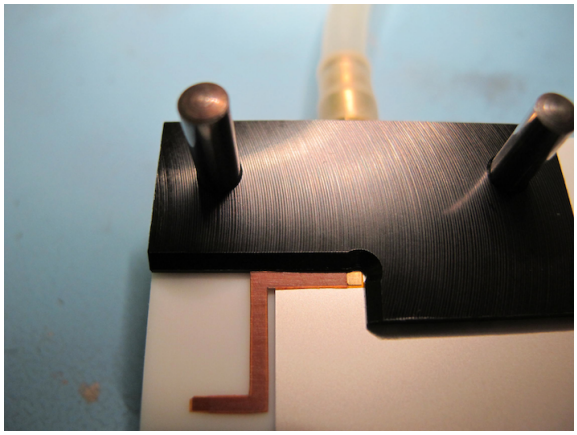
The different stages of the assembly sequence are described below.

1.- Baseboard and facings assembly

A rectangular teflon piece with a single linear vacuum channel is fixed on top of each far-end of the baseboard assembly plate (Fig. 35a). The four alignment pins located in the corners of the base-plate are used to drive auxiliary jigs at different stages of the module assembly. Two AlN facings are positioned to the plungers over the teflon pieces and vacuum is applied to avoid displacements. Glue (Araldite 2011) is dispensed to the facings. The TPG baseboard is laid on top of the facings by means of the four guiding pins (Fig. 35b). Two other AlN facings are held with vacuum on two independent vacuum chucks (Fig. 35c). Each chuck contains the same teflon structure as in the baseboard assembly plate so that all four module facings are identical. The vacuum chucks are inserted into the alignment pins of the base-plate (Fig. 35d). Vacuum is applied to press the facings to the baseboard (curing time is typically 24 hours).



(a)



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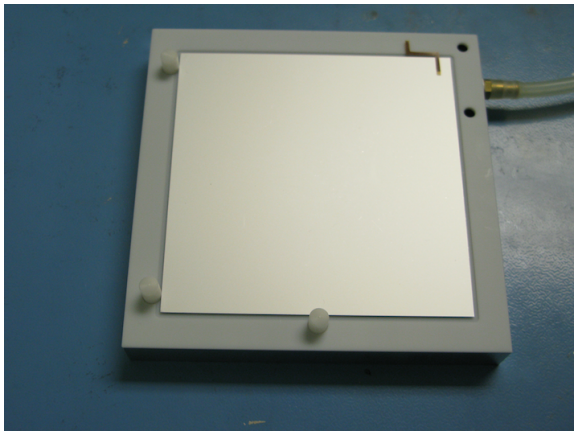
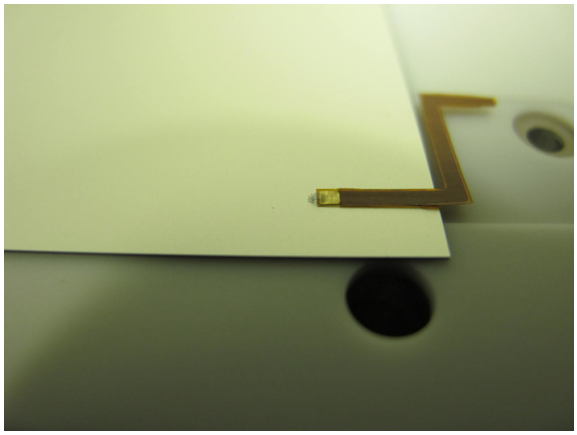


(c)



(d)

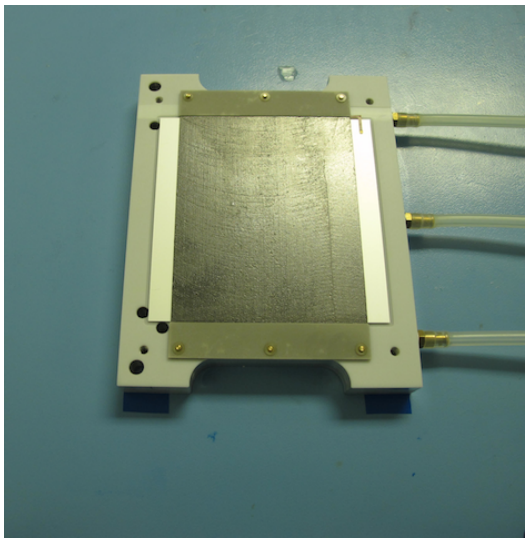
Figure 36. High-voltage tongue assembly.

2.- Assembly of high-voltage tongue to sensors

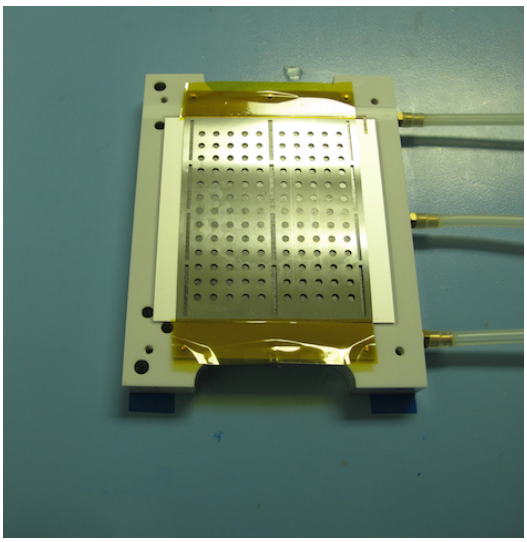
A silicon detector is placed (back-plane facing up) on a detector vacuum chuck by aligning two of the sensor edges to three alignment pins. Vacuum is applied to hold the detector and the high-voltage tongue assembly jig is inserted into the chuck by means of two guiding pins (Fig. 36a). The *s-shaped* tongue is positioned (Fig. 36b) and glued with Araldite-2011 (electrically non-conductive). After removal of the assembly jig, the electrical connection to the sensor back-plane is made with four low-height wire-bonds (Fig. 36d).

3.- Detector assembly

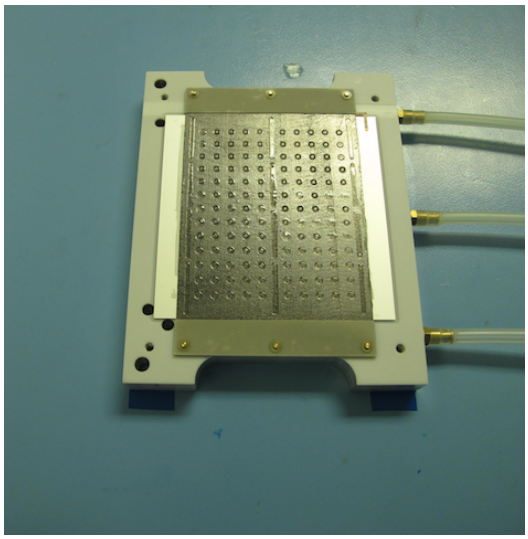
Fig. 37a shows a sensor already glued to one side of the TPG baseboard. The assembly of the other side follows exactly the same procedure. A 100 μm-thick mask with a glue distribution pattern is placed over the baseboard between the facings and fixed with kapton tapes before spreading the glue. The mask pattern is shown in Fig. 38. The pattern provides a good glue coverage for most of the sensor area while avoiding the edges and ensures the required fixation of the sensor (and in particular under the bond-pads) that avoids difficulties during wire-bonding operations. The glue mask has been used for all modules assembled in KEK and for the last module built by the University of Geneva, GMX-2008. The remaining six modules assembled in Geneva were fabricated without the mask and therefore without an accurate control of the total glue dispensed.



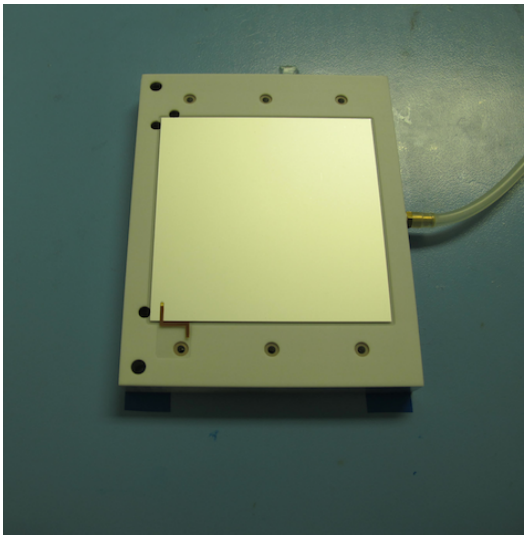
(a)



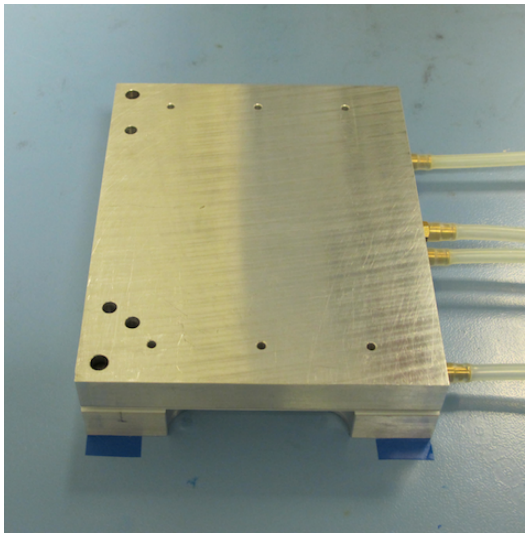
(b)



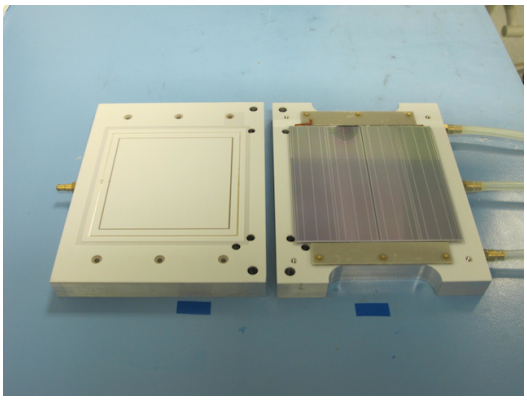
(c)



(d)



(e)



(f)

Figure 37. Detectors to baseboard assembly.

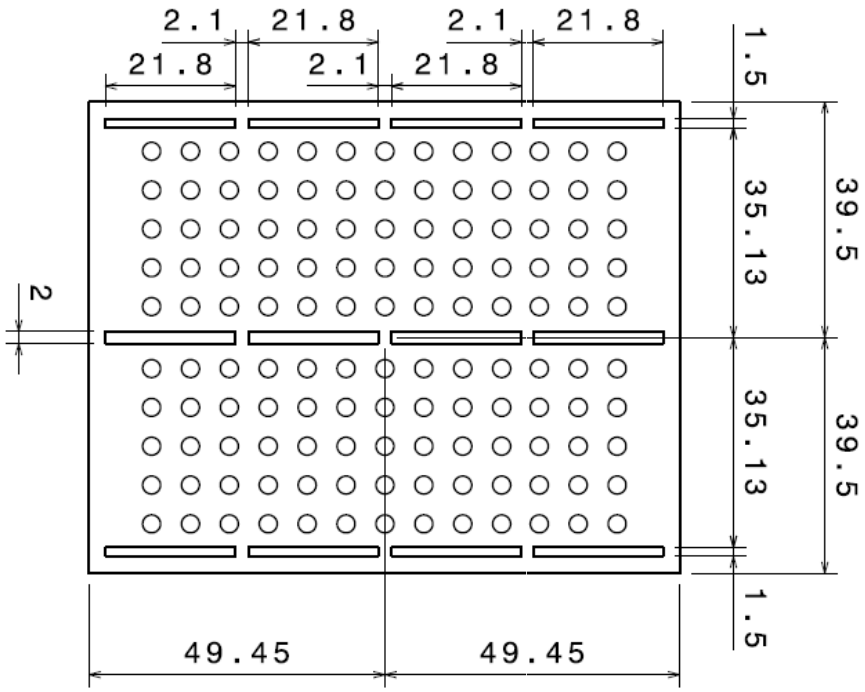


Figure 38. Mask pattern for glue dispensing over the TPG baseboard (sensor-to-baseboard gluing). The quoted dimensions are before glue compression (typically the glue area is extended by a factor ~1.6). The dot diameter is 3 mm.

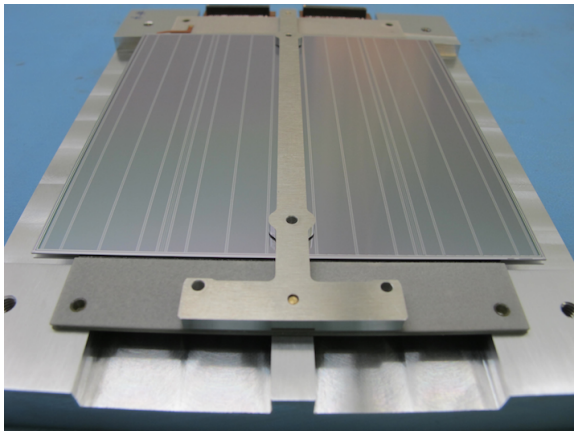
Fig.37c shows the glue after being applied to the pattern. The second detector, with the HV-tongue already bonded to the back-plane, is transferred to the baseboard (Fig. 37e) and pressed against it. After curing during 24 hours at room temperature, the set is ready (Fig. 37f) and IV-characteristics are measured for both sensors.

4.- Hybrid assembly

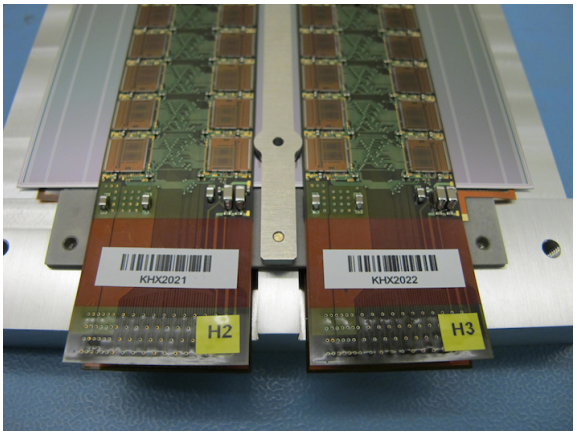
The complete set of baseboard and sensors is transferred to the hybrid assembly plate (see Fig. 33b). The T-shaped hybrid placement jig is positioned on top of one sensor by means of two guiding pins (Fig. 39a). Glue is dispensed to the the carbon-carbon feet of the bridge the main flex sits on and two hybrids are aligned with respect to their edges to the placement jig (Fig. 39b and 39c). The hybrid pressing jigs are put in place so that to press both ends of the hybrids to the facings (Figs. 39d and 39e). After glue curing, the set is turned upside-down (see the grooves in the assembly plate Fig. 33b that provide the required space for the already glued hybrids) and the other two remaining hybrids are assembled the same way (Figs. 39f).

5.- Wire-bonding

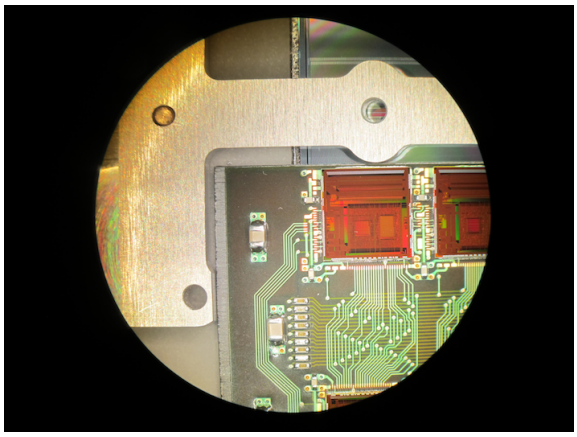
The module is transfered to the *multi-purpose holding box* for bonding. The chip-to-hybrid and the chip-to-sensor wire-bonds are made using with standard 25 μm Al-Si(1%) wire. Due to the presence of the CC-bridge underneath the hybrid flex, the the wire-bonds to the sensor may reach several milimeters-height (see Fig. 40). Each of the 80 ABCN25 chips of the module has a unique address. Appendix B describes the convention that has been followed for all modules.



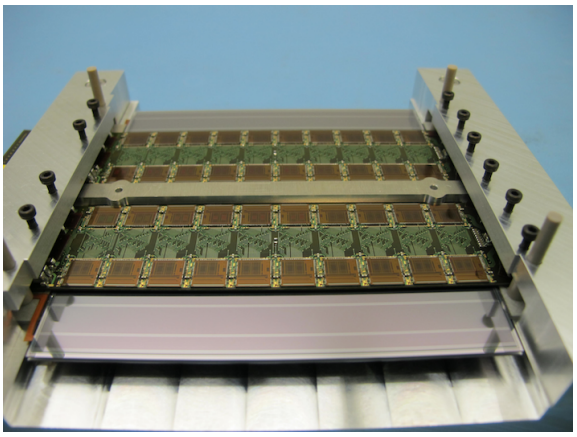
(a)



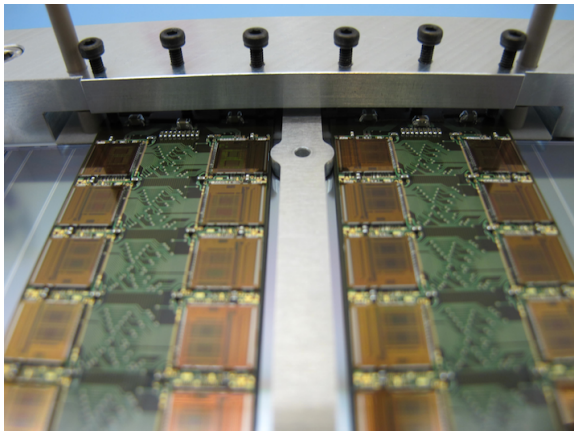
(b)



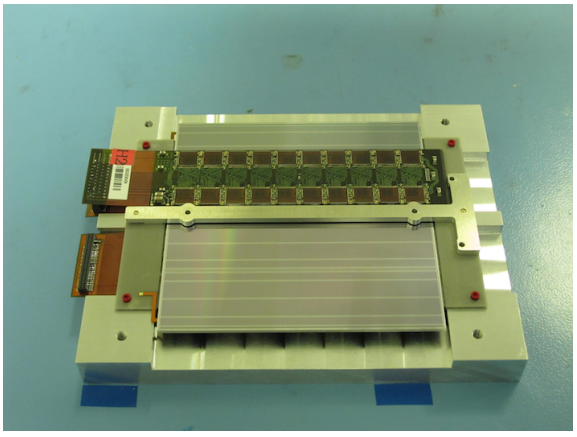
(c)



(d)



(e)



(f)

Figure 39. Hybrids assembly sequence.

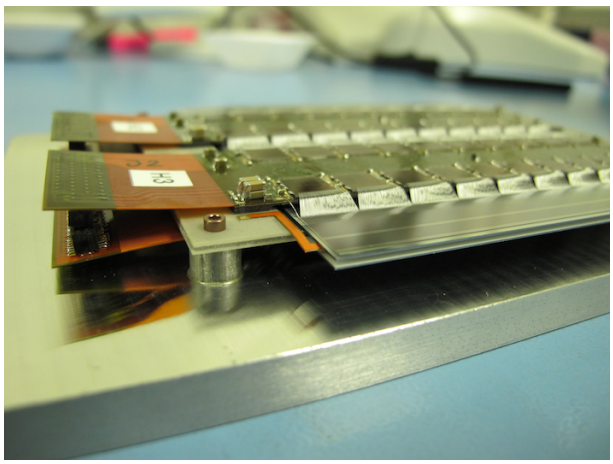


Figure 40. Detail of wire-bonds from ASICs to sensor.

6 Optimized design and improved material budget

Material improvements can be considered in the short-term by reducing the thickness of both the TPG baseboard and the CC-bridge, if the thermal and electrical performance of the module is not compromised. Further material reductions are expected in the near future with the next generation of ABCN chips (ABCN-13), produced in 130 nm with 256 channels per ASIC. In that case, the hybrid would have a single column of ten chips, allowing to read two segments of 1280 strips each. The width of the hybrid will be decreased significantly and a design with a single connector serving two hybrids is considered possible. With these realistic asumptions, a single 15 mm-wide hybrid (without connector), including SMDs and 10 ABCN-13 ASICs would make ~0.17% X_0. A double-sided silicon module, with four hybrids, a single connector for two hybrids, a 300 μm-thick CC-bridge and TPG would represent ~1.7% X_0 with an estimated weight of ~40 g, improving by ~30% the total radiation length and ~32% the estimated weight with respect to the current "as-built" module prototype presented in this note.

7 Summary

A double-sided silicon strip module is proposed as the detecting unit for the short-strip region of the upgraded ATLAS inner tracker. The module design has been presented in detail. The module consists in two silicon micro-strip sensors glued to a central TPG baseboard that provides the required mechanical stability while ensuring an optimal thermal path to dissipate the heat generated by the readout electronics. This module design present clear advantages over other possible approaches: repairability and repleaceability operations possible up to the latest assembly stage, accurate space-point formation for pattern recognition, complete hermeticity of the tracker in both $R\phi$ and Z, optimized large-scale production including QA in a world-wide collaboration, ease of testing in heterogenous environments (laboratories, irradiation areas, testbeam areas).

The current "as-built" prototypes represents a material budget of 2.44% X_0. A large fraction of the material budget is driven by the sensors and the hybrid. The CC-bridge represents 22% of the hybrid material budget. Significant material improvements are expected with the future ABCN13 ASICs and further optimizations in the hybrid design are underway. The thermal FEA simulations show excellent results in terms of sensor temperature uniformity (-13.5 °C within 1 °C assuming a for a coolant temper-

ature of -30 °C with an Heat Transfer Coefficient of 4000W/m^2 K) and large safety margins with respect to mechanical stresses. For a large range of thermal grease conductivities simulated, the module design shows a safety factor of at least a factor of two with respect to the thermal runaway point.

Both the University of Geneva and KEK have built first module prototypes with the aim of validating the module design mainly in terms of electrical performance. The first modules assembled were used to exercice the assembly procedures and to address several issues that appeared with the first version of the KEK hybrid. Most of the problems were solved with a second version of the hybrid. The assembly sequence described in detail in this note shows that double-sided silicon modules are reasonable small objects that can be assembled without difficulty in most institutes.

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Appendices

A Hybrid circuit diagram

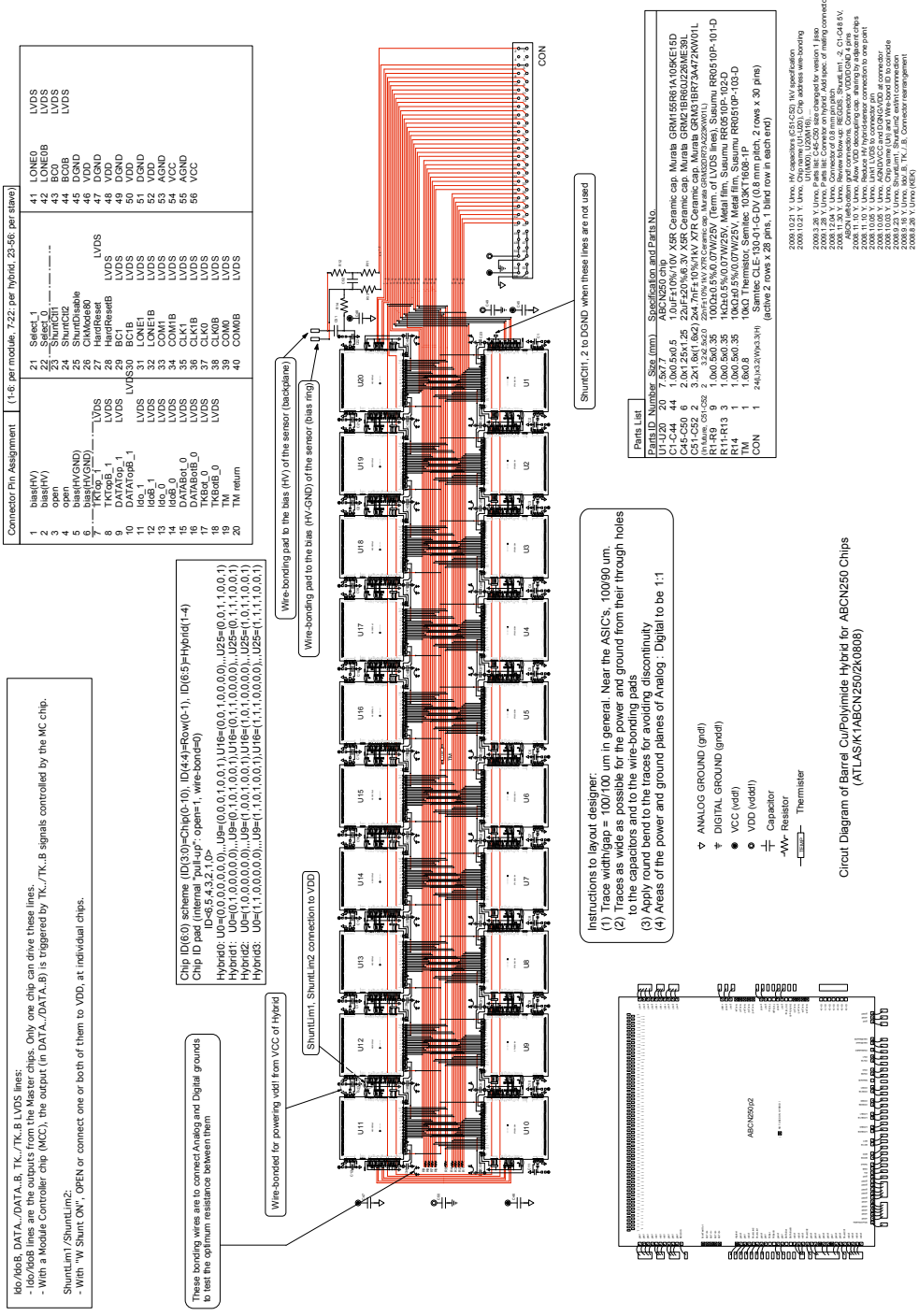

Figure 41. KEK hybrid circuit diagram.

B Numbering conventions and chip addreses

The double-sided silicon module has four hybrids arranged in two sides. The convention chosen to number hybrids within the module is shown in Fig. 42. Hybrids 0 and 1 are on the same side (*e.g.* top-side). Hybrid 2/3 is the lower (bottom-side) with respect to hybrid 0/1.

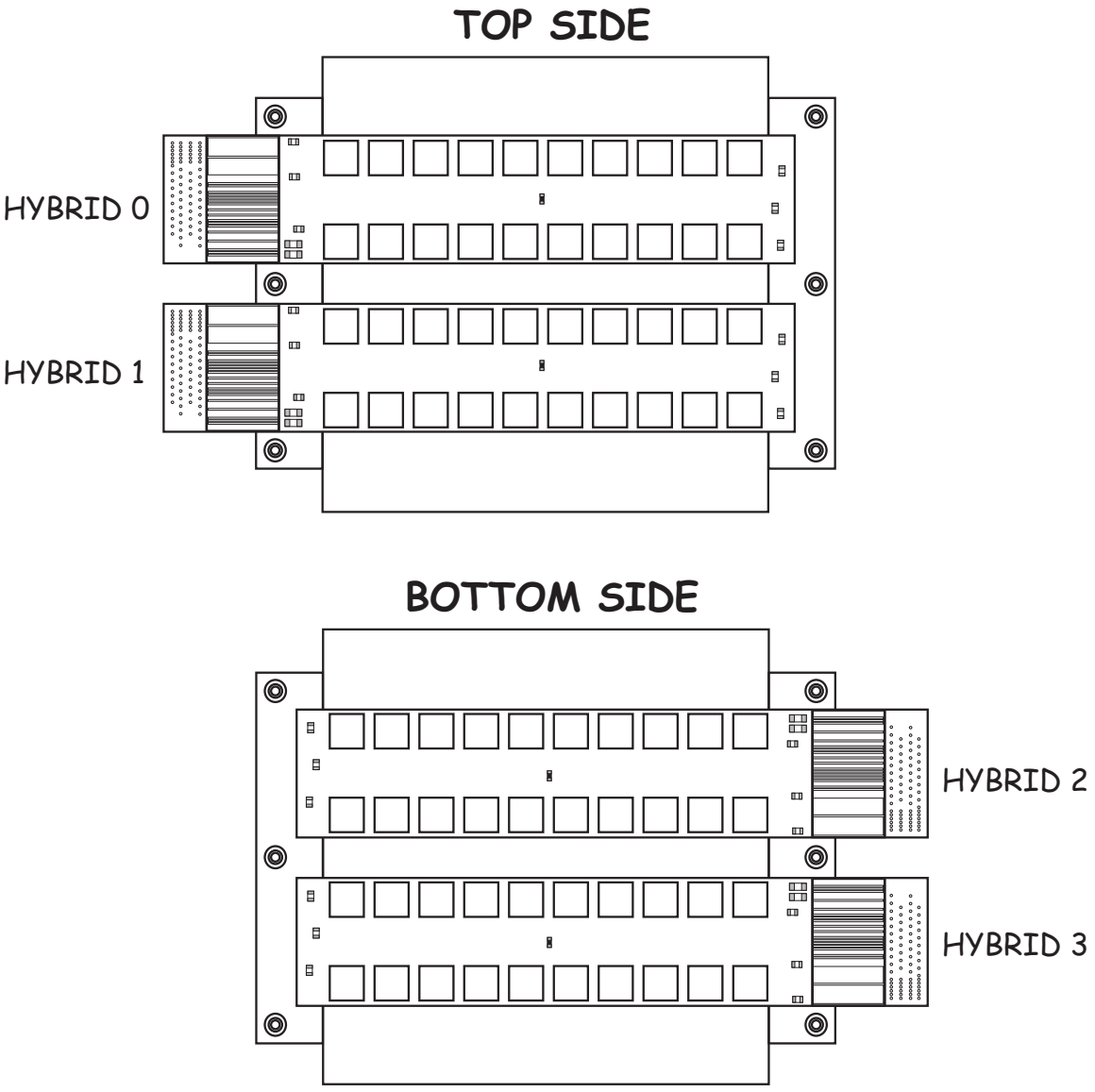

Figure 42. Hybrid numbering within module.

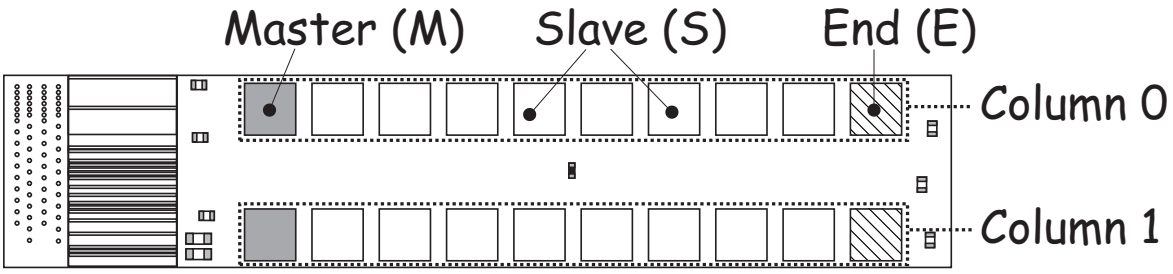

Figure 43. Column numbering within hybrid.

Each hybrid has 20 ASICs arranged in two columns of ten. Fig. 43 shows how the two columns are numbered within a hybrid. With the orientation shown, the left/right-most chips (closest/farest to the connector side) are the *Master*/*End* chips, while the others are *Slave* chips. In this case, the readout mode is *stand-alone* or "legacy" mode, in which the Master chip issues a preamble and the End chip a trailer to indicate respectively the start and end of the data-pattern.

The ABCN-25 FE has seven inputs [id6 . . . id0] that can be wire-bonded to set a given logic level. The set of these levels defines the chip address. Tables 11 and 12 show the chip addresses for all 80 chips within a single module, where:

*	means bonded
	means "open" (no wire-bond)

Note that with this address scheme:

- [id0 . . . id3] are identical for a given chip independently of hybrid and column numbers (the input pattern just depends on the position of the chip within the column)
- id4 is the column number
- [id6, id5] is the hybrid number

Hybrid 0																	
Column 0									Column 1								
Chip name	Bond pads							Add.	Chip name	Bond pads							Add.
	id6	id5	id4	id3	id2	id1	id0			id6	id5	id4	id3	id2	id1	id0	
M0	*	*	*	*	*	*	*	0	M16	*	*		*	*	*	*	16
S1	*	*	*	*	*	*		1	S17	*	*		*	*	*		17
S2	*	*	*	*	*		*	2	S18	*	*		*	*		*	18
S3	*	*	*	*	*			3	S19	*	*		*	*			19
S4	*	*	*	*		*	*	4	S20	*	*		*		*	*	20
S5	*	*	*	*		*		5	S21	*	*		*		*		21
S6	*	*	*	*			*	6	S22	*	*		*			*	22
S7	*	*	*	*				7	S23	*	*		*				23
S8	*	*	*		*	*	*	8	S24	*	*			*	*	*	24
E9	*	*	*		*	*		9	E25	*	*			*	*		25
Hybrid 1																	
Column 0									Column 1								
Chip name	Bond pads							Add.	Chip name	Bond pads							Add.
	id6	id5	id4	id3	id2	id1	id0			id6	id5	id4	id3	id2	id1	id0	
M32	*		*	*	*	*	*	32	M48	*			*	*	*	*	48
S33	*		*	*	*	*		33	S49	*			*	*	*		49
S34	*		*	*	*		*	34	S50	*			*	*		*	50
S35	*		*	*	*			35	S51	*			*	*			51
S36	*		*	*		*	*	36	S52	*			*		*	*	52
S37	*		*	*		*		37	S53	*			*		*		53
S38	*		*	*			*	38	S54	*			*			*	54
S39	*		*	*				39	S55	*			*				55
S40	*		*		*	*	*	40	S56	*				*	*	*	56
E41	*		*		*	*		41	E57	*				*	*		57

Table 11. Chip addresses for hybrids 0 and 1.

Hybrid 2																	
Column 0									Column 1								
Chip name	Bond pads							Add.	Chip name	Bond pads							Add.
	id6	id5	id4	id3	id2	id1	id0			id6	id5	id4	id3	id2	id1	id0	
M64		*	*	*	*	*	*	64	M80		*		*	*	*	*	80
S65		*	*	*	*	*		65	S81		*		*	*	*		81
S66		*	*	*	*		*	66	S82		*		*	*		*	82
S67		*	*	*	*			67	S83		*		*	*			83
S68		*	*	*		*	*	68	S84		*		*		*	*	84
S69		*	*	*		*		69	S85		*		*		*		85
S70		*	*	*			*	70	S86		*		*			*	86
S71		*	*	*				71	S87		*		*				87
S72		*	*		*	*	*	72	S88		*			*	*	*	88
E73		*	*		*	*		73	E89		*			*	*		89
Hybrid 3																	
Column 0									Column 1								
Chip name	Bond pads							Add.	Chip name	Bond pads							Add.
	id6	id5	id4	id3	id2	id1	id0			id6	id5	id4	id3	id2	id1	id0	
M96			*	*	*	*	*	96	M112				*	*	*	*	112
S97			*	*	*	*		97	S113				*	*	*		113
S98			*	*	*		*	98	S114				*	*		*	114
S99			*	*	*			99	S115				*	*			115
S100			*	*		*	*	100	S116				*		*	*	116
S101			*	*		*		101	S117				*		*		117
S102			*	*			*	102	S118				*			*	118
S103			*	*				103	S119				*				119
S104			*		*	*	*	104	S120					*	*	*	120
E105			*		*	*		105	E121					*	*		121

Table 12. Chip addresses for hybrids 2 and 3.

Material	Symbol	Z	A	Density	Radiation length	
				(g/cm^3)	(g/cm^2)	(cm)
Hydrogen	H	1	1.008	8.2×10^{-5}	58.701	717614
Beryllium	Be	4	9.013	1.846	64.128	34.739
Boron	B	5	10.810	2.466	52.682	21.363
Carbon	C	6	12.011	2.266	42.698	18.843
Nitrogen	N	7	14.007	1.165×10^{-3}	37.988	32524
Oxygen	O	8	15.999	1.332×10^{-3}	34.238	27066
Aluminum	Al	13	26.981	2.698	24.011	8.897
Silicon	Si	14	28.086	2.329	21.824	9.370
Titanium	Ti	22	47.900	4.540	16.175	3.588
Nickel	Ni	28	58.700	8.902	12.680	1.424
Copper	Cu	29	63.546	8.960	12.863	1.440
Silver	Ag	47	107.868	10.500	8.972	0.854
Tin	Sn	50	118.690	7.310	8.817	1.210
Barium	Ba	56	137.340	3.500	8.307	2.312
Gold	Au	79	196.966	19.281	6.461	0.335
Lead	Pb	82	207.200	11.343	6.370	0.562

Table 13. Density and radiation length of some elements. Z is the atomic number, A is the atomic weight.

C Radiation length calculation and material budget

The radiation length X_0 of a compound material is calculated as:

$$\frac{1}{X_0} = \sum_i \frac{w_i}{X_i} \tag{1}$$

where w_i and X_i are respectively the mass fraction (or relative weight) and the radiation length of the i^{th} element in the compound. In the case of compounds defined by a chemical composition, the mass fraction w_i is calculated as:

$$w_i = \frac{n_i A_i}{\sum_i n_i A_i}$$

where n_i and A_i are respectively the number of moles and the atomic weight of the corresponding constituent. Table 13 lists the density and radiation length of some elements. The radiation length calculated using eq. 1 is given in g/cm^2. In order to obtain the corresponding X_0 in length-units, the density of the compound is required. For materials with a crystalline or semi-crystalline structure (*e.g.* ceramics, oxides, some polymers, etc.), the density depends in the final arrangement of the atoms in the lattice (and the air spaces between atoms). In that case, the density is taken as an *ansatz* from the manufacturer technical data-sheet (see table 14). For the rest of materials (see table 15), the density ρ of the compound is calculated to a good approximation as:

$$\frac{1}{\rho} = \sum_i \frac{w_i}{\rho_i} \tag{2}$$

Element	n	w	$w/(\rho \cdot X_0)$ $(g/cm^2)^{-1}$	ρ (g/cm^3)	X_0 (cm)
Aluminum Nitride AlN					
Al	1	0.658	0.027416		
N	1	0.342	0.008996		
		1.000	0.036412	3.280	8.373
Boron Nitride BN					
B	1	0.436	0.008268		
N	1	0.564	0.014858		
		1.000	0.023126	3.450	12.534
Aluminum Oxide Al_2O_3					
Al	2	0.529	0.022042		
O	3	0.471	0.013749		
		1.000	0.035791	3.970	7.038
Barium Titanate $BaTiO_3$					
Ba	1	0.589	0.070880		
Ti	1	0.205	0.012697		
O	3	0.206	0.006011		
		1.000	0.089588	6.020	1.854
Polyether ether ketone $C_{19}H_{12}O_3$					
C	19	0.792	0.018539		
H	12	0.042	0.000715		
O	3	0.166	0.004863		
		1.000	0.024116	1.320	31.414

Table 14. Radiation length of compounds (crystalline structure). For each component, n is the number of moles and w is the mass fraction. The radiation length in cm is obtained from the quoted density and the calculated radiation length in g/cm^2.

where ρ_i is the density of the i^{th} element in the compound.

Table 16 lists the density and radiation length of all the compounds used in the assembly of the modules. In the cases in which the exact composition is not known, the quoted values are those obtained directly from the manufacturer technical data-sheets. In the other cases, the corresponding values have been obtained as explained above and as shown in tables 14 and 15. A short-name descriptor is given to all materials to ease cross-referencing in subsequent calculations.

Element	w	$w/(\rho \cdot X_0)$ $(g/cm^2)^{-1}$	ρ (g/cm^3)	X_0 (cm)
Conductive glue Epoxy(39%) Ag(61%)				
Epoxy†	0.390	0.010833	1.200	30.000
Ag	0.610	0.068003	10.500	0.854
	1.000	0.078837	2.610	4.859
Thermal glue Araldite(69%) BN(31%)				
Araldite	0.690	0.017604	1.170	33.500
BN	0.310	0.007169	3.450	12.533
	1.000	0.024773	1.471	27.433
Soldering paste Sn(63%) Pb(35%) Ag(2%)				
Sn	0.630	0.071451	7.285	1.210
Pb	0.350	0.054948	11.343	0.562
Ag	0.020	0.002230	10.500	0.854
	1.000	0.128629	8.386	0.927
Capacitor $BaTiO_3$(86%) Ni(8%) Sn(6%)				
$BaTiO_3$	0.860	0.077046	6.020	1.854
Ni	0.080	0.006309	8.907	1.424
Sn	0.060	0.006805	7.285	1.210
	1.000	0.090160	6.247	1.775
Thin film resistor Al_2O_3(92.7%) Ni(3.1%) Sn(2.4%) Epoxy(1.8%)				
Al_2O_3	0.927	0.033175	3.970	7.038
Ni	0.031	0.002445	8.907	1.424
Sn	0.024	0.002722	7.285	1.210
Epoxy†	0.018	0.000500	1.200	30.000
	1.000	0.038842	3.912	6.572
Wire-bond Al(99%) Si(1%)				
Al	0.990	0.041232	2.698	8.899
Si	0.001	0.000458	2.329	9.370
	1.000	0.041690	2.694	8.905

Table 15. Radiation length of compounds. For each component w is the mass fraction (relative weight). the density of the compound is calculated using eq. 2 (see text for details). † The values for *Epoxy* are given in table 16.

Compound material		Density	Radiation length	
short name	**comment**	(g/cm^3)	(g/cm^2)	(cm)
Epoxy	Polyepoxide	1.200	36.000	30.000
Araldite	Araldite 2011	1.170	39.195	33.500
Parylene		1.289	32.870	25.500
CC2D	carbon-carbon	1.900	41.420	21.800
Polymide		1.136	40.612	35.750
TPG	Thermal Pyrolytic Graphite	2.260	42.714	18.900
Conn	Samtec connector (Liquid Crystal Polymer)	1.550	38.750	25.000
Peek	Polyether ether ketone♠	1.320	41.466	31.414
CGlue	Conductive glue†	2.610	27.433	40.366
TGlue	Thermal glue†	1.471	40.366	27.433
SoldPaste	Soldering paste†	8.386	7.774	0.927
Capa	Capacitor†	6.247	11.091	1.775
SuRes	Thin film resistor†	3.912	25.745	6.572
Wirebond	Wire-bond†	2.694	23.987	8.905

Table 16. Density and radiation length of compounds. (♠ see table 14). († see table 15).

Reference		Hybrid version	Length (mm)	Width (mm)	Thickness (mm)	Number
Murata GRM155R61A105KE15D	C1-C44, C55	all	1.00	0.50	0.50	45
Murata GRM21BR60J226ME39L	C45-C50	all	2.00	1.25	1.25	6
Murata GRM31BR72J103KW01L	C51-C54	all	3.20	1.60	1.60	4
Susumu RR0510P-101-D	R1-R9	all	1.00	0.50	0.35	9
Susumu RR0510P-102-D	R11-R13	2	1.00	0.50	0.35	3
Kamaya RGC1/16C102DTP		3	1.60	0.80	0.45	
Susumu RR0510P-103-D	R14	all	1.00	0.50	0.35	1
Semitec 103KT1608-1P	TM	all	1.60	0.80	0.95	1

Table 17. SMD components of KEK hybrid.

Item	**Material**	**Num**	X_0 (g/cm^2)	**Density** (g/cm^3)	**Length** (mm)	**Width** (mm)	**Thickness** (mm)	**Area** (mm^2)	**Less area** (mm^2)	**Norm. factor**	X_0 (%)	**Mass** (g)
Gold flash	Au	1	6.46	19.281	136.000	28.000	0.3×10^{-3}	3808	1896	0.2009	0.0018	0.011
Nickel plating	Ni	1	12.68	8.907	136.000	28.000	0.005	3808	1896	0.2009	0.0071	0.085
Top resisitve layer	Polymide	1	40.61	1.136	136.000	28.000	0.020	3808	2026	0.1873	0.0010	0.040
L1 copper button plating	Cu	1	12.86	8.933	136.000	28.000	0.020	3808	3667	0.0148	0.0021	0.025
L1 copper	Cu	1	12.86	8.933	136.000	28.000	0.012	3808	1896	0.2009	0.0167	0.205
Polymide	Polymide	1	40.61	1.136	136.000	28.000	0.025	3808	0	0.4003	0.0028	0.108
Adhesive layer	Polymide	1	40.61	1.136	136.000	28.000	0.025	3808	0	0.4003	0.0028	0.108
L2 copper	Cu	1	12.86	8.933	136.000	28.000	0.012	3808	2913	0.0941	0.0078	0.096
Polymide	Polymide	1	40.61	1.136	136.000	28.000	0.025	3808	0	0.4003	0.0028	0.108
L3 copper	Cu	1	12.86	8.933	136.000	28.000	0.012	3808	244	0.3746	0.0312	0.382
Adhesive layer	Polymide	1	40.61	1.136	136.000	28.000	0.025	3808	0	0.4003	0.0028	0.108
Polymide	Polymide	1	40.61	1.136	136.000	28.000	0.025	3808	0	0.4003	0.0028	0.108
L4 copper	Cu	1	12.86	8.933	136.000	28.000	0.012	3808	800	0.3162	0.0264	0.322
Adhesive layer	Polymide	1	40.61	1.136	136.000	28.000	0.033	3808	647	0.3322	0.0031	0.118
Polymide L4 cover	Polymide	1	40.61	1.136	136.000	28.000	12.7×10^{-3}	3808	647	0.3322	0.0012	0.046
L4 copper button plating	Cu	1	12.86	8.933	136.000	28.000	0.020	3808	3667	0.0148	0.0021	0.025
Nickel plating	Ni	1	12.68	8.933	136.000	28.000	0.005	3808	3667	0.0148	0.0005	0.006
Gold flash	Au	1	6.46	19.281	136.000	28.000	0.3×10^{-3}	3808	3667	0.0148	0.0001	0.001
SUB-TOTAL 1: hybrid + pigtail											0.1151	1.904
Pigtal connector housing	Conn	1	38.75	1.550	3.200	24.000	3.300	76.8	6	0.0075	0.0099	0.364
Connector female pins	Cu	26	12.86	8.933	0.300	3.500	0.200	1.1	0	0.0001	0.0040	0.049
Gold flash	Au	26	6.46	19.281	0.300	7.400	0.3×10^{-3}	2.2	0	0.0002	0.0001	0.3×10^{-3}
Nickel plating	Ni	26	12.68	8.907	0.300	7.400	0.005	2.2	0	0.0002	0.0002	0.003
Soldering paste	SoldPaste	26	7.77	8.386	1.000	0.400	0.120	0.4	0	4.2×10^{-5}	0.0014	0.010
SUB-TOTAL 2: connector											0.0155	0.427

Table 18. KEK hybrid (v3) material budget (see text for details).

Item	Material	Num	X_0 (g/cm^2)	Density (g/cm^3)	Length (mm)	Width (mm)	Thickness (mm)	Area (mm^2)	Less area (mm^2)	Norm. factor	X_0 (%)	Mass (g)
Parylene top	Parylene	1	32.870	1.289	112.000	28.000	0.010	3136.0	220	0.3065	0.0012	0.038
Parylene bottom	Parylene	1	32.870	1.289	112.000	28.000	0.010	3136.0	0	0.3296	0.0013	0.040
CC-bridge	CC2D	1	41.420	1.900	112.000	28.000	0.400	3136.0	0	0.3296	0.0605	2.383
CC-step	CC2D	2	41.420	1.900	5.500	28.000	0.600	154.0	0	0.0162	0.0089	0.351
SUB-TOTAL 3: hybrid substrate											0.0719	2.812
Conductive epoxy	CGlue	1	12.684	2.610	136.000	28.000	0.050	3808.0	3275.0	0.0560	0.0058	0.070
Thermal epoxy	TGlue	1	40.366	1.471	136.000	28.000	0.050	3808.0	533.0	0.3442	0.0063	0.241
SUB-TOTAL 4: hybrid-to-substrate adhesive											0.0120	0.311
Ceramic capa. C1-44, C55	Capa	45	11.091	6.247	1.000	0.500	0.500	0.5	0	0.0001	0.0067	0.070
Ceramic capa. C45-50	Capa	6	11.091	6.247	2.000	1.250	1.250	2.5	0	0.0003	0.0111	0.117
Ceramic capa. C51-54	Capa	4	11.091	6.247	3.200	1.600	1.600	5.1	0	0.0005	0.0194	0.205
Resistor R1-R9	Res	9	25.745	3.918	1.000	0.500	0.350	0.5	0	0.0001	0.0003	0.006
Resistor R11-R13	Res	3	25.745	3.918	1.600	0.800	0.450	0.5	0	0.0001	0.0003	0.007
Resistor R14	Res	1	25.745	3.918	1.000	0.500	0.350	0.5	0	0.0001	2.8×10^{-5}	0.001
Thermistor TM	Res	1	25.745	3.918	1.600	0.800	0.950	1.3	0	0.0001	0.0002	0.005
Soldering paste	SoldPaste	69	7.774	8.386	1.267	0.633	0.120	0.8	0	0.0001	0.0078	0.058
SUB-TOTAL 5: SMD passive components											0.0458	0.469
ABCN-25 chip	Si	20	21.823	2.329	7.550	7.800	0.300	58.9	0	0.0062	0.0396	0.823
Conductive glue	CGlue	20	12.684	2.105	7.550	7.800	0.100	58.9	0	0.0062	0.0255	0.307
Wire-bonds	Wirebond	4760	23.987	2.300	0.025	3.000	0.025	0.1	0	7.8×10^{-6}	0.0011	0.021
SUB-TOTAL 6: ASICS glued and bonded											0.0662	1.151
TOTAL (1+2+3+4+5+6) KEK hybrid (v3)											**0.3264**	**7.073**

Table 19. KEK hybrid (v3) material budget (see text for details).

Item	**Material**	**Num**	X_0 (g/cm^2)	**Density** (g/cm^3)	**Length** (mm)	**Width** (mm)	**Thickness** (mm)	**Area** (mm^2)	**Less area** (mm^2)	**Norm. factor**	X_0 (%)	**Mass** (g)
Silicon sensor	Si	2	21.823	2.329	97.540	97.540	0.320	9514.1	0	1.0000	0.6830	14.181
HV tongue	Cu	2	12.863	8.933	1.000	20.000	0.012	20.0	0	0.0021	0.0004	0.004
Thermal glue	TGlue	416	40.366	1.471	1.500	1.500	0.060	2.3	0	0.0002	0.0022	0.083
SUB-TOTAL 1: silicon sensors with thermal glue											0.6855	14.268
TPG baseboard	TPG	1	42.714	2.260	126.000	72.000	0.600	9072.0	0	0.5721	0.3027	12.302
Parylene cover layer	Parylene	2	32.870	1.289	126.000	72.000	0.020	9072.0	0	0.0191	0.0150	0.468
Facing (cooling-end)	AlN	2	27.464	3.280	13.000	72.000	0.250	936.0	0	0.0246	0.0587	1.535
Facing (far-end)	AlN	2	27.464	3.280	13.000	72.000	0.250	936.0	0	0.0246	0.0587	1.535
Washers	Peek	6	41.466	1.320	5.000	5.000	1.500	$19.6^{\dagger}$	$3^{\dagger}$	0.0027	0.0051	0.203
SUB-TOTAL 2: base-board, facings ans adhesives											0.4403	16.042
Stuffed hybrids		4									1.3058	28.291
Hybrid-facing thermal glue	TGlue	8	40.366	1.471	5.550	28.000	0.080	154.0	0	0.0062	0.0038	0.145
SUB-TOTAL 3: hybrids + adhesive to facings											1.3096	28.436
AS-BUILT SHORT STRIP MODULE (ABCN-25, KEK hybrid v3)											**2.4354**	**58.747**

Table 20. TOTAL (1+2+3): (see text for details). †: area calculated as $(x \cdot y \cdot \pi)/4$.