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FLAXE, a SoC readout ASIC for electromagnetic calorimeter at LUXE experiment

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Abstract: The design and qualification results of a System on Chip (SoC) Application-Specific Integrated Circuit (ASIC), called FLAXE, fabricated in 130 nm CMOS technology are presented. FLAXE is a readout ASIC designed for ECAL-p, a compact electromagnetic calorimeter being a part of a detector system for Laser Und XFEL Experiment (LUXE) proposed at DESY, Hamburg, as an extension to the European X-ray Free Electron Laser (XFEL) facility. ECAL-p is a sampling calorimeter with a very compact design targeting small Molière radius, comprising 16 (up to 20) layers composed of 3.5 mm (1 X_0) thick tungsten absorber plates interspersed with silicon sensors. Sensor signal is read and shaped by the analogue readout channel, comprising a Charge Sensitive Amplifier (CSA) and a fully differential CR-RC shaper with 50 ns peaking time, which output is digitized in each channel by a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). Data from ADC are collected into the ASIC internal memory and read out by the Data Acquisition (DAQ) system between Bunch Crossings (BXs). Around 1000 ASICs have been fabricated and a first batch of 142 ASICs has been packaged and tested. The results of the qualification procedure, as well as measurement result of a single ASIC are presented and discussed.

Keywords: Analogue electronic circuits; Digital electronic circuits; Front-end electronics for detector readout; VLSI circuits

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1 Introduction

The Laser Und XFEL Experiment (LUXE) [1] is proposed at DESY as an extension to the European X-ray Free Electron Laser (XFEL) in Hamburg, Germany, to study strong-field Quantum Electrodynamics (QED) processes in collisions of the 16.5 GeV electron beam of the XFEL with the high-intensity optical laser (in so-called e-laser setup) or in collisions of the laser beam with the high-energy secondary photons produced from the XFEL electron beam (γ-laser setup). Although the QED is already a very well-tested theory, its experimental verification is based on the comparison of the data with precise perturbative calculations of the model. However, in the vicinity of a strong background field, exceeding the rest mass of a virtual particle, the perturbative approach of the QED breaks down as the vacuum becomes polarised. It is expected to observe a creation of physical electron-positron pairs from the fluctuations of the polarised vacuum, when the background field strength exceeds the so-called Schwinger limit. The 350 TW laser pulse, enhanced by the Lorentz boost of the electrons, will exceed this limit in the LUXE experiment, allowing it to explore this uncharted so far QED regime.

The main goal of the experiment is to measure the rate of positrons, originating from the vacuum polarisation, as a function of the laser intensity and quantum parameter χ. The positrons are measured using a conventional tracker-calorimeter tandem, located in the left arm after the first dipole magnet downstream the interaction point (IP). The positron calorimeter, called ECAL-p, is a compact sampling calorimeter with a small Molière radius [2] and high granularity, based on the luminosity detector developed by a Forward Calorimetry (FCAL) collaboration for a future e^+e^- colliders [3]. The ECAL-p is composed of 16 (up to 20) layers of a 3.5 mm (1 X_0) thick tungsten absorber plates interspersed with 1 mm gap where 320 µm thick silicon sensors, developed by the CALICE collaboration [4], are located. Each sensor consist of 16×16 5.5×5.5 mm^2 pads, resulting in 1536 readout channels per layer; every layer comprises six sensors. The readout is provided by the FLAXE System on Chip (SoC) Application-Specific Integrated Circuit (ASIC), developed specifically for the ECAL-p detector to match both the geometric constraints of its compact design and a very specific beam structure of the experiment, with an extremely low Bunch Crossing (BX) rate of only 10 Hz, resulting from the laser charging time. This ASIC is an evaluation of the FLAME ASIC [5], developed for the luminosity detector within the FCAL collaboration, with a redesigned digital back-end and minor changes to the analogue front-end.

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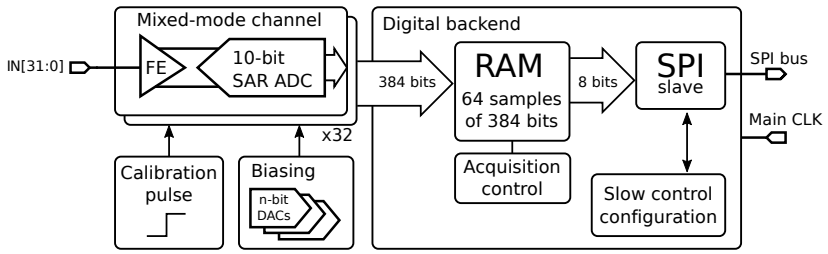

Figure 1. Simplified block diagram of the FLAXE ASIC.

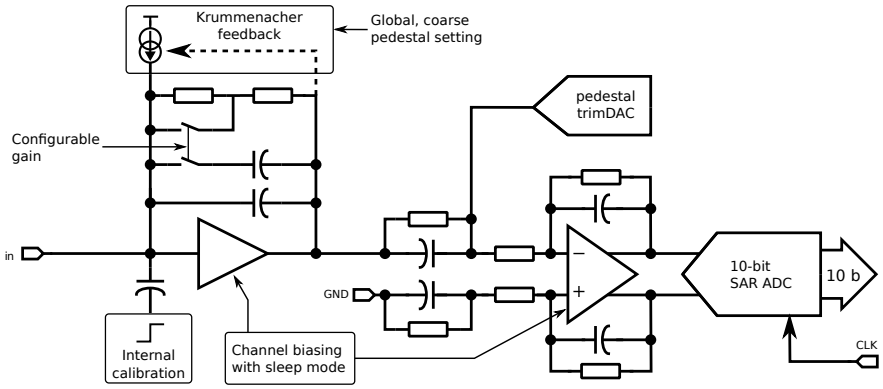

Figure 2. Schematic of the mixed-mode FLAXE channel.

2 FLAXE ASIC

The FLAXE ASIC block diagram is shown in figure 1. The ASIC comprises 32 mixed-mode channels, a digital back-end, an internal biasing circuitry, and a calibration pulse generator. The mixed-mode channel, presented in figure 2, consists of a Charge Sensitive Amplifier (CSA) with two programmable gains, one for a Minimum Ionizing Particle (MIP) sensitivity and a linear range up to around 40 MIPs, and the other extending the dynamic range to around 1250 MIPs. The CSA is followed by a fully differential pole-zero cancellation circuit and CR-RC shaper with a nominal 50 ns peaking time, based on the fully differential amplifier originally developed for the lpGBT ASIC [6]. The analogue part is complemented by a Digital-to-Analog Converter (DAC) for fine per-channel pedestal trimming and Krummenacher feedback circuitry, providing sensor leakage compensation as well as preamplifier DC output voltage shift, which allows for an extended dynamic range for the CSA negative output pulses, while retaining the NMOS input transistor for better noise and bandwidth performance. This voltage shift is programmable, allowing for a coarse, global per-chip pedestal setting. The shaper output is digitised in each channel using a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) [7], operating at 20 MSps sampling rate, matched to the peaking time of the shaper, as required by the signal reconstruction procedure.

Due to the extremely low BX rate of 10 Hz foreseen for the experiment, the digital back-end comprises an on-chip Data Acquisition (DAQ) system based on an internal Random Access Memory (RAM), collecting 64 consecutive ADC samples from all 32 channels around each BX. Although the 10-bit ADC is currently being used, the channel data has been already extended to 12-bit, since in the next stage of the LUXE experiment an evolution of the FLAXE ASIC is foreseen to cover even larger dynamic range expected for higher laser intensity. Therefore a 64, 384 b (32 × 12 b) words are

stored in the internal RAM for each BX. The collected data is read out between BXs using a custom communication protocol, based on Serial Peripheral Interface (SPI) in the physical layer and I^2C in the logical layer. This synergy was chosen to meet the specific requirements of the ECAL-p and LUXE design. The SPI physical layer, in combination with differential drivers, provides sufficient signal integrity for communication with a central DAQ system located up to 100 m away from the detector. The logical layer, based on the I^2C protocol, provides ASIC addressing, which allows multiple ASICs to be connected to a common data bus, reducing the number of connections to the central DAQ. The same protocol is used to access the configuration registers for ASIC programming. Additionally, to reduce power consumption, a sleep mode has been added in which the mixed mode domain is automatically powered down between BXs. This feature can be disabled, keeping the mixed-mode domain constantly powered on for test purposes.

3 Qualification, yield and measurement results

Around 1000 ASICs, as required by ECAL-p demand, were fabricated in 130 nm CMOS technology. The die area is $4045 \times 3725\ \mu m^2$, while a single mixed-mode channel occupies $2800 \times 85\ \mu m^2$. To meet the detector geometrical constrains, a 128-lead Low profile plastic Quad Flat Pack (LQFP) package, with 0.4 mm lead pitch and a thickness below 1.6 mm, was selected. The first batch of 142 ASICs was packaged and qualification tests were performed in mid-2024. To confidently declare the ASIC fully functional, the qualification procedure performs a complete set of measurements under nominal environmental conditions. For the digital back-end, the configuration registers are tested by writing (and reading back) all possible values, while RAM and the data path are tested using dedicated test modes, replacing the actual ADC data with previously known values. The ASIC power consumption is measured, both in sleep mode and in continuous awake mode. Finally, the analogue front-end is tested by measuring each channel's nominal pedestal and noise, trimming DAC response, pulse shape, and peaking time, as well as linear range and gain. The last measurements are made using an external signal generator that provides a voltage step, converted to a sensor-like current signal via a capacitor connected in series to the front-end input. This setup enables precise shaper response measurement by shifting the phase of the injected signal relative to the ADC sampling clock by sub-ns steps, effectively providing ADC samples of the shaper response at intervals equal to these phase shifts.

Unfortunately, for the first batch of FLAXE ASICs an absolutely catastrophic yield of 5% was obtained. Approximately 95% of ASICs suffer from extreme current consumption in at least one of the power domains, with 35% of the entire batch consuming over 700–800 mA rendering them completely unusable. 60% consume 10 to 20 times more than nominal power, and although these ASICs are at least partially operational, extreme overcurrent significantly affects their performance. In particular, the IR drop in the digital power distribution grid manifests itself as numerous bit errors in the DAQ RAM, making it impossible to read the ADC data. Although this issue is still under investigation, many clues point to a failure of the manufacturing process. The excess current consumption acts as pure leakage, being completely independent of the activity of the ASIC, e.g., the presence of the main clock, the ASIC configuration or the applied sleep mode. The most affected part is the ADC supply domain, which was reused from the FLAXE predecessor, the FLAME ASIC, and thus was already silicon proven. In addition to the packaged ASICs, several bare dies were also received from the manufacturer. Some of these were tested for current consumption and were found to behave exactly the same as the packaged ones, eliminating the packaging as a possible failure point. The bare dies were examined with an

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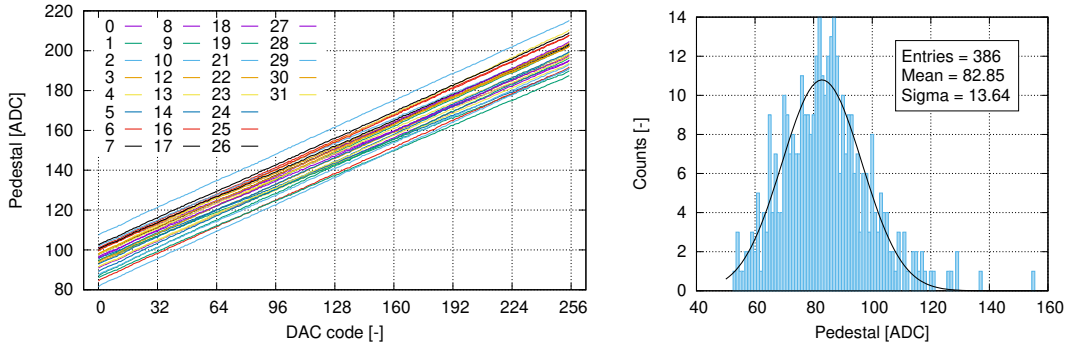

Figure 3. Trimming DAC response of a single ASIC (left) and nominal pedestal spread for all measured channels (right).

infrared camera, clearly showing extreme power dissipation at the silicon level, under the metallisation, mainly in areas where thick silicon oxide was used for power supply decoupling capacitors and IO ESD structures (both already also silicon proven), which may pin-point failure. Due to these problems, only seven ASICs were found to be working quite well, although even these had a few dead channels. Furthermore, several ASICs showed few enough RAM errors to allow mixed-mode channel testing, resulting in 386 channels tested for nominal pedestal and noise and around 190 for pulse shape and gain.

The trimming DAC response of a single ASIC (FLAXE ID 136) and the spread of the nominal pedestal value are shown in figure 3. Due to a small mistake in the qualification procedure, the pedestal value was measured for the minimal trimming DAC setting, instead of the middle one. Despite this issue, the results show that the trimming range of around 100 Least Significant Bit (LSB) is fully sufficient to cover the pedestal spread over many ASICs. The pulse shape and peaking time spread are shown in figure 4. Both results are within the specification and agree very well with the simulations, showing an average peaking time of 54 ns (8 % higher than designed 50 ns) with minimal spread, while the pulse shape demonstrate a very small deviation from the ideal CR-RC shape. The linearity measurement result of a single ASIC and the gain spread are shown in figure 5. Only the high gain of the CSA was measured as the primary point of interest for the initial ECAL-p development, leaving the low gain for a more detailed characterisation in the future. Again, both results agree almost perfectly with the simulations, showing an average gain of 3.94 LSB/fC (1.5 % lower than simulated) and a linear range as expected from the simulations.

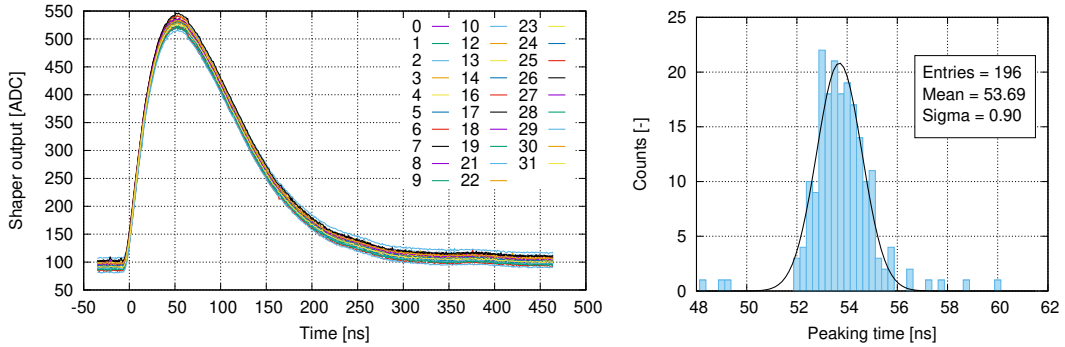

Figure 4. Shaper pulse response of a single ASIC (left) and peaking time spread for all measured channels (right).

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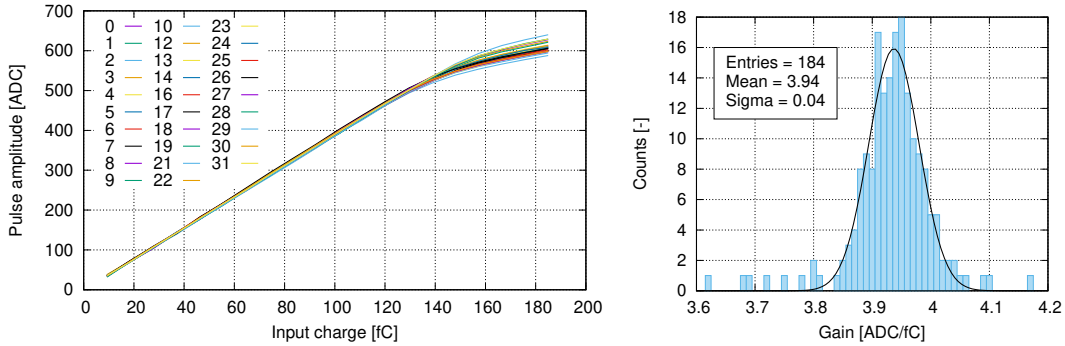

Figure 5. Linearity measurement of a single ASIC (left) and gain spread for all measured channels (right).

In selected ASICs that did not have an excessive overcurrent, it was possible to estimate the power consumption of individual domains. With the mixed-mode domain being constantly powered on, the ASIC consumes a total 71 mW (2.2 mW per channel), with 37 mW (1.2 mW per channel) contributed by the analogue front-end, 12 mW (375 µW per channel) by the ADC domain, and 22 mW (690 µW) by the digital domain. In sleep mode, the power consumption of the front-end and ADC domains drops below measurable level, resulting in a total ASIC consumption of 19 mW (600 µW per channel) coming solely from the digital domain.

4 Conclusions

The SoC readout ASIC, dedicated to the ECAL-p detector for the LUXE experiment, has been designed and fabricated. A first batch of 142 ASICs has been packaged and tested. Unfortunately, during the measurements, a catastrophic yield of 5 % was found. The most likely reason for this is an error in the manufacturing process, which has resulted in extremely high leakage currents being measured in most ASICs. Due to this problem, the dicing and packaging of the remaining wafers was cancelled. All working and measurable channels were characterised during qualification tests, showing performance and parameters perfectly in line with both the specification and simulations. The huge power consumption issue is currently being investigated in detail before the design is resubmitted for another run, as measurements of the working ASICs show that the design is perfectly suited for the ECAL-p requirements.

Acknowledgments

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