Development of the ABCStar front-end chip for the ATLAS silicon strip upgrade

2017 JINST 12 C04017

(http://iopscience.iop.org/1748-0221/12/04/C04017)

Published by IOP Publishing for Sissa Medialab

Received: *November 15, 2016*
Revised: *January 24, 2017*
Accepted: *March 13, 2017*
Published: *April 19, 2017*

Topical Workshop on Electronics for Particle Physics,
26–30 September 2016,
Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany

Development of the ABCStar front-end chip for the ATLAS silicon strip upgrade

W. Lu,[a,1] **F. Anghinolfi,**[b] **L. Cheng,**[a] **J. De Witt,**[c] **J. Kaplon,**[b] **P. Keener,**[d] **A. Narayan,**[d] **M. Newcomer**[d] **and K. Swientek**[e] **on behalf of the ATLAS ITk Strips collaboration**

[a] *State Key Laboratory of Particle Detection and Electronics, Institute of High Energy Physics, Chinese Academy of Sciences, Beijing, China*
[b] *CERN, European Certer for Nuclear Research, Geneva, Switzerland*
[c] *University of California Santa Cruz, Santa Cruz Institute for Particle Physics (SCIPP), Santa Cruz, CA, U.S.A*
[d] *University of Pennsylvania, Philadelphia, Pennsylvania, U.S.A*
[e] *Department of Physics and Applied Computer Science, AGH University of Science and Technology, Krakow, Poland*

E-mail: weiguo.lu@cern.ch

Abstract: The ATLAS experiment will build an all-silicon tracker in the Phase II upgrade for the High Luminosity LHC (HL-LHC) at CERN. For the silicon strip detector of the Inner Tracker, a new readout chip ABCStar is under design to cope with the increased occupancies and harsher radiation environment, and to accomodate the new trigger architecture. In this paper, we summarize the status of the design work and present the new features of the chip.

Keywords: Analogue electronic circuits; Digital electronic circuits; Front-end electronics for detector readout; VLSI circuits

[1] Corresponding author.

doi:10.1088/1748-0221/12/04/C04017

Contents

1 Introduction

The Large Hadron Collider (LHC) at CERN will undergo another upgrade around 2023, referred to as the High Luminosity LHC (HL-LHC). Improved radiation resistant and finer granular detector structure will be required for the severalfold higher instantaneous luminosity, and the much higher track density, after the Phase II upgrade [1]. The ATLAS experiment will replace the current Inner Detector with a new tracking system, named as the Inner Tracker (ITk). It will be an all silicon detector made up of a pixel detector at small radius close to the beam line and a large area strip detector surrounding it. In figure 1, the ITk Strip Detector barrel layers and end-cap disks are shown.

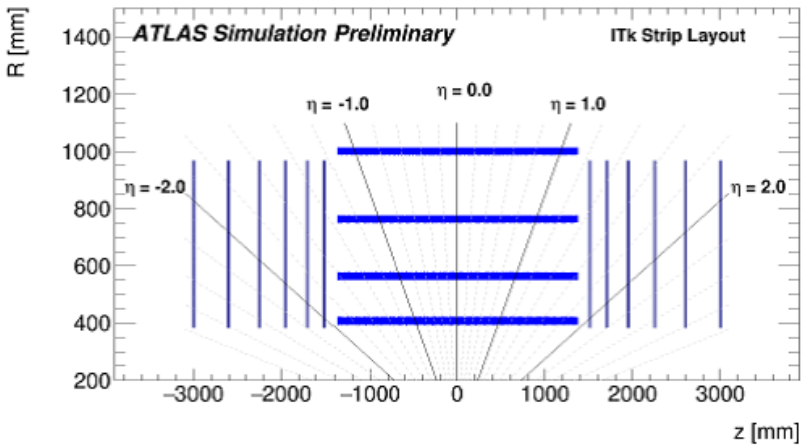

Figure 1. Layout of the ITk Strip Detector.

Compared to the current ATLAS SemiConductor Tracker (SCT), there will be significant increase in size and complexity for the new strip detector [2]. Each cylinder of the barrel will be segmented into staves, and the end-cap disks into petals. Detector module is constructed as the basic building block for each stave and petal. Figure 2 shows the prototype design of the short strip barrel module. On top of the silicon strip sensor, each of the two readout hybrids contains 10 ATLAS Binary Chip (ABC) and one Hybrid Controller Chip (HCC). A power board located between the two readout hybrids provides necessary power to the read-out ASICs and auxiliary on-detector electronics used for monitoring, control and sensor HV biasing.

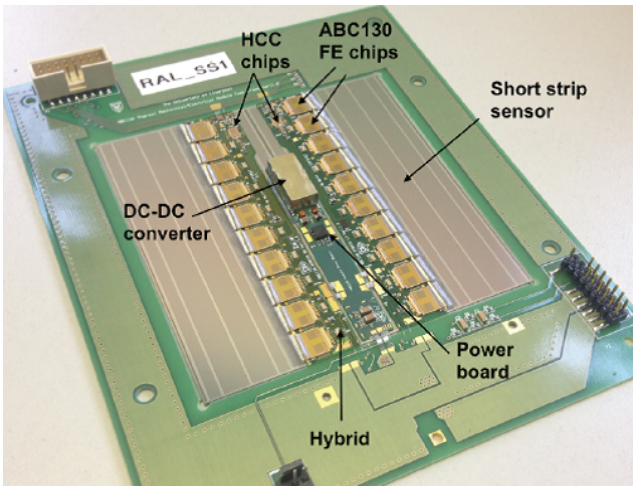

Figure 2. Short-strip barrel module with test structure (green frame).

The ATLAS upgrade trigger rates and latencies have been changed after the fabrication of the prototype ASIC named ABC130 which employed the chained readout scheme [3]. The readout architecture of on-detector electronics could not support the latest trigger requirements and a design change was required. The fundamental change was the interface from ABCs to the HCC as shown in figure 3. Serial transfer of data to the HCC was changed to direct communication from all ABCs to the HCC-hence the new ABCStar and HCCStar. This "star" configuration will remove the bandwidth bottleneck in data transfer to the HCC, and significantly simplify the system architecture.

2 ABCStar design

This chip must provide all functions required for processing of signals from 256 strips of a silicon strip detector in the ATLAS experiment employing the binary readout. The architecture chosen for ABCStar allows a multi-trigger data flow control retaining the beam crossing synchronous pipeline transfer signal (L0) from previous versions, a first asynchronous read out request (PR) with priority and low latency (this signal is distributed to a fraction of the detector to get the tracking data participating to the L1 trigger) and a second asynchronous data readout request (LP) intended for a global readout. Besides the essential front-end and power regulation, the main functional blocks of the digital part include: Input Registers block, two stage buffers, Cluster Finder, Readout, Command Decoder and Top Logic. A simplified diagram of ABCStar chip is depicted in figure 4.

2017 JINST 12 C04017

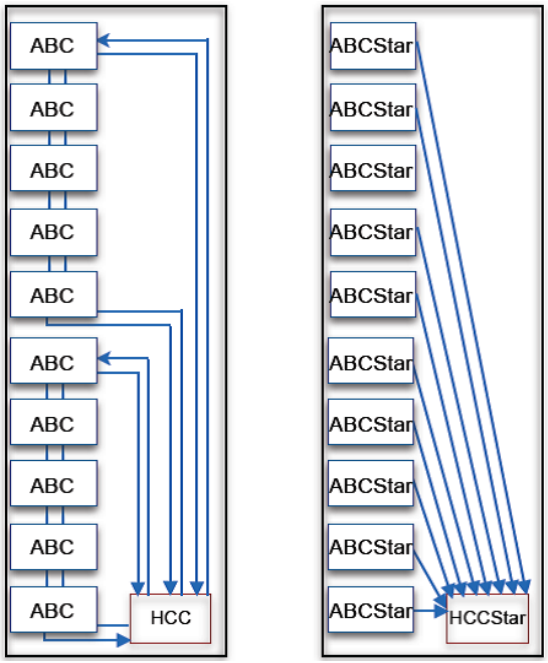

Figure 3. From ABC130/HCC130 to ABCStar/HCCStar.

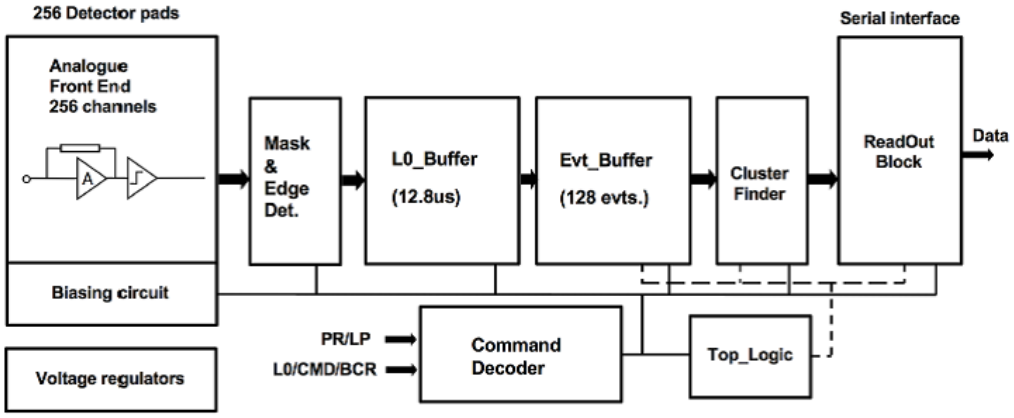

Figure 4. Block diagram of current ABCStar.

Signals from the detector are first processed by the front-end which contains 256 analogue preamplifier-shapers followed by discriminators with individual threshold trimming capabilities. The binary output of the discriminator are sampled at the bunch crossing clocking rate and stored in the pipeline (L0 Buffer) after an "edge detection" process. At reception of the L0 signal, data in the memory that were stored at some fixed latency time before the L0 signal are extracted from the pipeline and transferred to the Event Buffer and stored as events tagged with an appropriate L0ID number. If a PR or LP signal is received with the corresponding L0ID number, the event is extracted from the Event Buffer and processed through the Cluster Finder. The Cluster Finder block acts as a data reduction circuit, creating a "cluster" byte for channels found with hits. The Readout

block does formatting packets with the event identification and the associated cluster bytes. In the end, the data is transmitted serially to the following HCC chip with point to point connection.

The Command Decoder block receives and distributes internally the trigger signals (L0, PR and LP). Through the same input the chip receives the configuration commands, the analog bias settings, the mask and test and calibration settings, the register read-back instructions. The Top Logic block is the autonomous sequencer that controls the data flow path according to the arrival of the L0, PR, LP trigger signals.

2.1 Front-end test and redesign

The new ABCStar chip is still in design phase. The readout is different, but its front-end part should be similar to that of the ABC130. Therefore, the ABC130 chip is under evaluation with particular focus on the front-end performance. Figure 5 summarises the noise measurements as a function of the input load capacitance for a range of prototype devices including the ABC130 front-end prototype, ABC130 single-chip test cards and full barrel hybrids with front-ends connected to both discrete capacitors and sensors.

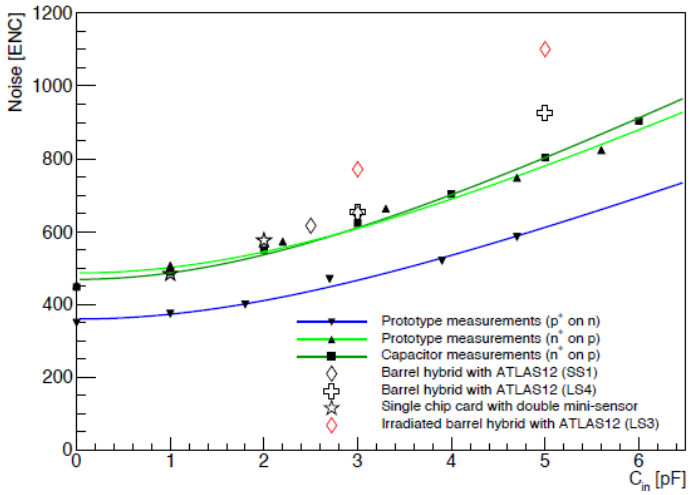

Figure 5. Measured noise as a function of input capacitance for a range of prototype devices.

A better noise performance was observed for the prototype front-end with positive signal (for the old p-on-n strips). For negative signal (for new n-on-p strips), although good agreement of noise behavior was achieved between the prototype front-end, the capacitive loading of hybrids and single chips, the noise was found to be higher than expected. In addition, excessive noise was observed after irradiation. As shown in figure 6, noise increased with the Total Ionizing Dose (TID) and reached a plateau after 15~20 MRad. No recovery towards the pre-rad value could be obtained [3].

The main possible reason of the worse noise performance after sensor polarity swap is the effect of the signal compression for negative signals caused by modulation of the trans-conductance of the active feedback transistor. This can be resolved by changing the pre-amplifier to resistive feedback. The noise increase after ionizing radiation is possibly due to the substantial increase of $1/f$ noise for regular NMOS devices. This can be improved in using gate enclosed layout for the critical NMOS transistors. The front-end is currently under partial redesign. Besides the two

modifications for noise performance improvement, the new front-end has been optimized for the measured sensor parameters after radiation, and a new biasing schema has been adopted for preamp and shaper to improve matching between channels.

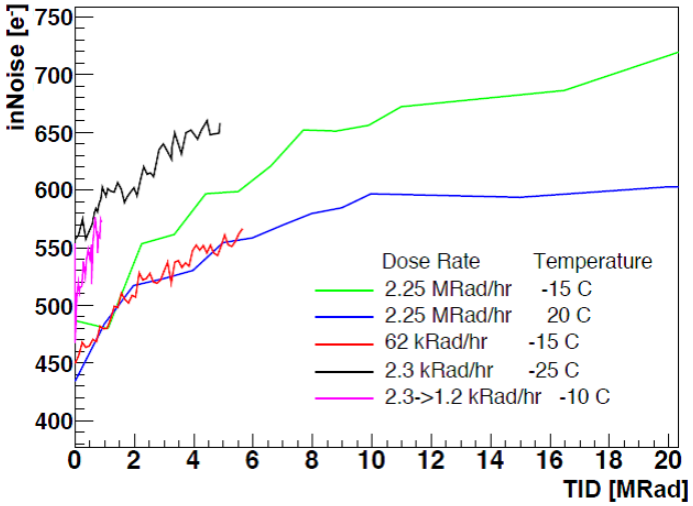

Figure 6. Increase of input noise as a function of TID.

2.2 Input registers block

This block includes the legacy functions of input register and mask/test register that was found on the ABC130. The input register latches the incoming data with the Bunch Crossing (BC) clock and delivers a clocked pulse to the subsequent circuit in data taking mode. It is also used to disable the outputs of front-end channels in the test modes. The mask/test register also serves a dual purpose. Firstly, it enables any bad or noisy channels to be turned off thus preventing them from increasing the data rate due to false hits. Secondly, it can be used during chip testing to apply a set of test patterns to the pipeline, continuously for static test and pulsed for dynamic test.

Table 1. Edge detection criteria.

Det_mode(1:0)	Name of Selection Criteria	Hit Pattern (Oldest data bit 1st on the left)	Usage
00	Hit	1XX or X1X or XX1	Detector alignment
01	Level	X1X	Normal Data Taking
10	Edge	01X	Normal Data Taking
11	Clear	None	Special Mode

The main feature of this block is the Edge Detection Circuit. It compares continuously the input signals corresponding to 3 consecutive BC clock periods with a given pattern. For each successful matching the circuit generates a pulse of duration one clock cycle. The effect of this circuit is that only a single "1" is written into the pipeline for every hit detected according to the match criteria, irrespective of the length of the incoming pulse. The various patterns of 3 consecutive BC are listed in table 1. By putting this Edge Detection Circuit in front of the pipeline, only one BC slot hits is to be transferred from Pipeline to Event Buffer per L0, making the readout system adaptable to

possible consecutive L0 triggers, which is one of the new requirements from physics. In order to test the function of Edge Detection, a new pulse test option was defined to provide 4 bits pattern along 4 consecutive BC cycles which can be triggered by particular command applied through the Command Decoder.

2.3 Two stage buffers

The two stage buffers inherit from the structure of the ABC130. The Pipeline (L0 Buffer) and the Event Buffer are all realized with single port RAM blocks, but the size of the two buffers are changed to cope with the different latencies as illustrated in table 2 and figure 7. The Pipeline is made of two RAM blocks of 320 bits (wide) by 256 bits (length), with the total pipeline length of 512 bits to accept hits for the 12.8us L0 latency. Whereas the Event Buffer is realized by one RAM block of 320 bits (width) by 128 bits (length) which is able to store 128 L0 tagged "events".

Table 2. Trigger rates and latencies of current design.

Trigger	Rate/Hz	Latency/μs	Description
L0	1M	2-12.8μs programmable	Synchronous
PR	100k	Few 100ns after L0 earliest	Asynchronous
LP	400k	~128μs latest LP	Asynchronous

A simplified diagram of the two stage buffers is shown on figure 7. With continuous writing of hits into the Pipeline, the two single port SRAM blocks are interleaved to allow simultaneous write and read operations. At every occurrence of L0, one event in the Pipeline is prone to be written directly into the Event Buffer. The operation can be continuous for several clock cycles in case of consecutive L0 signals. A small size of intermediate FIFO controlled by appropriate logic is inserted between the Pipeline and the Event Buffer to give priority to the read operation of the Event Buffer. When a read occurs, after a LP or PR trigger, if a L0 is at the same time, the event is stored into the intermediate FIFO for one clock cycle. This keeps the delay between receiving a PR/LP trigger and sending the corresponding data to the Cluster Finder block as small as possible.

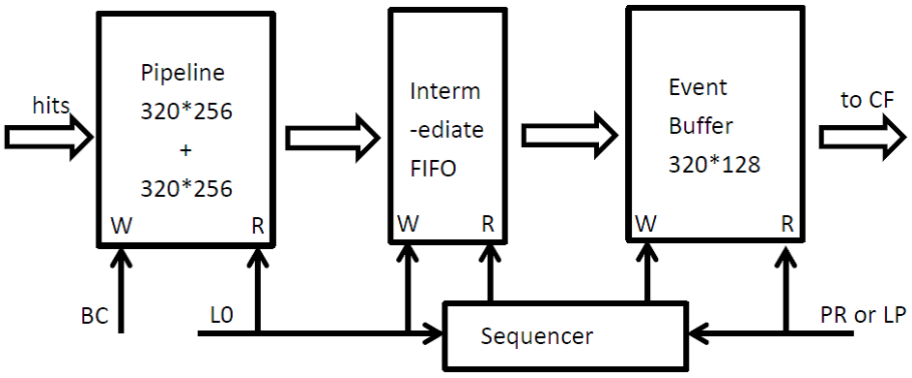

Figure 7. Structure of two stage buffers.

2.4 L0 tag insertion

In ABC130, local counters are used for event identification. These counters are prone to errors due to missed or extra triggers transmitted or SEU (Single Event Upset) effects encountered in the counters. Once a counter is in error state, all the following events are out of order until the counter is reset. Thus a new scheme of L0 with tag has been proposed for ABCStar. Each L0 trigger will be accompanied by a tag which will be sent back as part of the event data, off-detector electronics will check for matching tags. Errors will still occur for the same reason, but each error should result in at most two lost or corrupted events rather than a long series of lost events [2].

The present implementation is to encode the L0 and L0tag (together with the Command and BCReset) into 4-BC frame transmitted on a 160Mbps physical differential line. For this purpose a new protocol called LCB is developed for ABCStar and HCCStar.

2.5 Cluster finder

It is anticipated that for any event a limited number of channels will contain hits. This fact can be used to reduce the number of bits that have to be read out for each event. The Cluster Finder will scan through the 256 channel input bits. If it finds "1", it creates the 8 bits address of the channel, then adds the values of 3 next channels. This operation is repeated until the last cluster is found. The 12-bit cluster byte is shown in table 3, it consists of 8 bits of hit address, 3 bits indicating the following 3 strip values and 1bit denoting whether it is the last cluster or not.

Table 3. Cluster byte format.

Hit Address	Following 3 strip values	Last cluster
8bits	3bits	1bit

In order to keep the minimum latency for PR readout mode, an algorithm has been implemented for the Cluster Finder. It takes in 256 bits of strip data from the Event Buffer and reports out 12-bit clusters at 40MHz. As the ABCStar chip is designed to read out two rows of strips, a rearrange block separates the input data into 2 banks of 128bits each called odd and even banks, to group together bits of adjacent channels in a strip row of the detector. Each Cluster Finder sub-block treats 128 strips of the same row. They are enabled in turn by a state machine. The two banks report out clusters one bank at a time alternatively to avoid bias to either bank.

2.6 Readout

The Readout block is responsible for building data packets with the hit patterns coming from the Cluster Finder blocks or from the registers to be read. A controller inside defines the order in which packets are formatted. Then each packet is transmitted to the fast 160Mbps serializer. All packets belonging to one event are sent out consecutively. Table 4 describes that the output format is a variable length readout packet with a maximum length of 68 bits for the physics data. The estimated

Table 4. Data format of ABCStar.

Start Bits	Header	Payload (4 clusters max.)	Trailer
3	16	12, 24, 36 or 48	1

average event size per chip is 2 to 3 clusters, therefore the average packet size is at most 56bits and the average data rate at the output of one ABCStar chip is 56Mbps for 1MHz L0 trigger rate. The 160Mbps readout rate has been chosen to reduce the transmission latency for PR packets that contribute to the L1-track trigger.

3 Verification of ABCStar

As shown in figure 8, a top verification setup based on the UVM (Universal Verification Methodology) has been built to facilitate the ABCStar design. It delivers functional coverage with customized random stimulus, result comparison with reference models and SystemVerilog assertions for validating key design features [4]. Validation results showed the clear advantages of this powerful UVM setup compared to the traditional verification method using the Verilog test cases.

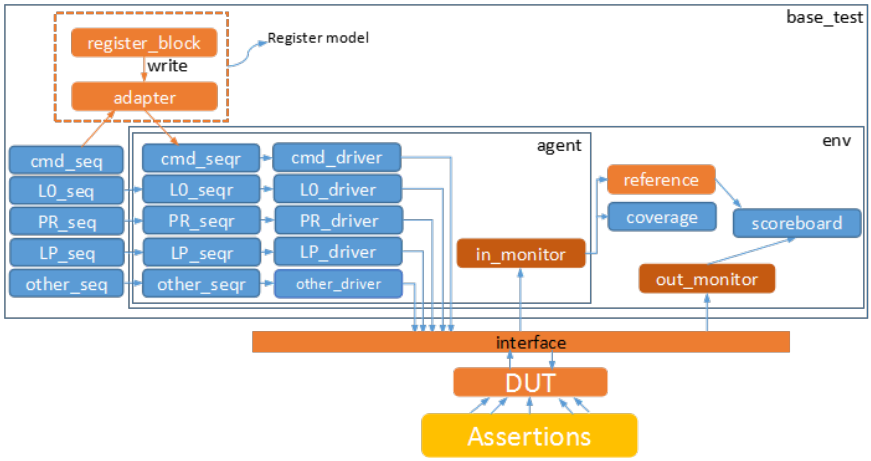

Figure 8. Diagram of ABCStar testbench based on UVM.

The ABCStar chip is being designed to support various trigger modes listed in table 5. Although the exact trigger specifications are still under discussion, this UVM setup is used to verify the current design under several possible trigger conditions. As shown in table 5, the current design is tested with the different trigger rates. Fixed latencies and distribution laws are adopted for L0, LP and PR during the tests according to the experimental trigger models.

Table 5. Supported trigger mode and tested trigger conditions.

Trigger mode	Description	Example tests with UVM setup
L0	Capture and readout at L0 rate	L0@1MHz, LP@1MHz
L0/LP	Capture data at L0, send requested data at LP rate	L0@4MHz, LP@1MHz
L0/PR/LP	Capture data at L0, send data with priority at PR rate, send remaining requested data at LP rate	L0@4MHz,LP@1MHz,PR@100KHz; L0@1MHz,LP@400KHz,PR@100KHz

2017 JINST 12 C04017

4 Conclusion

The design status of the ABCStar chip has been presented. Its specifications are yet to be fully defined, and several options are still under discussion. Compared to its predecessor the ABC130, important new features are added, which are mainly motivated by the new requirements of the higher trigger rates and lower readout latency towards the ATLAS Phase II upgrade.

Design and verification of ABCStar chip is ongoing. Besides the new features that were described in the previous sections, several other items are under consideration. For instance, adding an individual chip identifier programmed by eFuse and, adding an analog monitor circuit to measure the regulated voltage and temperature. More items like improved input ESD protection, hits accumulators for calibration, extended range regulator and new SEU mitigation techniques, which are still in progress, are not described in this paper.

Acknowledgments

IHEP's work is supported by the CAS-Helmholtz Joint Research Group Program and the National Key Program for S&T Research and Development (Grant No:2016YFA0400101). We would like to thank many colleagues from the ITk strip collaboration for their valuable discussions and strong supports.

References

[1] ATLAS Collaboration, *Letter of Intent for the Phase-II upgrade of the ATLAS Experiment*, CERN-LHCC-2012-022 (2012).

[2] A.A. Grillo, *ATLAS Silicon Strip Electronics*, ATL-UPGRADE-SLIDE-2016-116 (2016).

[3] ATLAS Collaboration, *Technical Design Report for the ATLAS ITk Strips Detector*, ATL-COM-UPGRADE-2016-040 (2016).

[4] L. Cheng et al., *A Testbench Research based on UVM for ABCStar*, in *IEEE-NPSS Real Time Conference (RT)* (2016).

2017 JINST 12 C04017