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Architecture and characterization of the P4DI CMOS hybrid pixel sensor

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ABSTRACT: Gamma ray imaging can be used for the extraction either of the activity map of a source or of the attenuation map of an object or both, as well as for the identification of the material composition of the emitting source or the object. All these imaging modalities can benefit from instruments giving the information of the energy of the converted photons and also the spatial and time coordinates of the conversion. The P4DI CMOS and hybrid provides the core technology for this task being a 2-D array based on Cd(Zn)Te material for the sensing layer. It consists of 1250 pixels with 400 μm pitch. The energy resolution of the ^{241}Am photopeak is 3.5 keV, time resolution is less than 12 μs and power consumption is less than 100 mW. Architecture and characterization are described.

KEYWORDS: Front-end electronics for detector readout; Hybrid detectors; Pixelated detectors and associated VLSI electronics; Compton imaging

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1 Introduction

During the last two decades a lot of effort has been devoted to the development of imaging devices of ionizing radiation using hybrid pixel detectors, where the detecting layer is made of semiconductors of high atomic number, Cd(Zn)Te mainly [1, 2]. Their success in gamma ray imaging is attributed to the energy resolution achieved by Cd(Zn)Te. This energy resolution may prove useful not only for the spectroscopic identification of the emitting source, but also for Compton scattering exploitation. Compton scatter imaging could provide many desirable features [3]: source activity orders of magnitude below conventional systems by avoiding collimators, direct and quantitative measurement of the electronic density of the studied object, sensitivity to low-density materials, it permits placement of both the radiation source and the detector on the same side of the object etc.

A significant amount of research and development around Compton imaging has been focused on localization of radioactive sources for security purposes [4, 5], although it was triggered by the successful implementation of the device concept presented in [6] for astrophysics [7]. Besides, this device was the first Compton camera used after the Fukushima accident to obtain radiation distribution maps [8].

The hybrid pixel sensor described in this paper was conceived as the core technology component of a Compton camera to be used for security-safety [9]. It combines state of the art functionality and performance with significantly lower power consumption, compared to those achieved by 1-dimensional readout circuits connected through fanout boards to Cd(Zn)Te detectors [10, 11]. The goals of our design were: (a) to demonstrate a pixel sensor which for every photo-conversion it could be capable to register energy and time tag and output this information together with address in digital format. (b) To include all this functionality in a system with manageable power consumption.

Table 1.

Num. of input channels	1250 (50 rows \times 25 columns)
Pixel pitch	400 μm
Input charge maximum	± 35 fC (218750 electrons)
Power Supply /Power Dissipation	1.8 V/100 mW max, 70 mW during hit recording period
Noise	Lowest gain 255 el(rms), Highest gain 410 el(rms)
Gain - peaking time configurable in eight combinations (see [15]).	Lowest gain: 18.9 mV/fC - 1.38 μs Highest gain: 58 mV/fC - 3 μs
Detector pixel leakage current	± 900 pA
A/D Conversion - Readout time	102.4 μs - 100 ns per pixel with hit
Counting capability	Time to first count

Furthermore, as every pixel is reset after it registers a hit and consequently not all hits are recorded, the average of the recorded time tags can be used for the estimation of the radiation field strength. Thus, “time to first count” readout has been implemented.

Critical parameters of the Compton camera [9] are detection efficiency and energy resolution, because they influence the event statistics, the uncertainty of the Compton scattering angle determination, the time needed to reach a conclusion about the identity and the direction of the source. Time of flight measurements were considered not possible, since the distance between successive interactions is small due to the hand-held size of the device. However the determination of the correct time sequence of interactions would be facilitated by electronics with time resolving capability, because time tagging helps to reduce the combinatorial background.

The main figures of the CMOS chip are displayed in table 1. It is a 2-D array which gives the charge deposited by a photo-conversion and the time of occurrence of this event simultaneously. The low power consumption and the existence of pads only on the one side enables the construction of $2 \times N$ matrices by tiling the hybrids Also the readout mode explained in section 6 permits the recording of dense temporal or spatial bursts without pile-up and, as referred previously, the estimation of the radiation field strength. A discussion of the methodology used to estimate the detecting layer influence has been given in [12].

Industrial applications could benefit from this hybrid, as it could be used in devices which measure the energy of the scattered gamma rays in a coincidence window with non-scattered gammas having the initial energy. With this information the reconstruction of the electronic density of the scattering material can be reconstructed [13]. The 400 μm pixel pitch enables its use in coded aperture imaging applications with mask element size of some mm [14].

The rest of the paper is organized as follows: in section 2, the chip architecture and main characteristics are described. In section 3, the details of the pixel design are presented. In section 4, the embedded controller architecture and operation are described briefly. In section 5, the operational sequence is presented. In section 6 the test setup and chip characterization results are discussed and conclusions are given in section 7.

2 Chip overview

P4DI_v2F is an integrated circuit with 1250 pixels organized in 50 rows \times 25 columns. It has been manufactured in the UMC 0.18 μm mixed signal 6 metals process. An image of the chip can be seen in figure 1(a). The chip contains more than 2 million transistors on a 10137 μm \times 22128 μm die. Each pixel contains an analog block where the sensor charge signal is amplified and compared to a threshold by a discriminator. The pixel hit flag sets in hold mode a detector which finds the peak of the amplified charge signal and triggers the production of a time flag in the form of an analog voltage level. The two voltage levels (amplified charge and time) are digitized in-pixel using single slope A/D conversion. The digital readout part transfers the two pixel voltage levels either in analog or in digital format to the chip periphery and recognizes and produces the address of the hit pixel. The hit pixel data and addresses are transmitted serially out of the chip.

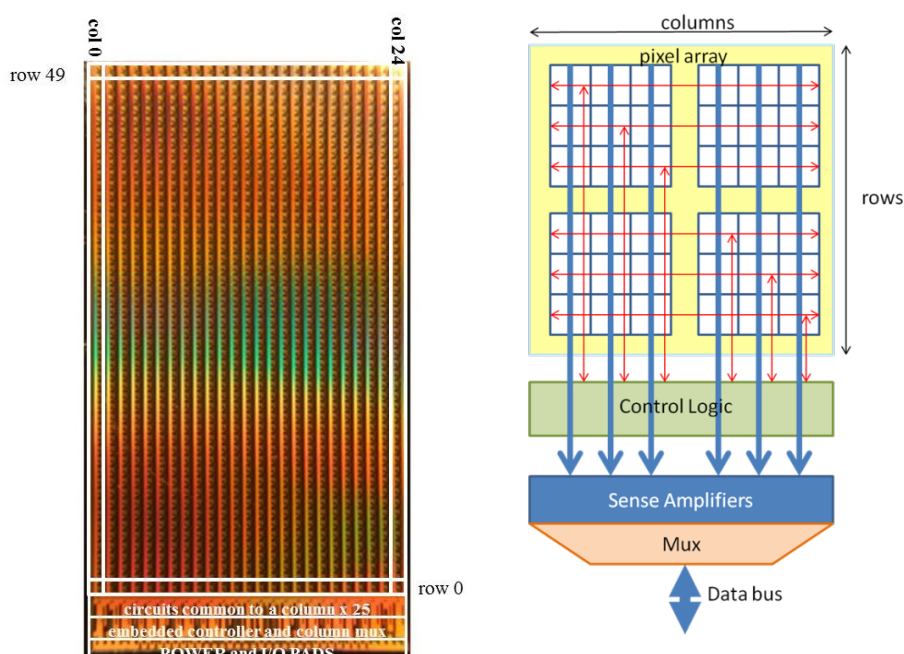


Figure 1. Left: the P4DI_v2F die. Right: main blocks of its circuitry identified.

The block diagram of the chip in figure 1(right) shows the constituents of the chip: the pixel array, the embedded controller, pixel control and data path flows. The data path (bold blue lines in figure 1(right)) consists of 25 column buses. Each bus has two groups of 10 bit lines. At the end of each bit line a sense amplifier regenerates the digital level received and forwards the signal to a multiplexer. An alternative path for the transmission of information in analog form (with in pixel digitization switched off) consists of voltage buffers at the pixel and column level. The control path (red lines in figure 1(right)) contains: (a) one initialization control bus for every column for the transfer of the pixel initial configuration data, (b) a hit row bus and a hit column bus, (c) a select row bus and a select column bus. The purpose of the hit and select bus is the readout of only the pixels which have been hit. The digital data are transmitted out of the chip at 100 MHz using four lines: one for the 10 bit digitized charge signal, one for the 10 bit digitized time tag and two lines for

the column and row address of the pixel. Alternatively the transmission of the two analog voltage levels is done at 10 MHz.

For test purposes, internal nodes of the analog part of one pixel (row = 0, col = 0) are buffered and driven to output pads, while another pixel (row = 0, col = 1) is used to test the DRAM operation and the in-pixel A/D conversion.

3 Pixel description

Each pixel includes an analog and a digital part. Figure 2 presents a simplified schematic. The analog part of the pixel contains a charge amplifier which is directly connected to the detector through a bump bonding pad. A leakage current compensation block is connected to both the input and the output of the charge amplifier. The charge amplifier is followed by the shaper amplifier. The circuitry supports detectors with either positive or negative bias voltage. Thus, when a detector that sources current is bump bonded, then the charge amplifier is connected directly to the shaper. An inverter block is activated and introduced between the charge amplifier and the shaper, when a detector that sinks current is connected. A comparator tracks the changes of the shaper output and triggers the production of a flag, when the pixel is hit. The hit flag (actually produced in the digital part of the pixel) activates both the peak detector and the time to voltage converter. The peak

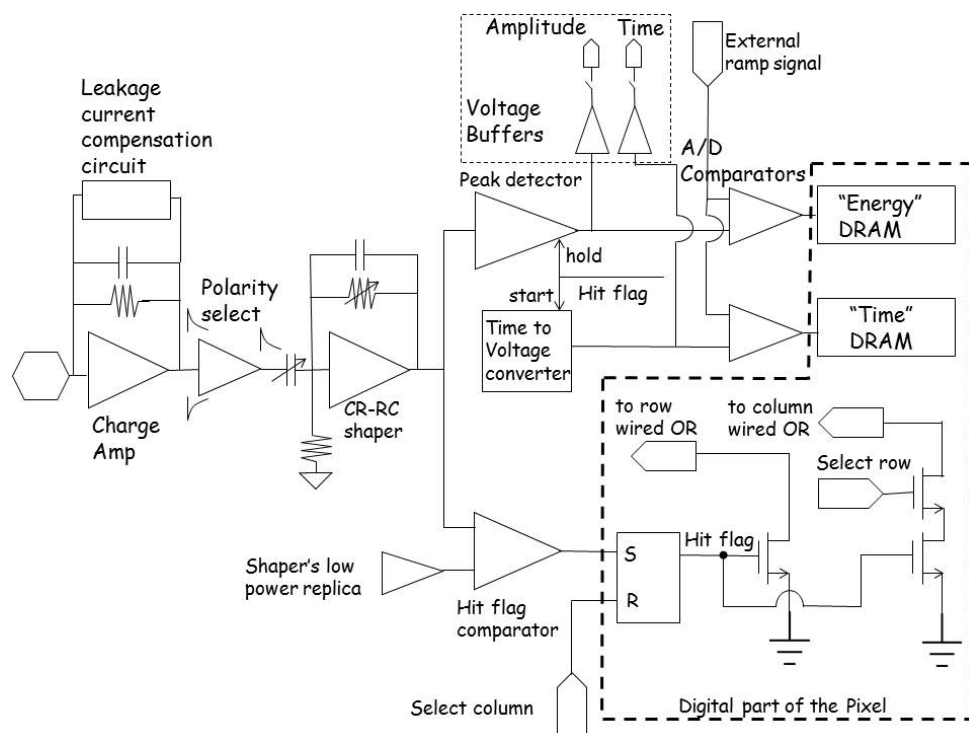


Figure 2. Pixel schematic block diagram with all the main blocks: charge amplifier, leakage current compensation circuit, polarity select circuit and shaper. Hit flag comparator and time to voltage converter. Digitization comparators and the analog buffers used to transfer out of the pixel analog voltages in case digitization is disabled. The main blocks of the digital part of the pixel are also presented: the hit flag production circuit and the 10 bit 3-T DRAMs.

detector input is connected to the output of the shaper and stores the peak value of the signal. The time to voltage converter stores the time of the hit. The amplitude and time of hit information are then converted to a digital pulse by two separate comparators connected to the output of the peak detector and of the time to voltage converter correspondingly. The same information (amplitude and time of the hit) is available in analog form too. Using voltage buffers this analog information can be guided to dedicated output pads. The digital part of the pixel contains logic circuitry which stores and resets a pixel hit-flag and informs the embedded controller that this hit-flag has been set. It sends control signals to the analog part of the pixel. These signals control the operation of the peak detector, of the time to voltage converter and of the digitization comparators while they switch on and off the charge amplifier and the shaper according to the readout sequence which is explained in section 5. It contains the two 10 bits DRAMs which store the digitized outputs of the peak detector and of the time to voltage converter, as well as circuits that generate the write and read signals of the DRAMs. Finally it contains a 14 bits configuration register which provides various adjustments at the pixel level: masking of the pixel, enabling of its test input, selection of the polarity according to the bias of the detector, selection of one out of eight combinations of gain + shaping time, selection of one out of eight threshold levels for the hit flag comparator as well as setting of its hysteresis margin, adjustment of the pole of the low pass filter used in the leakage current compensation circuit and switching on-off of the in-pixel digitization.

3.1 Pixel analog circuit blocks

The charge sensitive amplifier (figure 3a) uses a single ended folded-cascode topology with a PMOS input device. The feedback resistor is implemented by a PMOS and an NMOS transistor connected in parallel. The voltage levels used to bias these devices are different and the choice depends on the amplifier's input current pulse direction so that the one device behaves as a voltage controlled resistor and the other is completely off. An additional enable digital signal is used to power down the charge amplifier. After a hit event of sufficient energy (enough to trigger the comparator connected to the output of the Shaper) the charge amplifier is switched off by the pixel's internal logic until the pixel is ready for the next event. The switches shown in figure 3a implement the power down while the charge amplifier's output is kept at a voltage level close to its operating one. Resistors connected in series to the source nodes of the biasing transistors decrease the noise generated by them. They are practically degeneration resistors which ensure ideal current mirroring and at the same time suppress noise by reducing the gain of the transfer function from their gates to the output.

The output of the charge amplifier is connected to one input of the leakage current compensator forming a negative feedback closed loop. The other input of the leakage current compensator is driven by the output of a low power replica of the charge amplifier. This low power replica provides one output either few millivolts above or few millivolts below the DC level of the charge amplifier. If leakage current appears, the output DC voltage of the charge amplifier moves away from its no-leakage value towards the one of the two limits depending on the leakage current direction. The closed loop operation does not allow this voltage to exceed the limits, thus cancelling the correct amount of leakage current.

The shaper's output drives a discriminator circuit which produces a pulse signal (figure 4 right) indicating that the pixel has received a hit. The block has a first differential stage (figure 3c), which feeds a comparator. Since the input of the discriminator is directly connected to the output of the

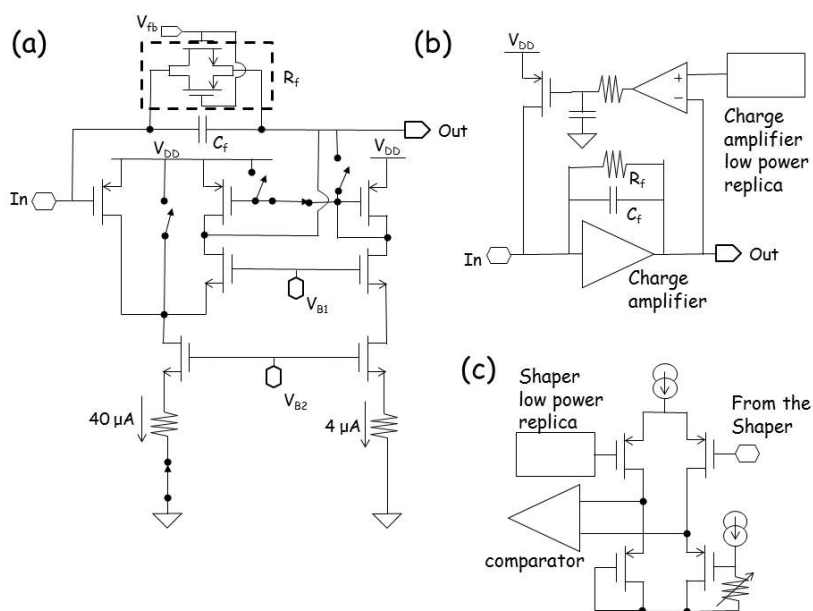


Figure 3. (a) Charge amplifier schematic. The state of the switches is shown for the amplifier enabled. They change state after a hit is received and they disable the charge amplifier until the beginning of the next frame. The dashed rectangle encloses the transistors which implement the feedback resistance. (b) Leakage current compensation circuit schematic. (c) Hit Flag comparator schematic.

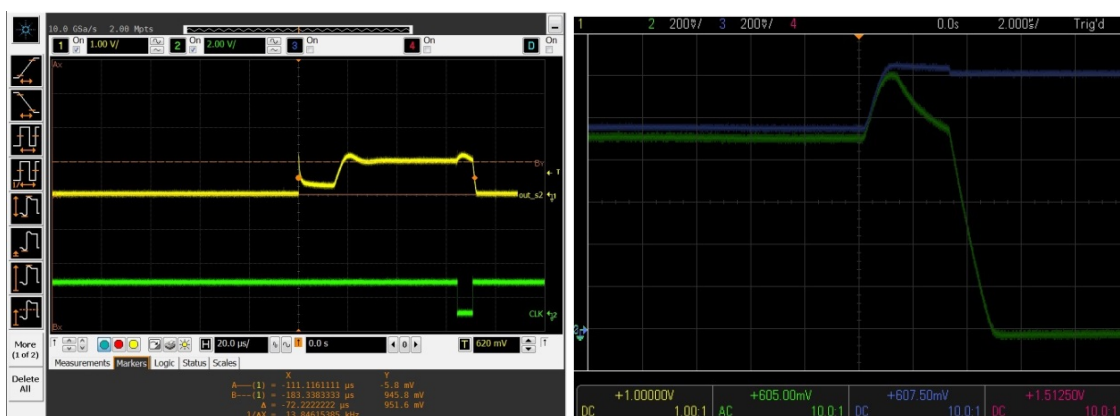


Figure 4. Left: oscilloscope picture of the shaper (yellow trace) and of the hit flag comparator (green trace). The scale of the vertical axis for the yellow trace is 1 V/div, for the green trace is 2 V/div and of the horizontal axis in 20 μ s/div. Right: oscilloscope picture of the shaper (green trace) and the peak detector (blue trace). When the hit flag is asserted the peak detector's output freezes and the shaper shuts down. The vertical axis scale for both traces is 200 mV/div and the horizontal axis scale is 2 μ s/div.

shaper, a circuit that produces the same quiescent voltage level as the shaper is essential. This block is a low power replica of the shaper. Thus, the differential input of the first stage of the discriminator is fed by the shaper output and by the output of its replica. The threshold of the discriminator (a few mV above the shaper quiescent voltage output) is set by the voltage drop produced by the flow

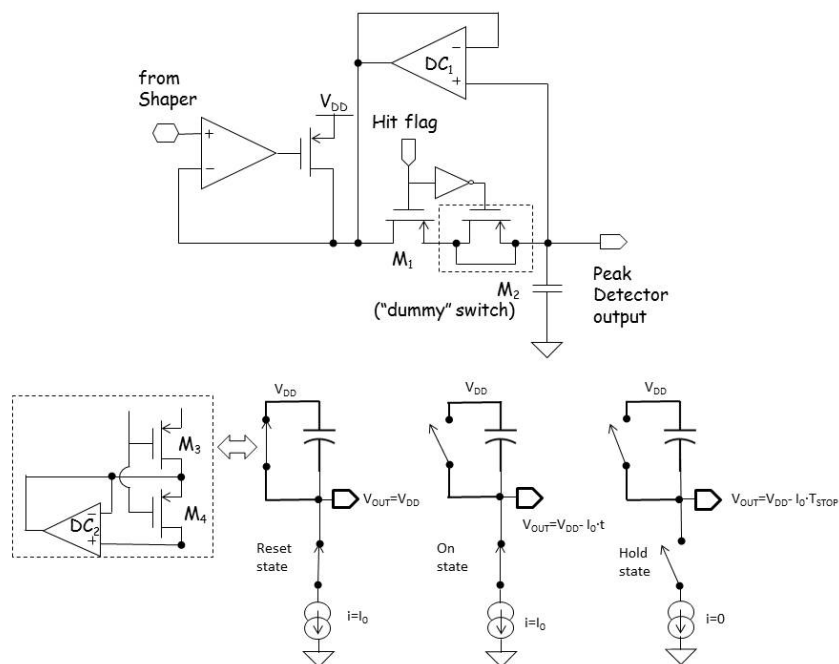


Figure 5. Top: peak detector schematic. M_1 , switch disconnects the capacitor from the operational amplifier which tracks the shaper output and buffer DC_1 assists leakage current minimization. Bottom: time to voltage simplified circuit. The sequence of operation phases is shown. The detail of the switch parallel to the capacitor is shown. The switch minimizes leakage current.

of a constant current into a digitally controlled resistor connected between the gate and the drain of the one of the loads of the differential stage. Three digital bits adjust the resistance value, thus offering an 8-level voltage trimming.

The other circuit which is directly connected to the shaper output is the peak detector. It consists of an operational amplifier in a negative feedback loop, which charges a capacitor with the aid of a PMOS device acting as a current source controlled by the operational amplifier output. When the capacitor has to be discharged the loop breaks, as the PMOS turns off. Leakage currents to ground from parasitic paths which reduce the voltage held by the capacitor are suppressed by putting two switches in series (M_1 and the dummy M_2 , shown in figure 5 top). When the capacitor is disconnected from the operational amplifier inverting input, buffer DC_1 does not allow a voltage difference between the inverting input of the operational amplifier and the capacitor. Figure 4 right depicts the operation of the peak detector and the freezing of the capacitor voltage at the moment the digital part of the pixel turns the switch off can be clearly seen (This happens when the hit flag is asserted).

The Time to Voltage converter (TVC) is activated by a control signal produced by the digital part of the pixel when the hit flag is asserted. It is implemented by a current sink which is connected in series to a capacitor when this signal comes. The capacitor plates are held initially at V_{DD} , but then the current sink starts discharging it and the voltage of the one plate ramps down. The different operation phases of the TVC can be seen in figure 5 bottom. Ideal current mirroring is achieved by an operational amplifier in buffer configuration which holds the drain of the current sinking transistor at the same voltage as the drain of the diode connected transistor of its biasing circuit.

The stop signal turns the capacitor to a “hold” state, but parasitic leakage paths can diminish the voltage held. Current leakage paths exist through the transistor switch parallel to the capacitor and through the current sink, although it has been deactivated by connecting to ground the gates of the NMOS biasing transistors. The leakage current through the path parallel to the capacitor is cancelled by implementing a switch with transistors M_3 and M_4 in series instead of one and by holding transistor’s M_4 source and drain terminals at equal potential with the aid of buffer DC_2 .

3.2 Pixel digital part

The digital part of the pixel contains the initial configuration registers, the hit identification and pixel selection logic, the analog part control logic and the Dynamic Random Access Memory (DRAM). Special care has been taken to assure that the writing of the memory is done after the valid presentation of a gray code word at its input, although the firing of the analog to digital conversion comparators occurs randomly within the conversion period. Sense amplifiers, whose circuits are presented in [15], are used for the readout of the DRAM bits. Hit identification is performed using wired OR logic. The hit flag comparator sets an S-R flip flop which pulls down the wired OR line of the row to which the pixel belongs. After the row selection by the embedded controller, the wired OR line of the column is pulled down. When the column is selected the S-R flip flop is reset. A simplified circuit diagram is shown in figure 2. The analog part control logic is triggered by the hit flag comparator and produces signals that start the operation of the time to voltage converter, control the shutdown of the pixel charge amplifier and shaper and produce the hold signal of the peak detector.

4 Embedded controller

The embedded controller contains: the multiplexer of the 25 columns data buses; two serial peripheral interfaces (one input for initial configuration data and another output of the pixel data); a 10 bit gray code counter for the pixel level A/D conversion; precharge circuitry for setting the lines which send the gray codes to the pixel array at predefined voltage levels before every transition and the controller core logic.

The controller core logic is a Mealy state machine used at all the operation phases except from the digitally quiet hit recording phase, during which no external clock is provided to the chip. It activates all the other entities of the controller and it is driven by 3 external inputs signaling the initialization, analog to digital conversion and data readout phases. Two priority encoders are used for the recognition of the pixels that have asserted their hit flags. At first the lowest row number having one or more hit flags set is selected and subsequently, within this row, the lowest column number having a hit is selected. Data of one hit pixel are transferred to the serialization circuit within one 100 ns clock cycle.

5 Sensor operation

In this section, we describe the details of the sensor operation. Its embedded controller is driven by external signals provided by a FPGA. According to their status the different operation phases are activated. Figure 6 depicts the operation sequence. The sensor works in snapshot mode. The frame

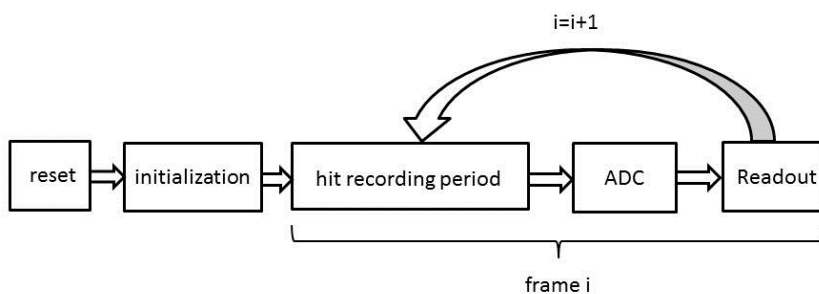


Figure 6. Operation sequence of the P4DI. The sensor operates in a snapshot fashion. During hit recording period every pixel registers the charge and the time of the first hit above threshold. After parallel digitization, the hit pixels are readout and a new frame starts.

period is adjustable depending on the duration of the hit recording phase and on the number of the hit pixels.

When initialization is activated, configuration data are sent to the sensor in a serial manner using a dedicated data line and one of the 3 clock lines provided to the chip. This phase lasts 17516 clock cycles of 100 ns. The 17500 are used for the initial configuration data of the pixel array (1250 pixels \times 14 bits) and 16 for global configuration settings.

Hit recording is enabled by a sequence of 3 external signals which activate the pixel circuits. This operation needs a time interval of 50–70 μ s. The last signal enables the hit flag production circuitry and marks the beginning of the hit recording time interval synchronously for all pixels. During this time all pixels are on and wait for a hit. If this occurs the hit pixel asserts a flag, produces the peak detector voltage level proportional to the charge collected and starts the time to voltage converter. During this phase no digital signal comes into or goes out from the pixel and the pixel array. The operation sequence is depicted in the oscilloscope pictures of figure 7.

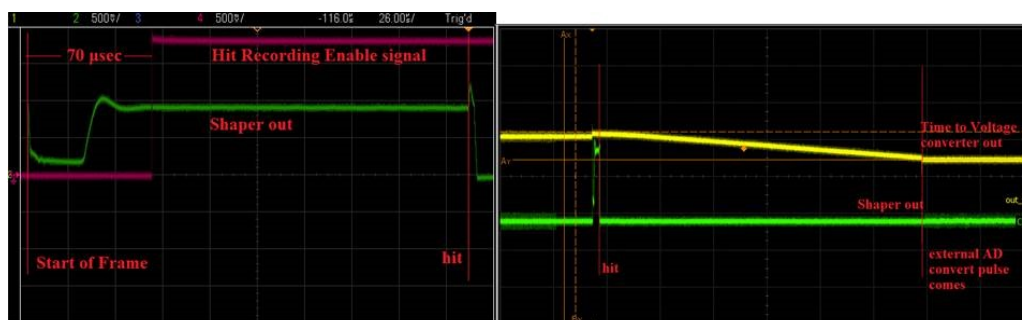


Figure 7. In-pixel signals recorded from a test pixel (row = 0, col = 0) whose internal nodes are buffered and brought to dedicated pads. Left: shaper output (green trace) and Hit Recording Enable (magenta trace) inserted to the chip from the FPGA. The start of the frame and the hit instant are labeled. Vertical axis for both traces is 500 mV/div and horizontal axis is 26 μ s/div. Right: the previous shaper signal (green trace) and the time to voltage converter (TVC) output (yellow trace). TVC ramps down until the external AD convert pulse comes. Vertical axis for the green trace is 500 mV/div, for the yellow trace is 1 V/div and the horizontal axis is 500 μ s/div.

After the hit recording an external signal stops the time to voltage converter and initiates pixel level analog to digital conversion. Two external analog ramps are fed into the chip to be used in the single slope analog to digital conversion together with two 10 MHz clocks with 90° phase difference between them. The clocks drive the gray code counter and the pre-charge circuits for the writing of the in-pixel DRAMs. The A/D conversion lasts 1024 10 MHz clock cycles.

Readout phase is initiated by an external signal too. During this phase the embedded controller selects the pixels that have asserted their hit flag and outputs the in-pixel stored data serially. The external controller should provide again the two 10 MHz clocks with 90° phase difference between them as well as a third clock with 100 MHz frequency. The two 10-bit words of in-pixel data are transferred to the periphery with 10 MHz frequency and there they are converted to 4 serial streams (energy, time, column address, row address) with the help of the 100 MHz clock.

The full pixel array can be read in 125 μs (provided all pixels have been hit). The analog to digital conversion which occurs in parallel for all hit pixels lasts 102.4 μs . Taking into account the set up time for one frame ($\leq 70 \mu\text{s}$) a hit recording time of 100 μs can be accommodated easily in a frame with total duration 400 μs . Thus 2500 hits/pixel/second can be recorded.

6 Test setup and characterization

The hybrid pixel sensor has been tested, characterized and demonstrated its functionality and performance. In the following, we briefly describe the test setup, present characterization results using test pulses and gamma sources as well as images acquired with the sensor.

Figure 8 shows the block diagram of the data acquisition system. The “Mother Board” based on the LX100/FG484 Xilinx FPGA and the CY7C68013 Cypress USB controller communicates through LVDS serial links with the “Daughter Board”. Piggy-back connected to the “Daughter Board” is the “Hybrid Board”. The “Hybrid Board” can house up to 8 hybrid sensors wire-bonded on it. The “Daughter Board” and the connected “Hybrid Board” compose one “Detection Layer”. The “Mother Board” can coordinate the operation of more than 10 “Detection Layers”. The “Daughter Board” is based on two LX9/CSG225 Xilinx FPGAs, each of them dedicated to control one bank of 4 hybrid sensors and transfer initialization/measurement data to/from them. Additional functionalities of the “Daughter board” are the generation of the ramp voltage which is provided to the chips for the in-pixel A/D conversion or A/D conversion of the analog data provided by the hybrids, when this functionality is not activated, as well as power supply of the hybrids. The setup is complemented by dedicated data acquisition and analysis software both on-line and off-line which evolves with data analysis tasks.

Data presented in this paper have been acquired by one detecting layer with 2 hybrids wire bonded on it. ACRORAD Al/CdTe/Pt Schottky type pixel detectors were used. Their thickness is 0.75 mm and they have been operated at 27°C with various bias voltages. During operation bias voltage is refreshed every 1000 frames.

In figure 9 one can see the detecting layer with the two hybrids and two metal objects (a screw and a nut placed 1.8 cm above them) and next to it a snapshot from the user interface of the data acquisition application which shows the “shadowgram” of these objects created by illuminating the setup with 37 MBq ^{241}Am placed at 3 cm above the metal objects. The image is created by measuring the total counts in every pixel. As a count is registered when the pulse amplitude exceeds

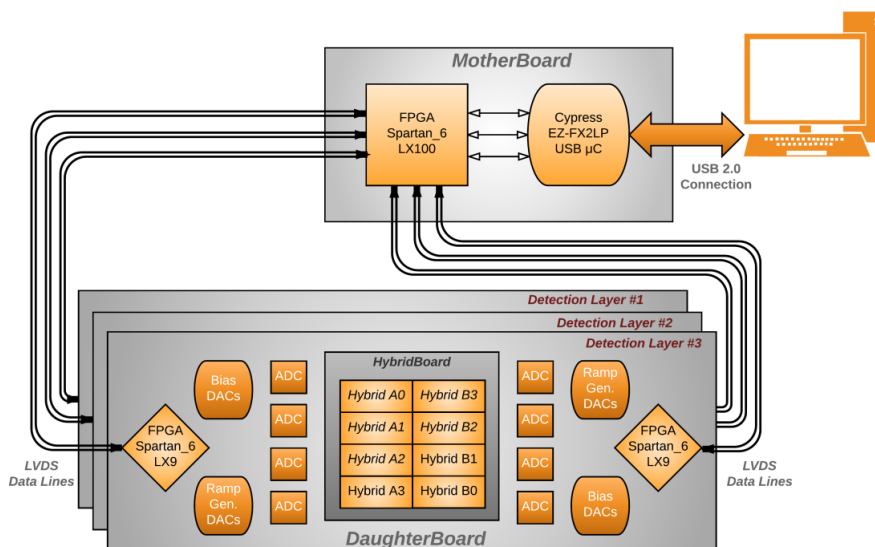


Figure 8. Sketch of the data acquisition system. It has been designed to accommodate multiple stacked detection layers. Each detection layer consists of 8 hybrids with total active surface of $4\text{ cm} \times 4\text{ cm}$ and 10000 pixels.

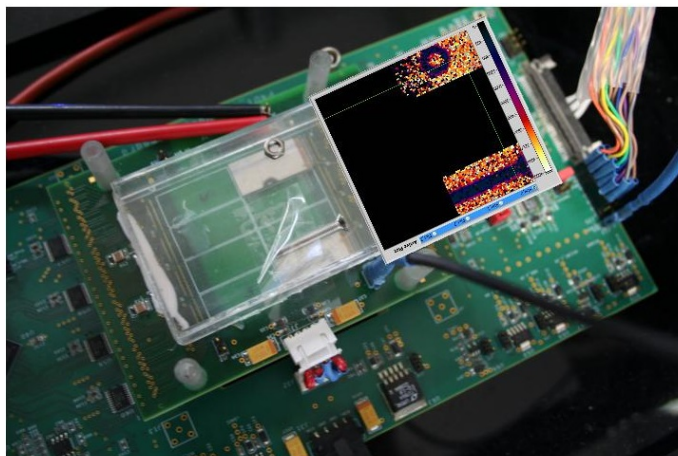


Figure 9. The shadowgrams of two metal objects superimposed on the picture of the experimental setup with the two objects. The hybrid board containing two hybrids is piggy-back connected on the daughter board. The hybrids are labeled A0 (with the screw on top) and A3 (with the nut).

the pixel amplifier baseline at least by 25 mV and by taking into account that low noise should be expected and that this is the case indeed, as one can see in figures 10 and 11, there is no need to limit the energy range of the counts which are considered for image formation. In other implementations (e.g. see [16]), one should calibrate in energy and afterwards define an energy range in order to be able to acquire images.

The energy calibration for a certain gain setting was done by recording the voltage value of two distinct photopeaks in order to construct a linear relation between volts and keV using these two

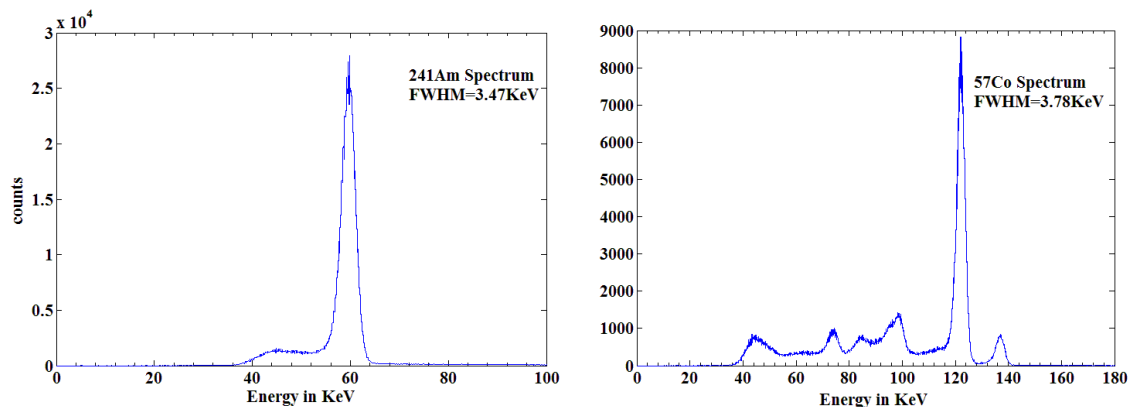


Figure 10. Cumulative spectra from all pixels of hybrid A0 obtained by irradiating with ^{241}Am (370 MBq) and ^{57}Co (2.035 MBq) sources placed 1.7 cm above the hybrid at 23°C. 1000 frames were collected. -500 V bias, 3 ms hit recording period and $3\ \mu\text{s}$ shaping time were applied.

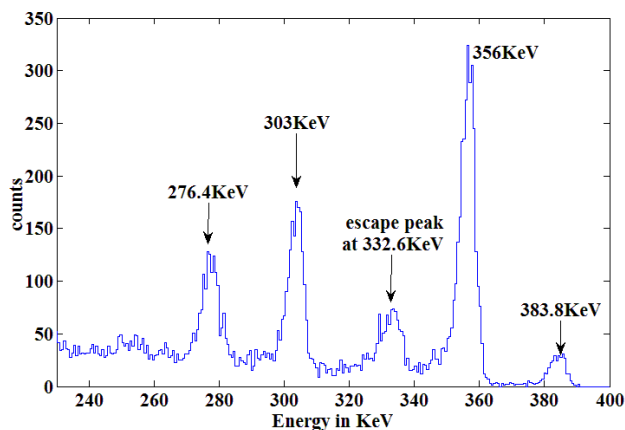


Figure 11. ^{133}Ba (6.549 MBq) spectrum recorded in pixel (row = 11, col = 9) of hybrid A3 at 23°C. The source was placed 1.7 cm above the hybrid. -500 V bias, 3 ms hit recording period and $1.8\ \mu\text{s}$ shaping time were applied.

points. This procedure was repeated for every pixel. Figure 10 shows the spectrum constructed by calibrating all pixels and then adding the counts in every energy bin from all pixels in one histogram. Figure 11 shows a pixel spectrum obtained by irradiating the hybrid with ^{133}Ba . The FWHM for the photopeaks shown is from 4.74 keV up to 5.74 keV and 7.32 keV for the escape peak.

Figure 12(a) shows the linear relation between the voltage output of the TVC at the end of the hit recording period and the time elapsed since the beginning of the hit recording for one pixel. The relation is linear but the slope varies from pixel to pixel. For this reason time calibration for every pixel was performed by using two pulses injected at known time instants within the hit recording period in a way analogous to the energy calibration. Figure 12(b) shows the distribution of the recorded time interval values for a pulse supposed to occur always at the same instant within 3 ms hit recording period. The experiment was repeated for 600 frames.

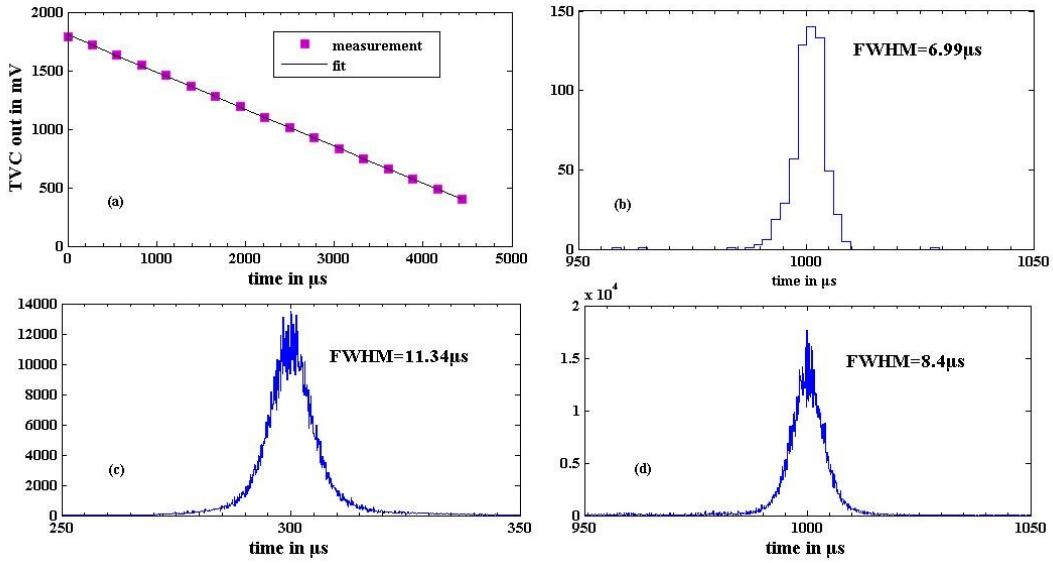


Figure 12. (a) The time to voltage converter (TVC) output at the end of the hit recording period of one frame as a function of the time of the hit occurrence measured from the start of the hit recording period. (b) Distribution of the hit time stamp for one pixel for 600 frames. (c) Cumulative distribution of the time stamp for the pixels of both hybrids for a hit occurred at $300 \mu\text{s}$. (d) The same distribution for a hit occurred at $1000 \mu\text{s}$.

The FWHM of the distribution is a measure of the time resolution capability of one pixel but one could take as system time resolution the FWHM of the distribution constructed by adding the histograms from all the pixels. This is presented in figures 12(c),(d) for all the pixels of the two hybrids. The FWHM is $11.34 \mu\text{s}$ at $300 \mu\text{s}$ and $8.4 \mu\text{s}$ at $1000 \mu\text{s}$, again measured from the start of a 3 ms hit recording period and repeated for 600 frames.

Figure 13 presents the time stamp-energy scatter plot of hits recorded by a pixel with ^{241}Am source. The reduction in the number of counts in high time stamps is artificial due to a cut imposed by the data acquisition program to events recorded in pixels whose TVC output exhibits a nonlinear behavior between 1.5–1.6 V. The reason for this non-linearity has not been resolved yet.

The noise map of hybrid A0 is shown in figure 14 for the highest gain setting. The mean of the equivalent noise charge (ENC) distribution is 255 electrons (rms). Mean ENC equal to 410 electrons has been measured for the lowest gain setting. For the measurement, 10000 pulses with amplitude 41 mV and 84 mV were injected into the test input of the chip. These amplitudes deliver to the in-pixel test capacitors almost the same charge as photons with energies of 60 keV and 122 keV respectively. The output data from every pixel were put in a histogram and a Gaussian curve was fitted to them. The standard deviation was divided by the gain of the pixel.

For fixed total input capacitance, which is the case when a pixel detector with certain thickness is bump bonded to the readout integrated circuit, shaping time is optimized to equalize the contributions of the thermal noise of the preamplifier input FET and the current noise of the preamplifier feedback circuit and the detector leakage, provided all other noise sources are negligible. However other considerations may prevail, such as power consumption minimization and time required for charge collection. Consequently noise optimization was achieved using Monte Carlo variation of

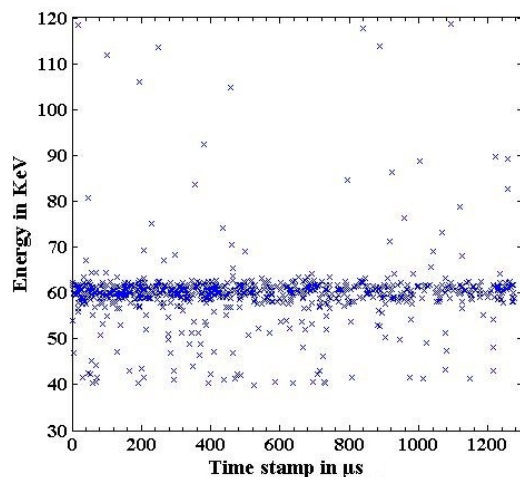


Figure 13. A scatter plot of valid events with respect to energy and event time recorded in pixel (row = 30, col = 2) in hybrid A0 when the hybrid was exposed to photons from ^{241}Am .

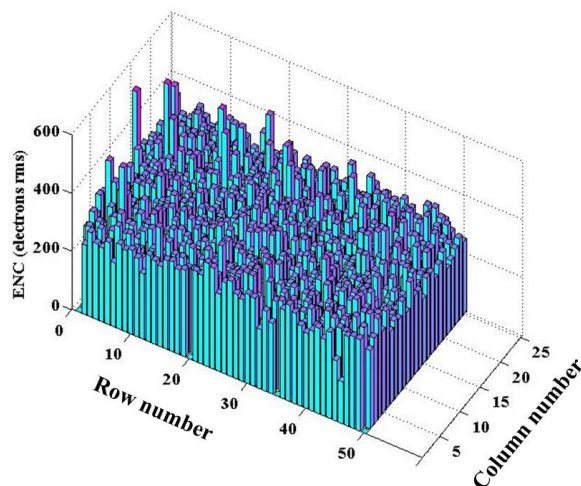


Figure 14. Noise map of hybrid A0 for the highest gain setting (shaping time $3\ \mu\text{s}$) with detector bias at $-500\ \text{V}$.

transistor sizes and bias points of the charge amplifier, by taking into account certain constraints [12]: (a) Pixel capacitance of a CdTe detector with $350\ \mu\text{m} \times 350\ \mu\text{m}$ pixel size, $400\ \mu\text{m}$ pixel pitch and 2 mm thickness was estimated using method of [17] implemented in the commercial 3-D simulator SENTAURUS SDEVICE by SYNOPSIS [18]. When the ASIC is bump bonded to the detector its top metal layers come close to the detector pixel (a distance of $15\ \mu\text{m}$ between the detector and the ASIC was assumed). This results in a charge redistribution which affects the capacitance dramatically. The effect was simulated too and the capacitance was found 6 times larger than without taking it into account. A 600 fF total input capacitance was calculated. (b) The maximum charge collection time was estimated again with the aid of transient simulations using SENTAURUS SDEVICE. A

gamma ray photon interacted just below the surface of the single Indium electrode and delivered 6 fC initial charge. The charge collection time in that case was 500 ns and it was considered lower than the real one, because defects which limit the carriers lifetime were not included in the model. For this reason programmable peaking time higher than 500 ns was implemented.

7 Conclusions

A hybrid pixel sensor implemented using a standard mixed signal CMOS 0.18 μm process and CdTe Schottky diode detector 0.75 mm thick bump bonded on it was described. The CMOS ASIC combines a rich set of features with prominent the simultaneous determination of the energy and of the time of occurrence of the recorded hits at a low power budget. Configurable gain settings allow its use in high and low gain tailored to the application. Pixel reset, integration, and A/D conversion occur in full frame parallel “snap-shot” fashion. Sparse data scan has been implemented and the readout is performed with serial links at 100 MHz. The 1250 pixel chip consumes less than 100 mW and can handle 2500 hits/pixel/sec.

The hybrid does not count the number of photons in a given time interval, but it measures the time until a hit is detected. It can be easily shown that due to the memoryless property of the Poisson process involved, the average of these times is an unbiased estimator of the mean hit rate. Thus the radiation field strength can be deduced with precision depending on the sample size used for the estimation.

The measured energy resolution in the 300 keV to 400 keV range implies that, if used in a Compton imager detecting layer, corresponds to less than 5° FWHM of the Angular Resolution Measure [9] in this energy range. The energy resolution achieved from all pixels was measured without any particular precaution, not even shielding in a metal box and at room temperature. It is comparable to the resolution reported in [10] for the best pixels and at -10°C .

The timing resolution is mediocre and prevents time of flight measurements. Nevertheless it permits enriching the samples used in the reconstruction of the Compton sequence with the aid of heuristic algorithms [19, 20] which deduce the correct Compton sequence with the aid of position and energy information. This coarse time resolution may prove beneficial for handheld Compton imagers, where computational resources are limited and the dimensions make difficult the use of time of flight.

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