CMS Phase-2 Inner Tracker Upgrade

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Abstract. The HL-LHC conditions of instantaneous peak luminosity up to 7.5×10^{34} $cm^{-2}s^{-1}$ and an integrated luminosity of the order of 300 fb^{-1}/year is expected to result in 1 MeV neutron equivalent fluence of 2.3×10^{16} n_{eq}/cm^2 and a total ionizing dose (TID) of 12 MGy (1.2 Grad) at the center of the CMS Experiment, where its innermost component, the Phase-2 Pixel Detector will be installed. This detector has to survive the above radiation dose, handle hit rates of 3.2 GHz/cm^2 in the layers closest to the beam line, be able to track and separate particles in extremely dense collisions, deal with a pileup of 140-200 collisions per bunch crossing and have a high impact parameter resolution. This translates into a highly granular detector design with thinner sensors and smaller pixels, and a faster and more radiation hard electronics compared to the Phase-1 detector. This contribution reviews the Phase-2 upgrade of the (silicon-based) CMS Inner Tracker focusing on the features of the detector layout and on developments of pixelated devices.

KEYWORDS: **HL-LHC, tracking, detectors, silicon, pixel**

1. Experimental Conditions and Requirements

A completely new Tracker will be built for the HL-LHC [1] Phase-2 upgrade [2,3,4] of the CMS Experiment [5]. Its goal is to maintain or even improve the tracking performance compared to the Phase-1 detector [6]. Made of hybrid silicon modules it is divided into two parts - the Outer Tracker (OT), based on silicon strips and macro-pixels, and the Inner Tracker (IT) based on pixelated sensors. The IT is required to withstand up to 1.2 Grad of Total Ionizing Dose (TID) and 1 MeV neutron equivalent fluence of up to 2.3×10^{16} n_{eq}/cm^2. It must also cope with hit rates of up to 3.2 GHz/cm^2 (Phase-1 value is 0.58 $GHz/cm^{-2)}$) for the innermost layer, have a trigger latency of 12.8 µs (Phase-1 value is 3.2 μs) and deal with a trigger rate of 750 kHz (Phase-1 value is 100 kHz). These requirements pose significant challenges for its design to meet the required physics goals. In addition, it also has an increased $|\eta|$ coverage of up to 4.0 to improve the missing E_T resolution and particle-flow event reconstruction by providing transverse momentum measurements and trajectories for charged particles entering the calorimeters. Improved missing E_T resolution is the key to BSM physics searches looking for exotic particles, dark matter, and extra dimension models, where particles escape the detector undetected. The smaller pixel size improves b-tagging as well as hadronic tau quark and track reconstruction efficiencies within boosted jets, which can be produced from new heavy objects decaying to Higgs, Z bosons, or top quarks – all heavy probes that can be exploited for new physics searches. The resulting design and layout of the detector and its components like sensors, readout chip, electronics, cooling, and other services are briefly described in this paper.

2. Detector Layout

The layout of IT is shown in Fig.1. It has a total silicon sensor area of 4.9 m^2 and is designed for ease of insertion and removal. It occupies a region with radius < 200 mm and is instrumented with about 4000 high granularity silicon pixel modules. These modules are of two types: 1x2 readout-chip and 2x2 readout-chip, shown in Fig. 1 with green and orange colours, respectively. They carry a total of 2 billion pixels for an efficient pattern recognition in the high track density environment of the HL-LHC.

The IT extends roughly from –265 cm to +265 cm in z which is the direction along the beam line. The beam pipe has a diameter of 45 mm. There are two envelopes of the IT. The first envelope starts just outside the beam pipe and has an inner radius of about 29 mm and extends up to |z| ~ 150 cm. The other envelope has an inner radius of about 64 mm and lies between |z| ~ 150 cm and |z| ~ 265 cm on either side of the first envelope giving a coverage of |η| ~ 4. The IT is divided into a Barrel (TBPX), Forward (TFPX) and Endcaps (TEPX) sub detectors as shown in Fig. 1. The TBPX consists of four layers with 9 modules per ladder with no gap at pseudorapidity |η|=0. It is flanked by the TFPX made of 8 small double-discs with 4 rings of modules per disc and the TEPX made of 4 large double-discs with 5 rings of modules per disc.

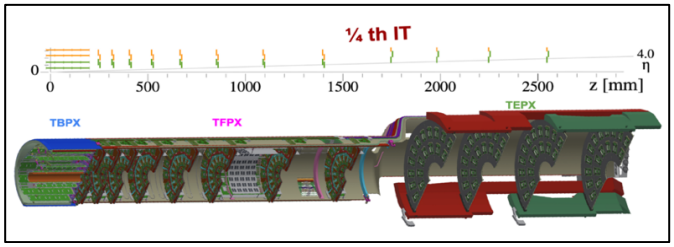

Figure 1: Layout (above) and cutout (below) of 1/4th of IT.

In TBPX, the pixel modules are arranged in “ladders” with neighbouring ladders in each layer mounted staggered in radius to have an overlap in r-ϕ. Each ladder carries 4 or 5 modules, and these do not overlap in z. In TFPX and TEPX the modules are arranged in concentric rings. Each double-disc is made of two discs with modules mounted on each of the four planes. The module overlaps in r and ϕ. Each disc is split into two halves, and these D-shaped structures are referred to as “Dees”. The innermost ring of the last TEPX disc is dedicated to the measurement of the bunch-by-bunch luminosity. The detector features a lightweight mechanical structure that is made from carbon fibre to reduce the material budget to avoid degradation of the tracking performance due to the interactions of particles with the detector material. Support structures and cooling pipes are shared among modules. A low mass two-phase CO_2 evaporative cooling is used to remove the heat and keep the sensors below -20 ^{0}C. The modules are a hybrid type where the sensors are bump bonded to a set of either two or four Read Out Chips (ROCs). The ROCs are wire-bonded to a flexible printed circuit board called High-Density Interconnect (HDI) that is populated with passive components and connectors. The HDI distributes low voltage to power the ROCs, high voltage to bias the sensor, as well as clock and control signals and routes the data from the chips. The modules connect via electrical links (or e-links) to optoelectronic service cards called the Portcards. The Portcards [7] are positioned around the support cylinder for the TBPX and on “Dee” structures for TFPX and TEPX.

The IT is designed to be installable after the OT and the beampipe are already in place. This enables the possibility to replace, radiation degraded or otherwise, parts of IT quickly and easily during a shutdown period of the data taking and detector maintenance.

3. Expected Performance

The IT features a reduced material budget, despite 2 billion readout channels, achieved using light weight carbon fiber material for mechanical support, low-mass CO2 cooling, a very first-time use of

serial powering in any HEP detector and an optimized routing of the services. This is essential to achieve the required accuracy in the transverse momentum of the tracks and reduction in fake tracks despite a high pile up environment. The optimal planning of the material budget is reflected in the improved expected performance as shown in Fig. 2 where p_T resolution and longitudinal impact parameter resolution are shown comparing the Phase-1 and Phase-2 detector. The beneficial design features lead to a better performance of the IT with extended η coverage and under higher pileup conditions compared to the Phase-1 detector.

4. Sensor, Readout Chip and Modules

The two types of modules [8] for the IT are shown in Fig. 3. The stringent requirements for a low material budget, high hit rates and high efficiency and resolution for tracking are met by using detector elements that are highly granular and radiation hard. Therefore, thin planar silicon sensors with small pixels are the choice. These pixels with a compatible bump bond pattern come in two flavors, a rectangular (25×100 μm^2) or a square (50×50 μm^2), as shown in Fig. 4.

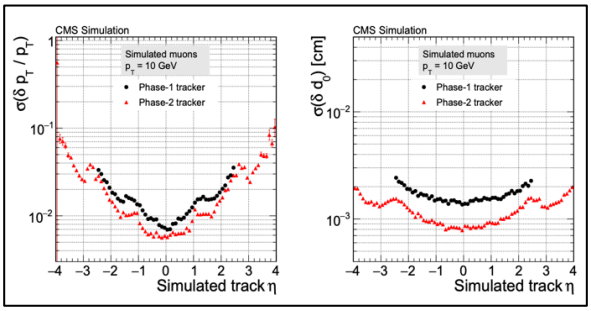

Figure 2: The resolution of the transverse momentum (left) and the transverse impact parameter (right) as a function of η compared to the Phase-1 detector is shown. Note that the η range for Phase-2 extends beyond the one of Phase-1 detector.

They have an area one-sixth of the Phase-1 pixel size (100x150 μm^2). Unlike the present n-in-n type sensors an n-in-p sensor technology is chosen. No double-sided processing is needed for the n-in-p type making it easier and more cost effective. The homogeneous back plane allows easier mounting of sensors and thinning of wafers to reduce the material budget. A spark protection between the ROC and sensor structure is required due to the presence of a high voltage for sensor bias in the proximity of the sensor edge. This voltage can go up to 1000 V as sensors accumulate radiation dose over time. Solutions have been developed and demonstrated to offer good protection up to more than 1000V. For the inner layers the 3D silicon sensor technology is also considered that has the advantage of better radiation hardness and lower bias voltages. However, 3D sensors have a larger pixel capacitance, are more expensive and have a lower production yield due a complex fabrication process. Both, planar and 3D sensors single chip assemblies, non-irradiated and irradiated, are currently being studied extensively in test beams [9] to measure charge collection efficiency and position resolution.

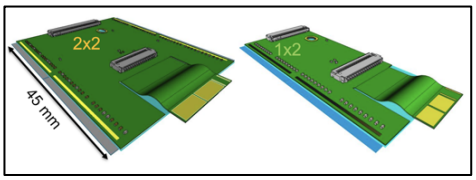

Figure 3: A sketch of a 2x2 and a 1x2 readout chip module.

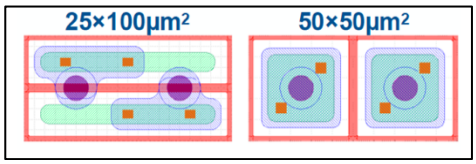

Figure 4: 25×100 μm^2 and 50×50 μm^2 pixel cell layout.

The ROC to read out signals from the sensor is being developed in 65 nm CMOS technology by the RD53 Collaboration [10,11], a joint effort between the ATLAS and CMS collaborations. This ROC must have a low threshold (1000 electrons), low noise, low power consumption at high hit rates, be able to sustain high hit rate, have high trigger rate capabilities and be sufficiently radiation hard. The option of replacing the innermost layers of the detector eases the radiation tolerance requirements with respect to the total radiation dose received over the lifetime of the IT. A first half-size prototype ROC, called RD53A [12,13,14], was used to test prototype HDI designs, prototype rails to mount modules, thermal grease for heat transfer, module (sensor + ROC) assembly, parylene coating for spark protection, system tests and quality control procedures. Some of the tested assemblies were irradiated to a fluence of ~10^{16} n^{eq}/cm^2. The improved version of this ROC is called RD53B-CMS (also called CROC) [15,16]. It is the CMS final version of the chip and has a linear front-end [15]. The ATLAS version is called RD53B-ATLAS and has a differential frontend. The choice of differential front-end by ATLAS is driven by its excellent noise occupancy performance even at rather low current consumption. CMS chose the linear front-end as the lowest risk option to integrate into the production chips, its ability to provide a fast preamplifier return to baseline with some margin in target discharge rate and being able to cope well with large detector leakage currents. These ROCs are being submitted for production at the time of writing of this paper after several bugs fixes compared to RD53A. The final CROC version is expected to be submitted next year.

5. Power Architecture

Higher granularity and long latency requirements lead to an increased power consumption by the ROCs. The use of the deep sub-micron CMOS technology and an efficient power architecture with a low supply voltage (1.2 V) demands a significant current level of about 2 A per ROC. In the serial power distribution design [17,18], a group of pixel channels share digital resources for buffering, control, and data formatting. The modules are powered in about 500 serial chains of up to 12 modules each. The ROCs share a constant input current and generate the necessary operational voltage themselves. The current flowing through the chain is used by each module and passed on to the next one. As the voltage is generated locally on the ROC, no auxiliary on-detector electronics are needed for powering the pixel modules. In this way only one supply line is needed per chain, leading to a reduction in the number of wires needed. The traditional powering scheme of supplying several modules in parallel would have led to an unacceptable amount of material budget coming from cable mass itself and significant power losses over the long supply lines (~ 40-60 m). The serial power scheme is current driven and is less sensitive to voltage drops on the supply cables and between modules, allowing the use of thin wires. Each module is exposed to a different voltage and therefore has a different local ground that needs to be electrically isolated from the other modules. All elements in a chain receive the same current and the voltage is equally shared if all elements represent the same and constant load. This is made possible due to the Shunt-LDO (Low Dropout) implementation in the readout chip that combines a linear regulator and a shunt. Within a module, chips are connected in parallel, sharing the incoming current. In addition, power is needed for the Portcards that hosts two LpGBT transceivers and two VTRx+ optical links for bidirectional data transfer. The Portcard is powered by a DC-DC convertor that is hosted on it. Power is also needed for pre-heaters (~ 350 in number) for the cooling system to mitigate CO_2 superheating.

6. Readout Chain

The length of the e-links (connecting modules to Portcards) is up to 1.6 m. A total of six 1.28 Gb/s up stream e-links per module are implemented for data from L1 trigger accept and monitoring information to the DAQ and control system. One 160 Mb/s downstream elink is used to bring clock, trigger, fast commands, and configuration data to the module. The LpGBT chip serializes/deserializes data to/from the modules while VTRx+ optoelectronic [18] converts the electrical to optical data with 10 Gbps rate and receives the commands from the back-end boards at 5 Gbps. The Portcards are limited to a fluence of $5x10^{15}$ n_{eq}/cm^2 (~100 Mrad). About 750 Portcards, 7k e-links for readout and 4k e-links for control signals are needed for the IT. A dedicated IT Data Acquisition (DAQ) Interface board, called DTC (Data

Trigger Control) receives the data from the front end. These boards host high bandwidth processors and receive hits pertaining to triggered events and send them to the CMS central DAQ system. It also controls, monitors the health, and calibrates the detector modules. The DTC boards conform to the ATCA standard and are located in the service cavern. A total of 28 DTC boards are needed for the entire IT. Dedicated boards and crates will be used for the luminosity and background measurements in the TEPX.

7. Summary

The upgraded CMS Tracker is an extremely challenging and ambitious project. It has been designed to cope with higher radiation level and pile-up (higher granularity, larger bandwidth), extended forward coverage ($|\eta|= 4$) and have a decreased material budget. It also includes luminosity measuring components. It uses CO_2 cooling, light structures to minimize material budget and a novel method of serial powering. The R&D is well into the prototyping phase. The demonstrator RD53A readout chip has been tested for full functionality. Power and readout tests have been performed with RD53A modules in serial power chains and readout via prototype e-links. The final CMS pixel read out chip submission is planned for the next year. Test beam characterization of prototype modules with thin planar sensors and 3D sensors, both non-irradiated and irradiated, bump bonded to RD53A is ongoing.

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