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# SPACIROC: A Front-End Readout ASIC for JEM-EUSO cosmic ray observatory

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**Abstract**

The SPACIROC ASIC is designed for the JEM-EUSO fluorescence imaging telescope onboard of the International Space Station. Its goal is the detection of Giant Air Shower above a few 10^19 eV, developing at a distance of about 400 km, downward in the troposphere. From such distance, most of the time, the number of the photons expected in the pixels is very weak, ranging from a few units to a few tens. For such running conditions, we propose a low-power, rad-hard ASIC which is intended for reading out a 64-channel Multi-Anode Photomultiplier. The two main features of this ASIC are the photon counting mode for each input and the charge-to-time (Q-to-T) conversions for the multiplexed channels. In the photon counting mode, the 100% triggering efficiency is achieved for 50 fC input charges. For the Q-to-T converter, the ASIC requires a minimum input of 2 pC. The working conditions of JEM-EUSO require the ASIC to have a low power dissipation which is around 1mW/channel. The design of SPACIROC and the test results are presented in this paper. SPACIROC is a result of the collaboration between OMEGA/LAL-Orsay, France, RIKEN, ISAS/JAXA and Konan University, Japan on behalf of the JEM-EUSO consortium.

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## 1. Introduction

The primary purpose of JEM-EUSO [1] mission is the detection of the Extensive Air Showers (EAS) created by the Extreme Energy Cosmic Rays (EECR $>10^{19}$ eV), inside the atmosphere. JEM-EUSO, which is a fluorescence telescope, looking downward, that should be installed on the JEM module of the International Space Station, will detect the fluorescent photons released by the EAS. By observing these phenomena from the upper side of the atmosphere, this telescope will be able to identify the EECR.

SPACIROC (Spatial Photomultiplier Array Counting and Integrating Readout Chip) was designed according to the requirements from the JEM-EUSO consortium. Multi-anode photomultipliers (MAPMT) are proposed to be the sensitive device of the JEM-EUSO observatory focal surface. SPACIROC [2] was designed to accommodate the readout of these MAPMTs. As JEM-EUSO is intended to track the fluorescent light, this ASIC is required to count the number of photons reaching each pixel of the MAPMTs. The secondary mission of SPACIROC is to measure the intensity of photon flux by performing charge to time (Q-to-T) conversion. The final dimensions of the ASIC are 4.6 mm x 4.1 mm (19mm²) and it was submitted to the foundry in March 2010. The chip was developed using the 0.35µm SiGe BiCMOS process from AMS.

## 2. The ASIC

SPACIROC offers 64 inputs dedicated to the anodes of one MAPMT and 1 input for the last dynode. For the following, the MAPMT gain is assumed to be $10^6$ in order to have 1 photoelectron (1 p.e.) around 160 fC.

### *2.1. Specifications*

The specifications for the chip are the following:

- 64 channels preamplifier with independent gain (8-bit) adjustment.
- Photon Counting : 64 channels.
- Q-to-T converter : 1 channel for last dynode + 8 internal channels (multiplexed inputs).
- 100% trigger efficiency for charge greater than 50 fC (~1/3 p.e.).
- Q-to-T converter input range: 2 pC – 200 pC (12.5 p.e – 1250 p.e.).
- Power consumption : ~1 mW/channel.
- 9 data serial outputs.

This circuit was designed for low-power spaceflight applications. SPACIROC is also radiation hardened by design against Single Event Latchup (SEL) and Single Event Upset (SEU).

### *2.2. Architecture*

The general architecture of SPACIROC could be divided into 3 main blocks: the Photon Counting, the Q-to-T converter (called KI) and the digital part. The Photon Counting and KI are the analog section of

this ASIC. The digital part of SPACIROC is used to count photon triggered pulses and to measure the photon intensity. The readout management is also implemented in the digital part. The final layout and the architecture of SPACIROC are represented in Fig 1(a) and Fig 1(b) respectively. However Fig 1(b) doesn't include the auxiliary components of the ASIC such as the bandgap reference, DACs and signals monitoring.

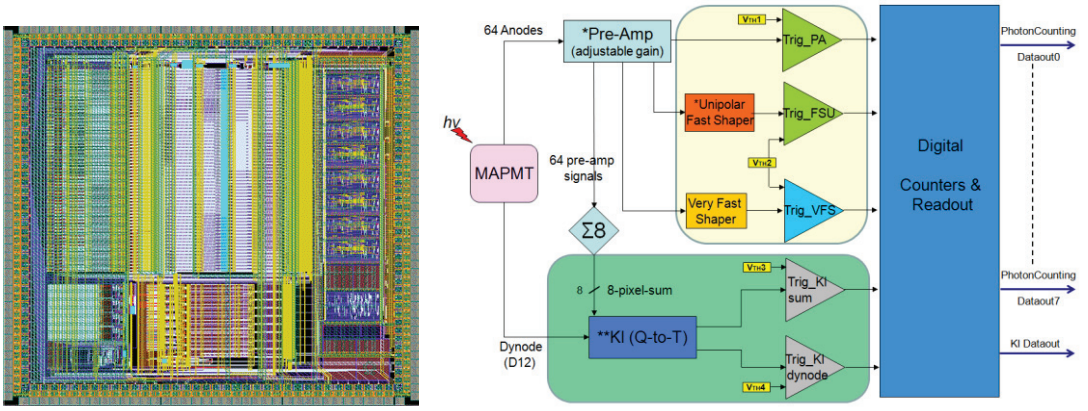


Fig. 1. (a) SPACIROC layout; (b) SPACIROC general architecture

The 64 signals from MAPMT anodes are fed through the preamplifiers which offer adjustable gain to correct the gain non-uniformity of the MAMPT. The preamplified signals are fed to the Photon Counting and KI in order to transform these signals into discriminator pulses. These discriminator pulses will be made available at the inputs of the digital part for counting and measuring. Each mentioned block will be described in the following sections. The use of the word "trigger(s)" in the next sections will refer to the Photon triggered pulses on the outputs of the analog part.

## 3. Analog Design

### *3.1. Photon Counting*

The 64-channel Photon Counting block is required to discriminate the preamplifier signal into trigger pulses. For this prototype, the ASIC offers three different discriminator outputs (Trig_PA,Trig_FSU and Trig_VFS) for each channel. The reason of having three different discriminators is to verify the performances of each triggering scheme under laboratory tests before choosing the design which represents the best trade-off between noise, speed and power consumption. Fig 2 shows the block diagram of the Photon Counting analog part.

The output for the first trigger design, which is called Trig_PA, is obtained from the preamplifier signal which is fed directly into a discriminator. Due to its simple architecture (a preamplifier and a discriminator), this design has the lowest power consumptions compared to the other trigger designs in the Photon Counting part.

For the next two trigger designs (Trig_FSU and Trig_VFS), the preamplifier signal is fed to shapers before reaching the discriminators. The shapers will add more gain to the preamplifier signal. As for the second trigger design, Trig_FSU, a low-noise with adjustable-gain shaper called FSU from MAROC3 [3] chip is used. The output pulse of the Trig_FSU is obtained by comparing the FSU signal to a fixed threshold.

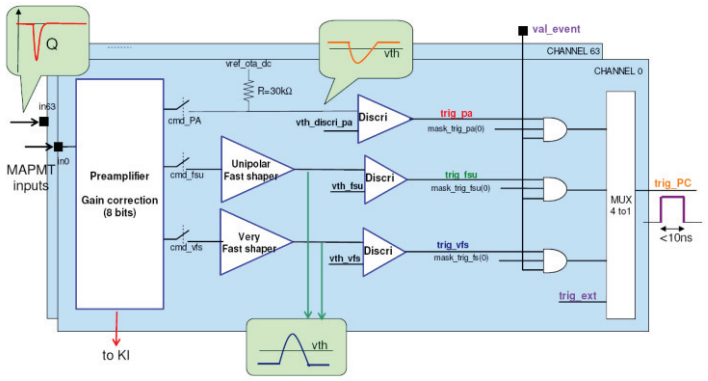


Fig. 2. Photon Counting architecture

For the last trigger design, Trig_VFS, a shaper is also used here. The shaper, which is known as VFS, has a larger gain and a faster shaping time compared to the FSU shaper. The output signal this design is obtained by discriminating the VFS signal.

These three discriminator outputs are sent to the digital block via a 4-to-1 analog multiplexer. The fourth input of the multiplexer is for the external trigger signal which is used to test the digital block independently.

Two 10-bit DACs are used in this block. One DAC is shared between Trig_FSU and Trig_VFS trigger designs as both designs will discriminate signals that have the same polarity and baseline. The other DAC is used for setting threshold in the Trig_PA trigger design because of the inverted polarity of the preamplifier signal at the discriminator input. Each trigger output could be masked independently as only one trigger could be used at one time.

### *3.2. KI*

Another important feature of this ASIC is the ability to perform the Charge to Time (Q-to-T) conversion by measuring the signal duration over a fixed threshold. Q-to-T conversion is done by the 9-channel KI block. The first 8 inputs of the KI converters receive the pre-amplified signals of the MAPMT anodes. The pre-amplified signals are reorganised into the sum of every 8 neighbouring channels or pixels; hence the given name of 8-pixel-sum for this part. However, the 9th input of KI takes a signal coming directly from the dynode of the MAPMT. The gathered data on the dynode could be used for the MAPMT protection strategy (gain reduction against high photon flux) in the JEM-EUSO experiment. Fig 3 shows the general architecture of this converter.

An impedance converter (Impedance Conversion) and a capacitive network (Dynamic Range) are used to transform the input current pulse into a voltage signal. The Impedance Conversion circuit will convert the low impedance input (~50Ω) of the KI part into higher impedance. The Dynamic Range circuit is used to scale the input dynamic range. The scaling is done via the ASIC configuration parameters in order to obtain the appropriate capacitance value for integrating the input signal. If the input signal is strong enough, it will produce a discriminator output, which in turn will deactivate the DC Feedback baseline and activate a variable gain current source (Current Sink). Once the current source takes over, the integrated signal length can be adjusted according to the selected current value. The 9-channel discriminator outputs can be masked individually or all at once. It is also possible to use external inputs for testing the digital part independently. This converter was designed in collaboration with RIKEN, Japan. The design is based on their KI02/03[4] chip.

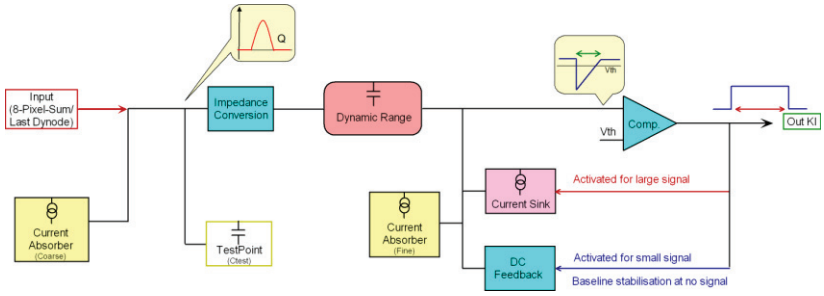


Fig. 3. KI architecture

### *3.3. Simulation results*

The analog part of Photon Counting and KI were fully simulated. Fig 4 shows the simulations for the Photon Counting block. The injected charge are 1/3 p.e, 1 p.e and 10 p.e. The simulations results indicate that Photon Counting block could achieve 100% trigger efficiency starting from 1/3 p.e. The Fig 5 shows the simulations results of the KI block for the summed channels and the MAPMT dynode pulses. For the simulations, charges ranging from 15p.e. to 1500p.e. are injected into input of KI dynode and 100p.e. – 1500p.e. are injected into the KI 8-pixel-sum inputs. The expected trigger widths could vary up to 2970 ns.

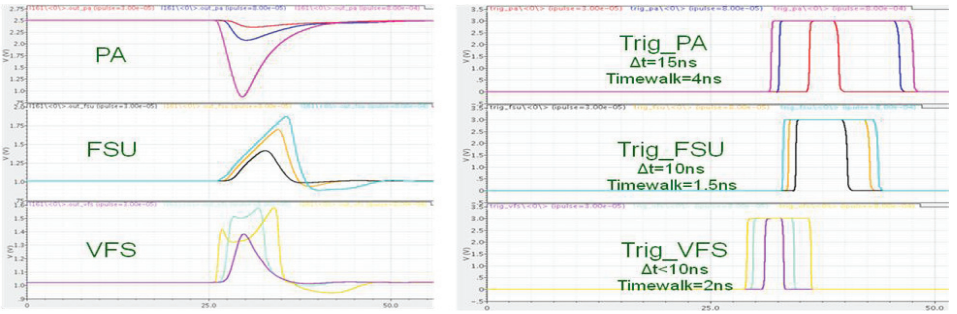


Fig. 4. Photon Counting simulations (a) Analog signals; (b) Triggers (discriminators) outputs

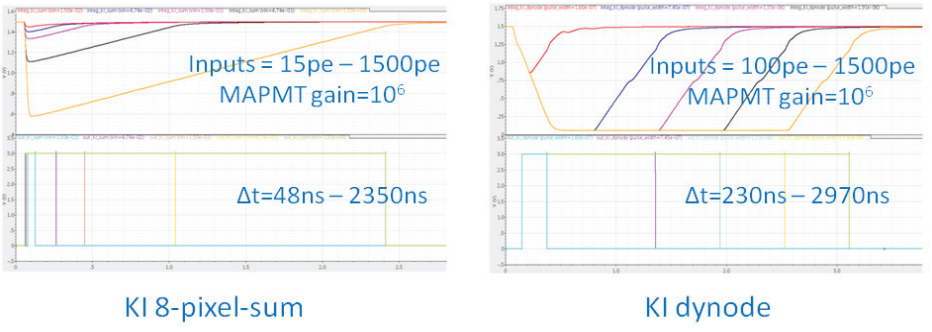


Fig. 5. KI analog signals and Triggers (Discriminators) outputs simulations. (a) KI 8-pixel-sum ; (b) KI dynode

## 4. Digital Design

All the data acquisition and readout are done within a defined time slot which is called Gate Time Unit (GTU=2.5µs). This means that for each cycle of GTU, the present data are acquired and the previously recorded data are sent out on the serial links. For the Photon Counting (Fig 6(a)), the digital part is organised into 8 identical modules. Each module will handle 8 triggers from Photon Counting analog part. The discriminator output's rising edge is used to clock an 8-bit counter which could operate up to 100 MHz. The counters data are transmitted on the dedicated serial links.

The digital part for the KI (Fig 6(b)) has the same architecture as the digital part for Photon Counting. However it has some minor differences for certain components. As the KI part has 9 channels, only one digital module is used. The KI discriminator outputs are sampled by the system clock of the digital block. The readout management program has been written differently so that it could accommodate a bigger channel number. The digital part of SPACIROC was designed carefully in order to minimize area usage, to reduce power consumption and to increase the robustness of the system. Flip-flops in critical areas are implemented in Triple Modular Redundancy (TMR) configuration in order to mitigate the effects of SEU.

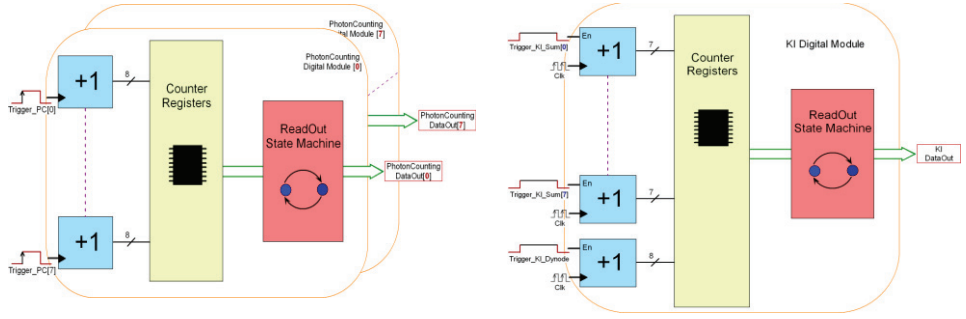


Fig. 6. (a) Photon Counting digital; (b) KI digital

## 5. Measurements

The ASIC was received in October 2010 and extensive tests have been carried out. A test board (Fig 7) and a Labview interface have been developed for testing SPACIROC.

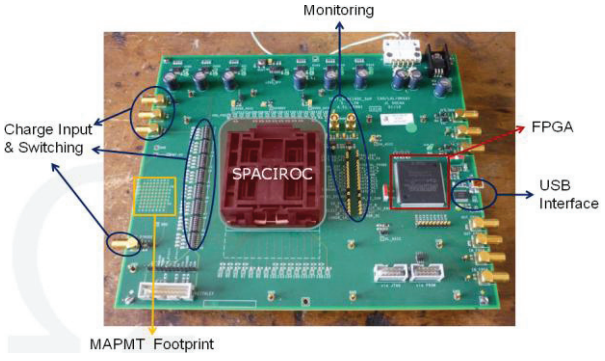


Fig. 7. SPACIROC test board

The linearity of the DACs is shown in Fig 8. These 10-bit DACs cover the voltage range of 0.9-2.6 V with a linearity of ±0.2%. The range and linearity of these DACs are good enough for the setting the thresholds.

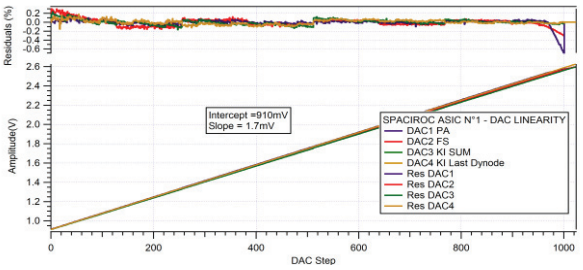


Fig. 8. SPACIROC DACs linearity

The usual S-Curves tests were done for the Photon Counting part. Fig 9 shows the S-curves for the Photon Counting triggers: Tig_FSU, Trig_PA and Trig_VFS.

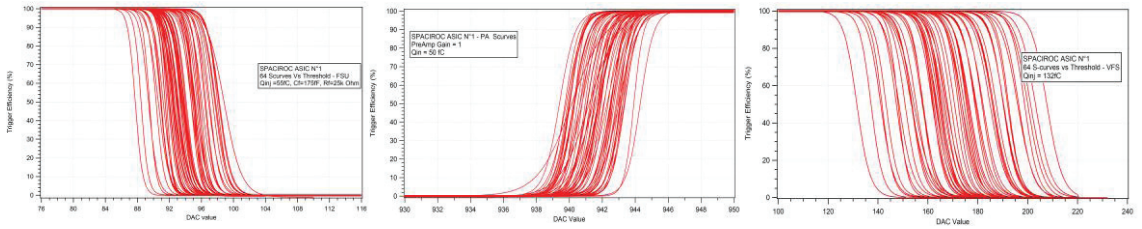


Fig. 9. Photon Counting 64-channels S-Curves. (a) Trig_FSU; (b) Trig_PA; (c) Trig_VFS

As shown in Table 1, Trig_FSU is giving the best trade off in term of noise, performances and power consumption. Thanks to the FSU variable gain, it will give users flexibility on controlling the noise level, shaping time and overall gain.

Table 1. Photon Counting characteristics summary

| | Double Pulse Separation | Gain | Min Input | 50% Triggering Efficiency RMS | Power Consumption |
|---|---|---|---|---|---|
| Trig_FSU(low noise config) | 30 ns | 1 mV/fC | 30 fC | 2.5 DAC unit | 0.4 mW/ch |
| Trig_PA (unity gain setting) | 36 ns | 0.32 mV/fC | 30 fC | 1.8 DAC unit | 0.2 mW/ch |
| Trig_VFS | 15 ns | 1.3 mV/fC | 60 fC | 17 DAC unit | 0.4 mW/ch |

For the KI part measurements, it was done in collaboration with RIKEN, Japan. Fig 10 is showing the linearity tests of the KI in single pulse/GTU mode. However, this is only one of the tests scenarios for the charge measurements. Extensive tests and optimisations on the KI part are currently underway especially by connecting a 64-channel MAPMT and LED light source. The final target is to give coarse measurements of the photon intensity under the JEM-EUSO running conditions.

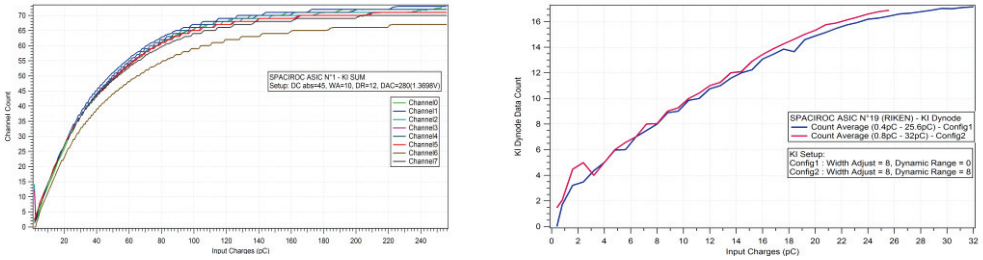


Fig. 10. KI Data count vs Input charges. (a) KI 8-pixel-sum. Input charges: 1.6 - 250 pC; (b) KI dynode. Input charges: 0.8 - 32 pC

Another important aspect of this ASIC is the power consumption. With the recommended settings for JEM-EUSO, this ASIC dissipates around 1.1 mW/ch. It is slightly higher than the expected values and it shall be corrected in the new version of SPACIROC.

## 6. Conclusions

As far as the tests and characterisations are progressing, SPACIROC is demonstrating good overall performances. Nevertheless better performances are needed for the JEM-EUSO applications. Otherwise, this ASIC is ready to be use for experiments having less constraint on the requirements compared to JEM-EUSO. A new version of this ASIC is currently under development in order to improve the performances and to eliminate the design bugs. The critical sectors which need to be rectified are the power consumptions, the double pulse separation resolution and the charge measurements. This is going to be the pre-production prototype before the mass production for the JEM-EUSO installation.

## Acknowledgements

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