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Vertex and Tracking Detector R&D for CLIC

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Abstract

The physics goals at the proposed future Compact Linear Collider (CLIC) pose challenging demands on the performance of the detector system. Precise hit-time tagging with a few nanoseconds resolution is required for the vertex and tracking detectors, as well as a very low mass per layer combined with a single-plane spatial resolution of a few micrometers. To address these requirements, an all silicon vertex and tracking system is foreseen at CLIC. To this end, a broad R&D program on new silicon detector technologies is being pursued. While the silicon pixel R&D for the CLIC vertex detector and tracker covers a wide range over various technologies and the development of different tools, this contribution is mainly focussed on the development of monolithic CMOS sensors with a small collection electrode.

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1. Introduction

The Compact Linear Collider CLIC is a project for a linear e^+e^- collider in the post-LHC era at CERN, with a centre-of-mass energy up to $\sqrt{s} = 3\,\text{TeV}$ [1]. The CLIC beam is structured in bunch trains with a length of 156 ns and repetition rate of 50 Hz. This corresponds to a low duty cycle, which allows the front-end electronics of the detectors to be switched off for most of the time of the CLIC beam cycle (*power pulsing*) to reduce the power consumption and thus the heat dissipation and cooling material significantly [2].

To achieve a high luminosity, the CLIC beam is reduced to a size of $40\,\text{nm} \times 1\,\text{nm} \times 44\,\mu\text{m}$ at the final focussing close to the interaction point. The resulting high electric fields of the incoming beams lead to a high rate of background particles especially in the innermost layers of the detector. To

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mitigate the impact of these background hits, precise hit time tagging with a resolution of $\sim$ 5 ns is needed in the vertex and tracking system. Moreover, to achieve the required measurement accuracy, a low mass of $\sim$ 0.2 %X_0 per layer for the vertex detector and $\sim$ 1 %X_0 per layer for the tracker is needed, combined with a single-plane spatial resolution of 3 μm in the vertex detector and 7 μm in the tracker [2].

A broad R&D program on new silicon detector technologies is carried out. This contribution gives a brief overview of the different technologies that are explored and mainly concentrates on the development of CMOS sensors with a small collection electrode.

2. Hybrid pixel detector developments

For the ultra-light vertex detector a very small pixel size of $\lesssim 25\,\mu$m is needed to reach the challenging requirement of 3 μm single-plane spatial precision. To fit complex functionality, such as power pulsing and simultaneous *Time of Arrival (ToA)* and *Time over Threshold (ToT)* measurement capabilities in the small pixels, hybrid technologies with the sensor and the circuitry in different physical layers are explored with innovative sensor concepts. A dedicated readout chip, the CLICpix2 [3], has been developed in a 65 nm CMOS process, with a $25 \times 25\mu\text{m}^2$ pixel size, 5-bit ToT readout and a 10 ns ToA binning. Moreover, adapted to the low duty cycle of CLIC, pulsed power operation has been implemented in CLICpix2 and experimentally tested [4]. The CLICpix2 has been interconnected via fine pitch bump-bonding to thin planar sensors and tested in various test-beam campaigns. Overall, the results indicate that with a thin sensor thickness of 50μm, needed to reach the low material budget, the charge sharing in the sensor is not sufficient to achieve a spatial precision of 3μm [2]. Innovative sensor concepts with deep implants to shape the field in the sensor and increase the lateral drift and thereby the charge sharing, *Enhanced Lateral Drift (ELAD) sensors* are thus under investigation [5]. Furthermore, alternative interconnects such as bonding using *Anisotropic Conductive Films (ACF)* are explored, to overcome the challenges of fine pitch bump-bonding [6]. Moreover, various *Silicon On Insulator (SOI)* test chips are under study [7, 8], which offer the advantages of a monolithic design, while implementing the circuitry in a separate and isolated layer.

3. Monolithic pixel detector developments

Monolithic pixel detector designs with the readout electronics integrated in the sensing layer allow to reduce the material budget and to overcome the cost and production effort of fine pitch bump bonding. As such, monolithic technologies are interesting for the large area silicon tracker for CLIC. In the *large collection electrode CMOS design* the circuitry for the readout is placed inside the collection electrode. To investigate this design, the ATLASpix_Simple prototype [9] has been extensively studied, meeting most of the requirements for the CLIC tracker [2].

A small sensor capacitance is advantageous in order to minimise analogue power consumption, noise and threshold and maximise the signal [10]. The sensor capacitance is in first approximation proportional to the radius of the collection electrode. Thus, to minimise the size of the collection electrode and as such the capacitance, the *small collection electrode CMOS design*, places the circuitry outside the collection electrode in a separate inversely doped well. For the *CLIC Tracker Detector (CLICTD)* [11] chip a modified small collection electrode imaging process is investigated, originally developed for the ALICE ITS upgrade [12]. This process makes use of a high resistivity P-type epitaxial layer grown on a low resistivity P-type substrate. A small N-type collection electrode is surrounded by highly P-doped wells that isolate the circuitry from the sensing volume. A process modification with a deep N-layer to achieve full depletion in the sensor [13] is used for CLICTD to improve the time-stamping capability.

In collaboration with the foundry a further modification of this process has been developed [14], to increase the lateral electric field at the pixel borders. In this process modification a gap in the N-layer or an additional P-implant are placed at the pixel borders to shape the electric field lines towards the collection electrode. In this way, the charge collection in the sensor and the sharing of the charge between individual pixels are reduced. The faster charge collection and higher single pixel charge simultaneously improve the radiation tolerance [15], the time-stamping capability and widen the efficient operation window to higher threshold values, which is especially relevant for thin sensors.

3.1. CLICTD - a small collection electrode CMOS chip for the CLIC tracker

The CLICTD chip has been implemented on a 30 μm thin epitaxial layer and contains 16 $\times$ 128 detector channels with a size of 300 $\times$ 30 μm^2. Each

channel consists of 8 pixels with a size of $37.5 \times 30\,\mu\mathrm{m}^2$ incorporating a dedicated analogue front end and collection electrode. The outputs of the 8 analogue front-ends in the channel are combined in a logic OR. The combined output is then processed in the digital logic of the channel, which performs an 8-bit ToA measurement with 10 ns time bins and a 5-bit ToT measurement with programmable range. In this way, the amount of digital logic is reduced while the separate collection electrodes maintain the small capacitance and fast charge collection. In addition, the hit pattern per channel is read out.

To reduce the in-channel charge sharing and speed-up the charge collection, the CLICTD chip has been submitted in two process variants: with a continuous deep N-implant and with a gap in the N-implant between the pixels in a channel, as illustrated in Figure 1. The gap in the N-implant has

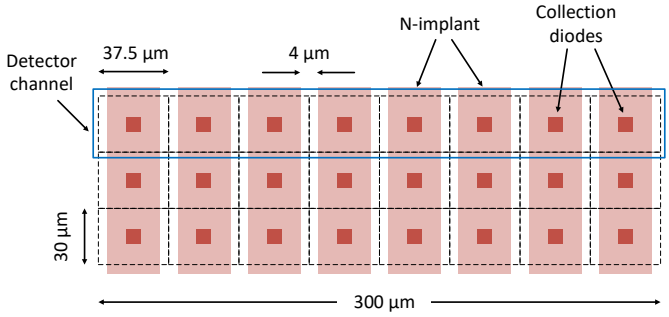

Figure 1: CLICTD channel layout for the process variant with gap in N-layer. The dark red squares indicate the collection electrode, the red area the segmented N-layer and the blue line the channel borders.

not been introduced in the other dimension between the channels of the chip, since this dimension corresponds to the rΦ-dimension of the detector, where the charge sharing is desired to improve the spatial precision.

Various test-beam campaigns have been performed at the DESYII test-beam facility [16], using a EUDET-type telescope [17] with a Timepix3 [18] plane as timing reference. With this setup, the expected precision of the telescope track position interpolated on the CLICTD is $\lesssim 2.5\,\mu$m.

For the results presented in the following, the CLICTD P-wells and substrate have been biased to -6 V. Figure 2 shows the cluster size within the pixel cell for both process variants at a low detection threshold of approximately $\sim 150\,\mathrm{e}^-$. The gap is located at the pixel borders within the detector

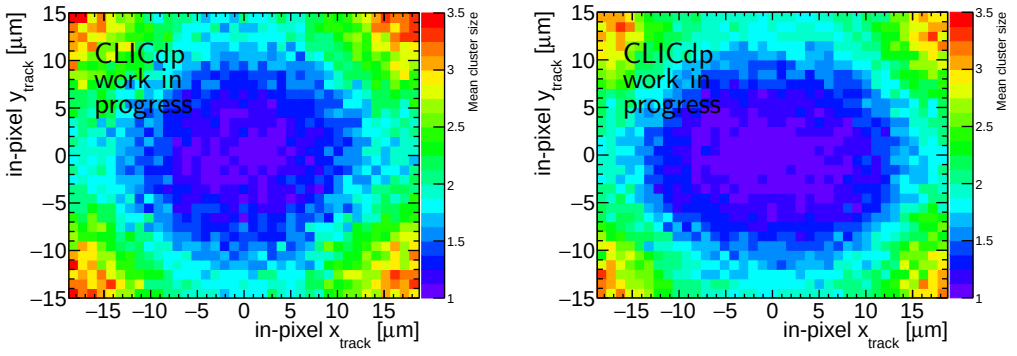

Figure 2: Cluster size within the pixel cell for the process variant *without (left)* and *with (right)* a gap in the N-layer.

channel at very high and very low X-values. The in-channel charge sharing in this pixel region is reduced by the gap in the N-layer, reducing the overall cluster size from 1.9 for the process variant without to 1.77 for the process variant with the gap in the N-layer.

Due to time-walk, the charge sharing within the pixel cell also impacts the precision of the hit time measurement. This effect is convolved with different arrival times due to lower electric field strength at the pixel borders, especially in the pixel corners. To account for this, a time-walk correction has been applied separately for the different process variants and different cluster sizes. The residual of the CLICTD hit time-stamp after time-walk correction with respect to the track reference time-stamp is presented in Figure 3. The

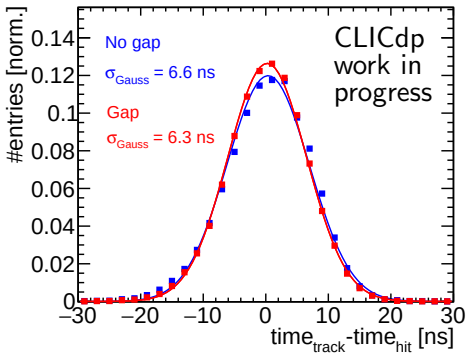

Figure 3: CLICTD temporal residual distribution for both process variants.

track time-stamp is defined as the time-stamp of the associated Timepix3 hit, with an expected uncertainty of $\sim$ 1.5 ns [19]. From a Gaussian fit to the residual distributions a width of $\sim$ 6 ns has been measured for both process variants, being slightly better for the process variant with thse gap in the N-layer, as expected due to the speed-up of the charge collection in the sensor. The differences in temporal resolution between the process variants are not very significant due to the 10 ns ToA binning of the 100 MHz readout clock frequency of CLICTD.

The efficiency as a function of the detection threshold shows a large efficient operation window, as illustrated in Figure 4 for the process variant without a gap in the N-layer. For threshold values $\lesssim 450\,\mathrm{e}^-$, the efficiency

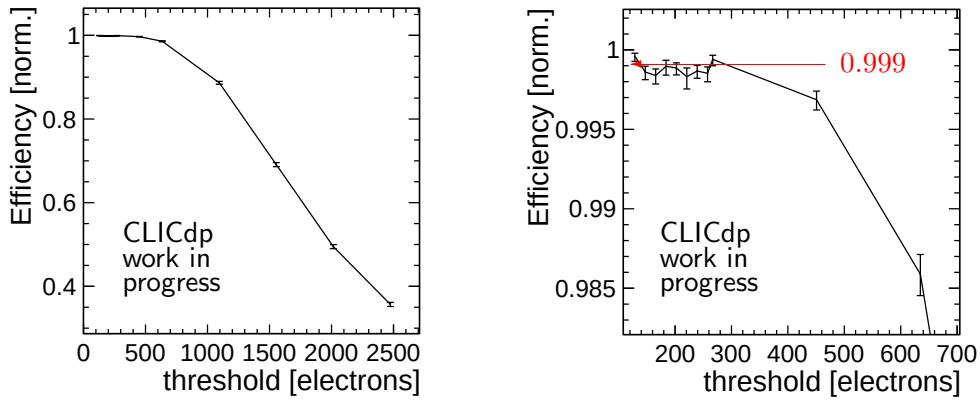

Figure 4: Efficiency as a function of threshold over the full measurement range *(left)* and zoomed into the high efficiency region *(right)*.

is well above 99.5 %, saturating at values of $\sim$ 99.9 % for threshold values $\lesssim 300\,\mathrm{e}^-$.

Using linear charge interpolation, a single hit resolution $\lesssim 7\,\mu$m has been measured. The reconstruction of the hit position with algorithms that account for non-linear charge sharing is currently in progress and is expected to further improve the measured spatial resolution.

4. Summary

Demanding requirements are imposed on the vertex and tracking system of the future linear $\mathrm{e^+e^-}$ collider CLIC. A broad R&D programme is being pursued to investigate the potential of various technologies.

For the CLIC tracker a small collection electrode CMOS chip, the CLICTD has been developed. It comprises a novel readout concept to reduce the digital circuitry while maintaining the small capacitance and speed of charge collection in the sensor. Moreover, process variants enhancing the sensor performance have been developed and implemented in the CLICTD. First CLICTD test-beam results show an excellent performance. With a spatial resolution $\lesssim 7\,\mu$m, a timing resolution of $\sim 6\,$ns and an efficiency of $\sim 99.9\,\%$, the measured performance of the chip is very close to the design specifications targeting the CLIC tracker requirements. Owing to the highly non-linear electric field in the sensor, the application of more advanced reconstruction algorithms is expected to further improve the temporal and spatial precision and is currently ongoing.

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