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Chapter 11

Warm Powering

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New power converters are needed for the powering of the HL-LHC circuits in the insertion regions of LHC points 1 and 5. In addition to the unprecedented precision, the HL-LHC power converters are also designed to assure very high availability in order to maximize operation time. Moreover, energy storage system will be designed to not only recuperate the magnet energy but to optimize the electrical infrastructure for accelerator applications as well. Furthermore, with an even more complex inner triplet circuit than in the LHC, a new nested circuit control needs to be developed for the HL-LHC. This chapter will present the main novelties and challenges in the development of the HL-LHC power converters.

1. Introduction

The new power converters for HL-LHC are requested to deliver even superior performance with respect to the systems developed for the LHC. The main challenges of the HL-LHC warm powering systems can be summarized as follows:

- high availability to maximize operation time;
- magnet energy storage and optimization of the electrical infrastructure;
- unprecedented precision request for the powering systems;
- handling circuit complexity: new decoupling control strategy.

To ensure high availability, the architecture of the power converters will be redundant, modular and radiation tolerant in radiation exposed technical galleries. Furthermore, an energy storage system will be designed for the HL-LHC inner triplets whose interest is twofold. Firstly, it will store the magnet energy for optimal energy management. Secondly, it represents a cornerstone for the optimization of the electrical infrastructure for accelerator applications. Furthermore, a new nested circuit control is developed to handle the complexity of this circuit. This chapter will present these main novelties and challenges of the HL-LHC power converters development.

2. High Availability by means of Modularity and Redundancy

Increasing the availability of the power converters is a major challenge to increase time of beam collisions. To achieve high availability, the architecture of modern power converters for particle accelerator has to be highly modular and radiation tolerant if placed in a radiation exposed area.

Two main parts constitute a power converter: the first comprises the power part that includes the power and protection modules, and the second can be categorised as the control and measurement electronics. Concerning the power system of the power converter, there are two main advantages for introducing modularity. Firstly, the power converter can be repaired faster in case of failure while spare parts quantities are minimized. Secondly, the architecture of the power converter with modular power bricks can provide redundancy for operation. In other terms, if a single power brick fails, operation can continue smoothly without triggering a beam dump and repair can be done during a technical stop if possible. This is also known as $n + 1$ redundancy. The power converter internal architecture is illustrated in Fig. 1 including the $n + 1$ parallel implementation of the power part which is common to all power converters for HL-LHC.

The high reliability control electronics based on FGC (Function Generator and Controller) is detailed in [1]. Two types of controllers are foreseen: FGC3.2 whose electronics will natively support $n + 1$ redundancy and FGCLite for radiation tolerant power converters (guaranteeing full compatibility with existing LHC ones).

The powering of the corrector magnets typically requires operation in positive and negative current. Three families of 4-quadrant power converters

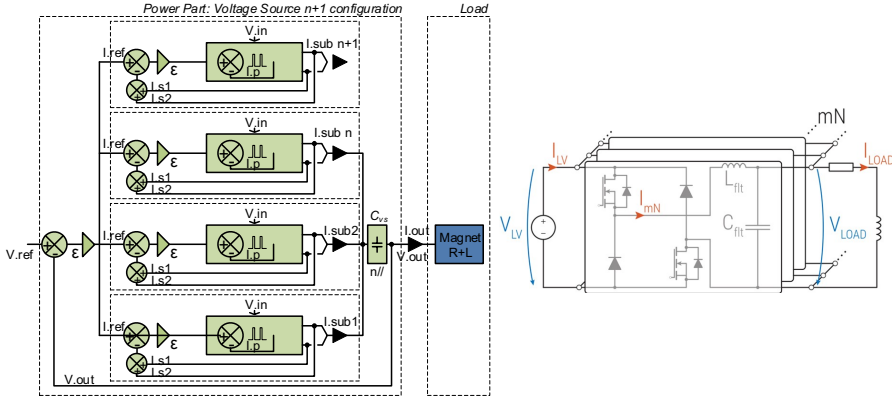

Fig. 1. Architecture of modular and redundant power converters: (left) the control scheme of the parallelization of $n + 1$ power sources to supply the final current to the load and (right) schematic illustration of the power connection of the parallel modular branches (N sub-converters composed on m branches each).

were developed for the LHC machine to cover all corrector magnet families and are rated for 60 A, 120 A and 600 A currents. With HL-LHC project, a new family of 4-quadrant power converter is required rated up to 2 kA (for some corrector magnets and trim circuits). The families developed for the LHC corrector magnets (below 600 A) are made with a unique power module rated at the maximum current, meaning with no modularity nor redundancy. In the higher currents family, the redundancy principle has demonstrated all its interest for the maintenance and for the availability of the machine. In the framework of R2E (Radiation to Electronics) Project, the 600 A converter was redesigned with introduction of redundancy. The power module is rated 400 A and two modules are placed in parallel to reach 600 A (current is limited to 600 A by the rating of the DCCT, DC Current Transformer, which is set to optimize for precision performance). In case of fault, and with an operational current set below 400 A, a power module failure will not stop the operation of the machine, as the second one will keep the magnet current constant. The redundancy is limited to 50% of the maximum current but most of the correctors operate far below their maximum current (in particular D2 correctors nominal current is 394 A so full redundancy is guaranteed up to 7 TeV).

For the new 2 kA family, the same redundancy principle will be used. The power converter will be composed of six power modules rated 400 A in

parallel. They shall be identical or based on the recently developed 400 A power modules.

3. High Current 2-Quadrant Power Converters with Energy Storage

Thyristor based power converters are widely used in particle accelerator high current applications. A main advantage of such a technology is the capability to operate in quadrant 2 where the energy is re-injected to the grid. However, these power converters are highly sensitive to grid glitches and inject harmonics to the grid where proper compensatory measures are needed.

For the HL-LHC, a new family for the 2-quadrant power converters is foreseen to be developed using switch-mode technology in order to keep the same good principles of the present LHC power converters where there is an increased immunity from grid glitches, where modularity can be easily applied, and where relatively low frequency voltage harmonics are not injected to the magnet circuit. However, the switch mode power converters developed for the high current LHC circuits are not bi-quadrant and do not provide the possibility to recuperate the energy stored in the magnet circuit during ramp-downs. The LHC solution relies on dissipating the energy stored in the magnet during ramp-downs in the resistive portion of the circuit i.e. DC cables. Therefore, as an addition to the switch-mode power converters developed for the LHC, energy management systems are studied for HL-LHC to find the best strategy to control the recovered magnet energy.

Moreover, due to several improvements of electrical storage systems like the last generation of batteries whose progress is driven by the development of electric vehicles, an Energy Storage System (ESS) that stores the magnet energy to be re-used in the following ramp-up could be envisaged [2]. The proposed scheme for energy storage is shown in Fig. 2.

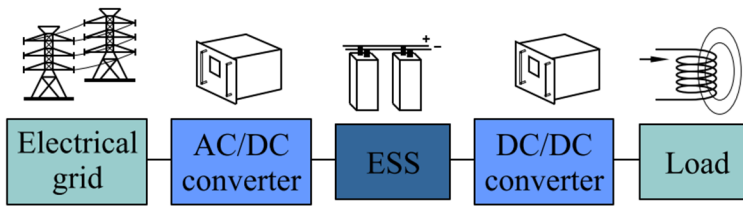

Fig. 2. Selected Energy Storage scheme.

In addition to the proper management of the energy stored in the magnet circuit, the introduction of energy storage brings another major advantage by reducing the power taken from the grid and reducing the infrastructure of the grid connection. The connection to the grid would, therefore, ensure only the losses due to the transmission chain (losses in the power converter, losses in the warm DC cables, etc.), whereas the magnet energy is provided by the electrical storage element. Moreover, the energy flow between grid, the energy storage system and the magnet would be optimized in order to maximize the lifetime of the storage element and its efficiency.

Research at CERN and within collaborations will be focused on power converter topologies, energy management and energy storage systems with a goal to keep reliability as high as possible, while reducing size and improving power quality and efficiency.

Concerning the energy storage system, many technologies were investigated, and the Lithium Titanate (LTO) batteries were chosen as baseline since they provide the best compromise between price, integration size and life cycle for the HL-LHC requirements. Fig. 3 shows an overview of the energy storage technologies (batteries and supercapacitors) and their performance.

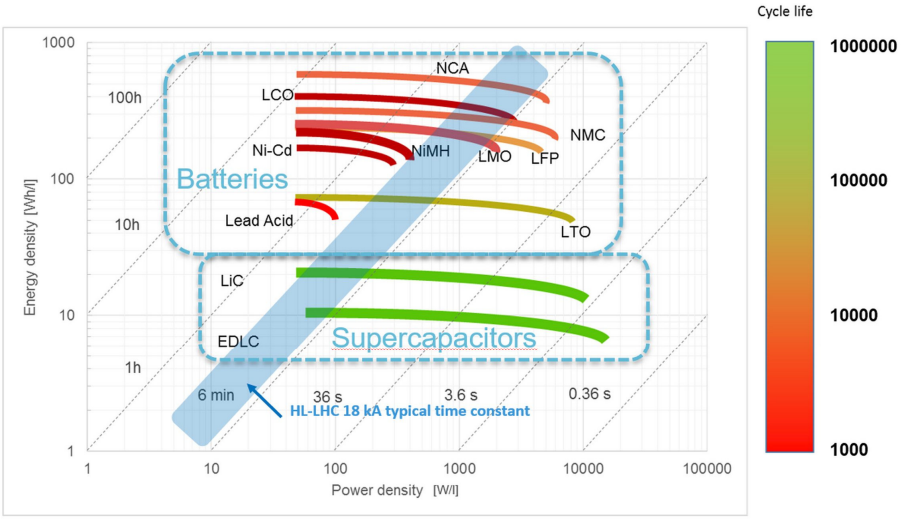

Fig. 3. Energy storage technologies and their performance in terms of energy density, power density and cycle lifetime.

4. Request for Unprecedented Precision

The new power converters for the Inner Triplets Q1-Q2a-Q2b-Q3 series and for the Separation/Recombination dipoles D1 and D2 are required to guarantee unprecedented current precision, and this represents a unique challenge in the design and more specifically in the measurement and control of the power converters' output current. The reader is referred to [3] (Chapter 6B) for proper definition of the main terms (borrowed either from metrology [4] or control theory [5]) used for the specification of power converter performance. As a reminder, throughout this chapter, relative figures are always expressed in ppm (parts-per-million) of a given reference value; for circuits currents the reference value is the rated current of the current measuring device, the DCCT (which usually coincides with the maximum value of current that can be generated by the power converter). As an example, the main power converter of the Inner Triplet Q1-Q2a-Q2b-Q3, the HCRPAFE, is rated 18 kA whereas the operating current at 7 TeV is about 16.5 kA; according to this convention one ppm amounts to 18 mA.

4.1. *Accuracy classes*

New accuracy classes have been defined for HL-LHC based on an update of the most useful classifications adopted for LHC. The new classification takes into account, as an example, the typical duration of a fill and is the result of a thorough estimation of the actual metrological performance of the current measurement chains of the LHC power converters [6] (the metrological performance turned out to be much better than what was specified for LHC in the design phase [7]). Its full definition is reported in [6]; only the main definitions are reported here (Fig. 4):

- **short term stability (20 min)** - variation of the delivered current (for a constant reference) during a period of 20 minutes, measured up to a frequency of 0.1 Hz
- **stability during a fill (12 h)** - variation of the delivered current (for a constant reference) during a period of 12 h, measured up to a frequency of 10 mHz
- **long term fill-to-fill stability** - variation of the delivered current for the same reference current after one year from the last calibration

- **fill-to-fill repeatability** - Fill to fill variation of the average of the delivered current (for a constant reference), measured over 10 consecutive fills.

All these parameters are defined at constant temperature; the effect of temperature change is then combined to calculate the global figures of merit summarized in Table 1. Furthermore these parameters are defined for a single converter (assuming an underlying statistical distribution), the spread among many converters is also considered in the global parameters, as an example taking the worst measured value on a set of tests or the maximum value for a uniform distribution (summarized Table 1 in column "Assumptions"). Finally, for uniformity of representation the global parameters are expressed as twice the rms, or standard deviation, value (gaussian distribution is not implied though, so twice the rms value does not translate into 95% confidence

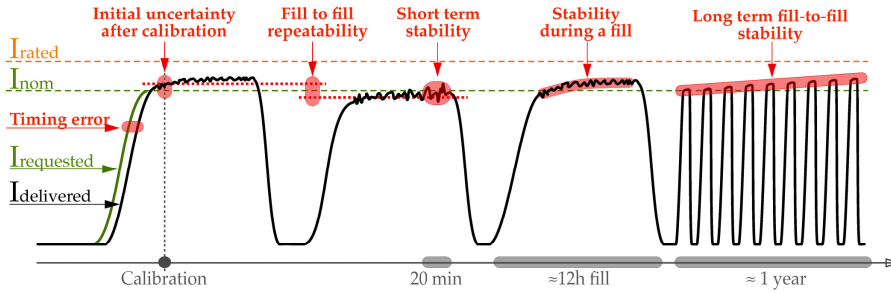

Fig. 4. Illustration of the main "precision performance" parameters together with their different time scales [8].

Table 1. Newly defined HL-LHC accuracy classes (main parameters only).

			ACCURACY CLASSES				
Metrological Parameter	Assumptions	Units	0	1	2	3	4
Short term stability (20 min)	w.c. / normal	2 x rms ppm	0.2	0.4	1.2	2.0	5.0
Stability during a fill (12 h)	max / uniform	2 x rms ppm	1.0	2.0	15.5	34	40
Long term fill to fill stability	max / uniform	2 x rms ppm	9.5	9.5	26.5	56	64
Fill to fill repeatability	w.c. / normal	2 x rms ppm	0.7	1.6	15.0	32	38
Temperature coefficient	uniform	max |.| ppm/C	1.0	1.2	2.5	5.5	6.5
12 h Delta T for HL-LHC	constant	max C	0.5	1.0	5.0	5.0	5.0
1 y Delta T for HL-LHC	constant	max C	0.5	1.0	5.0	5.0	5.0

Table 2. Summary of precision requirements per magnet/circuit (including LHC mains for comparison). In the definition of these parameters specific frequency ranges have been considered based on the considerations presented in section 0.

Circuit Name	Equipment Code	I_{DCCT} [kA]	Accuracy Class	Stability [ppm of $I_{DCCT.rated}$] expressed as twice the rms value		
				Short Term	During a fill (12 h)	Long Term fill-to fill
RB	HCRPTE	13	1	0.4	2	9.5
RQ(D/F)	HCRPHE	13	1	0.4	2	9.5
RQX	HCRPAFE	18	0	0.2	1	9.5
RTQX1	HCRPBAB	2	2	1.2	15.5	26.5
RTQXA1	HCRPALD	0.06	4	5	40	64
RTQX3	HCRPBAB	2	2	1.2	15.5	26.5
RCBX	HCRPBAA	2	2	1.2	15.5	26.5
RQSX	HCRPMBD	0.6	3	2	34	56
RC(S/O)X	HCRPLBC	0.12	4	5	40	64
RC(D/T)X	HCRPLBC	0.12	4	5	40	64
RD(1/2)	HCRPAFF	14	0	0.2	1	9.5
RCBRD	HCRPMBF	0.6	3	2	34	56
RQ4	HCRPHRA	4	2	1.2	15.5	26.5
RCBY	HCRPLBC	0.12	4	5	40	64
RQ(5/6)	HCRPHSB	5	2	1.2	15.5	26.5
RCBC	HCRPLBC	0.12	4	5	40	64
RTB9	HCRPMBE	0.60	3	2	34	56

interval). A summary of accuracy classes and precision parameters, per circuit, is reported in Table 2.

4.2. *Impact on the beam quality – requirements from beam physics*

A first thorough review of the precision and accuracy requirements for all circuit types is reported in [8].

4.2.1. *DC performance*

Requirements are currently based on a rather simplified model of the full transfer function from power converter output (voltage or current delivered to the load) to the magnetic field experienced by the beam. The full transfer function, for a frequency range where stray capacitances can be neglected, can

be modelled as in the following equation:

$$\mathrm{B_b}(f) = \begin{cases} T_{\mathrm{B_m toB_b}}(f) \cdot T_{\mathrm{ItoB_m}}(f) \cdot i(f) & f \le f_0 \\ T_{\mathrm{B_m toB_b}}(f) \cdot T_{i\mathrm{toB_m}}(f) \cdot T_{v\mathrm{to}i}(f) \cdot v(f) & f > f_0 \end{cases} \quad (1)$$

where $i(f)$ is the (circuit) current noise, $v(f)$ is the power converter's voltage noise, $T_{v\mathrm{to}i}(f)$ is the overall circuit admittance, as seen at the power converter's terminals, $T_{i\mathrm{toB_m}}(f)$ is the transfer function from the circuit current to the magnetic field produced by the magnet, $T_{\mathrm{B_m toB_b}}(f)$ is the transfer function of the cold bore, beam screen etc. (which determines the magnetic field actually seen by the beam) and f_0 is a parameter set by the (digital) current regulation of the power converter. For frequencies below f_0 the current regulation is fully active, and the power converter is operating in "current control" mode, whereas for frequency above f_0 the electrical characteristics of the circuit dominate over the current regulation loop and the converter is considered to be operating in "voltage control" mode. Both $T_{\mathrm{B_m toB_b}}(f)$ and $T_{i\mathrm{toB_m}}(f)$ were assumed constant for LHC design. This approximation is rather accurate in the "current control" frequency and f_0 spans from few tenths of Hz to few Hz as for LHC and HL-LHC (performance parameters presented in 4.1 mostly cover this range of frequencies). However, such an approximation is overly pessimistic for higher frequencies where important attenuations due to different loss phenomena are indeed introduced; neglecting them would turn into an overspecification of power converters and finally extra costs. The frequency response $T_{\mathrm{B_m toB_b}}(f)$ for HL-LHC magnets/ beam screens configurations and the LHC mains, has been thoroughly investigated in [9]: the cut-off frequency spans from about 32 Hz for HL-LHC Q1 to about 135 Hz of LHC main quadrupoles. An equivalent electrical circuit model (a generalization of the one presented in [10]) is shown in Fig. 5 (left) assuming that all the circuit current is producing magnetic field (lossless magnet) and assuming $H(s) = T_{i_{\mathrm{B_m}}\mathrm{to}i_{\mathrm{B_b}}}(s) = T_{\mathrm{B_m toB_b}}(s)$. With this simplified model all the effects of the power converter voltage noise $v(f)$ on the field experienced by the beam, $\mathrm{B_b}$, can be translated in terms of the equivalent current $i_{\mathrm{B_b}}$ [11]. The overall transfer function is (for $0 \le k \le 1$):

$$\frac{i_{\mathrm{B_b}}(f)}{v(f)} = \frac{H(f)}{R_c + j2\pi f L[(1-k)+kH(f)]} \quad (2)$$

It is important to highlight that the noise on the circuit current i (measured by the current measurement chain) is greater than the noise on i_{B_b} (for $f \geq f_0$):

$$\left|\frac{i_{B_b}(f)}{v(f)}\right| \cong \frac{1}{2\pi f L}\left|\frac{H(f)}{[(1-k)+kH(f)]}\right| \leq \frac{1}{2\pi f L} \cong \left|\frac{i(f)}{v(f)}\right| \tag{3}$$

In other terms the presence of a conductive beam screen, $|H(f)| \leq 1$, guarantees additional lowpass filtering of the power converter noise with respect to an ideal inductor with the same DC (differential) inductance L. The voltage noise acceptance limits currently considered, for spectral lines (and not for broadband noise) are reported in Fig. 5 (right).

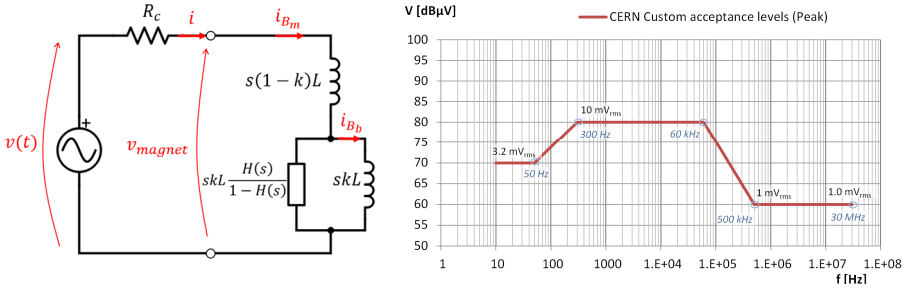

Fig. 5. (Left) Equivalent circuit of a lossless superconducting magnet with a beam screen. (Right) Output ripple limits profile (≤ 50 V DC output): maximum tolerated tone amplitude for a given $\boldsymbol{f}$.

4.2.2. *Tracking*

As for LHC [12], and many other accelerators at CERN [13], the digital control algorithm is the RST, a 2-degree-of-freedom polynomial controller, implementing a dead-beat input-output relationship as in the following equation:

$$\frac{i_{ref}}{i} \cong e^{-\tau_d s} \leftrightarrow i(t) \cong i_{ref}(t-\tau_d) \tag{4}$$

In closed loop actual circuit current is approximately a delayed version of the reference current; being a design parameter, τ_d can be corrected for and the error between the two (actual versus "delayed reference"), during ramp-up and ramp-down phases, would be constrained only by the accuracy class of the power converter [6,8,14].

4.3. *High precision measurement R&D for Class 0 Accuracy*

The principles and main components of the high precision measurement chain of the power converters current are discussed in [1,3] and in more details in [15]. It is assumed here that the uncertainty of the power converter is equal to the uncertainty of the measurement chain in the low frequency range which can be translated into the combined uncertainty of DCCTs and ADCs (Analog-to-Digital Converter). Here, only their R&D aspects will be highlighted.

4.3.1. *DCCT*

The DCCT is a mature and highly reliable technology based on the concept of "zero flux" where the DCCT current can be assumed to be an extremely accurate fraction of the measurand current that nullifies the flux produced by the latter. Some improvement is however still needed to comply with Class 0 requirements: R&D activities are focusing on improvements on the summing node of the feedback loop of the "zero flux" circuit and, more importantly, in the "current to voltage" conversion stage, as voltage is always used for digitization [15]. In particular the focus is on the high-precision current sensing resistors (a.k.a. the burden resistors) or alternative "current to voltage" conversion technologies as they represent a strategic know-how for CERN [16].

4.3.2. *ADC*

At the end of the 90's no ADC on the market was deemed to be able to comply with LHC Class 1 requirements, so a CERN internal development was launched which led to the DS22 (22-bit resolution Delta-Sigma ADC). Given its obsolescence and the new challenge of Class 0 [17] an R&D project was launched for its upgrade. Another direction of R&D is a completely new design based on commercial ADCs with improved performance; this included a thorough survey of the state-of-the-art in high resolution ADCs [18]. Preliminary test results are quite encouraging both for the DS24 (the upgraded version of the DS22 with 2 extra bits of resolution) and for the HPM7177 [19] (the new ADC based on the commercial Delta-Sigma chip AD7177-2, Fig. 6).

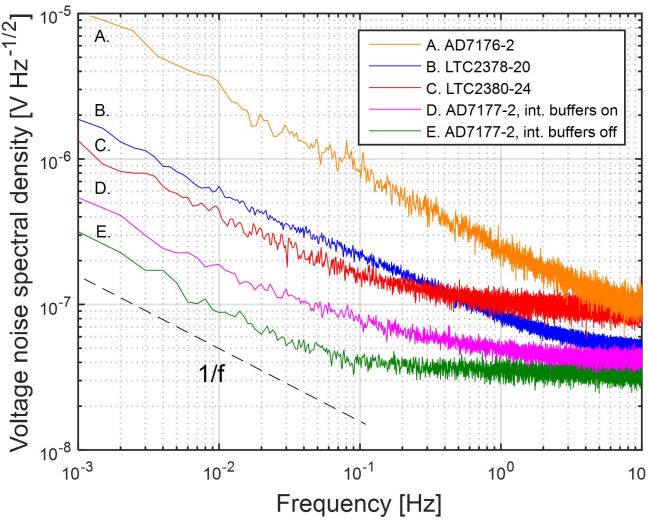

Fig. 6. Comparison of noise performance of the most promising commercial ADCs [19].

5. Handling Circuit Complexity: A New Decoupling Control

The main quadrupole circuits for the inner triplets of LHC comprise three nested circuits [12]. From the circuit control point of view, this connection represents a Multiple Input Multiple Output (MIMO) system where the action on one circuit leads to a change of state of the other connected circuits. The adopted strategy for the control of the LHC inner triplets is based on the decoupling principle and it is realized by means of dedicated hardware.

For the HL-LHC inner triplets, four nested circuits are foreseen as shown on Fig. 7. In addition to the main 18 kA circuit to feed the triplets, two 4-quadrant trim power converters are added over Q1 and Q3 (rated ±2 kA, ±10 V) and a 4-quadrant trim power converter over Q1a (rated ±35 A, ±10 V) to perform k-modulation (see Chapter 5). Therefore, even if the decoupling strategy is kept for the HL-LHC, a new solution is developed to take into account the new configuration and the new challenge of controlling a three-layer nested circuit in contrast to the two-layer nested circuit of the LHC. Given the upgraded control capabilities of the control infrastructure based on Ethernet, a full software solution is chosen. This software solution includes an inter-FGC communication where information for the different branches of the circuit is shared to perform a global control of the current circulating in each

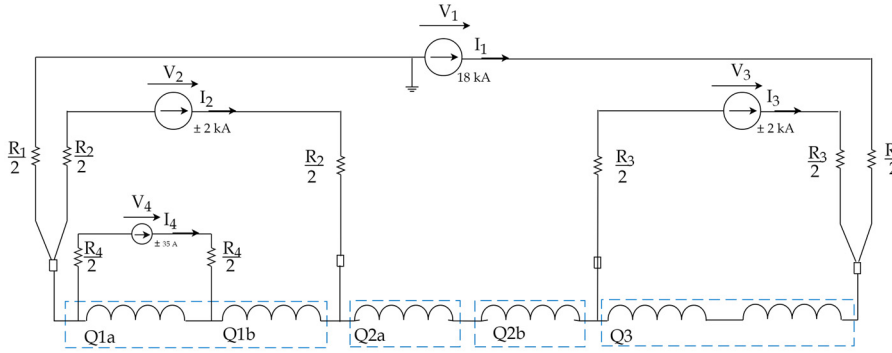

Fig. 7. Inner triplet main circuit simplified powering layout (cold diodes not shown).

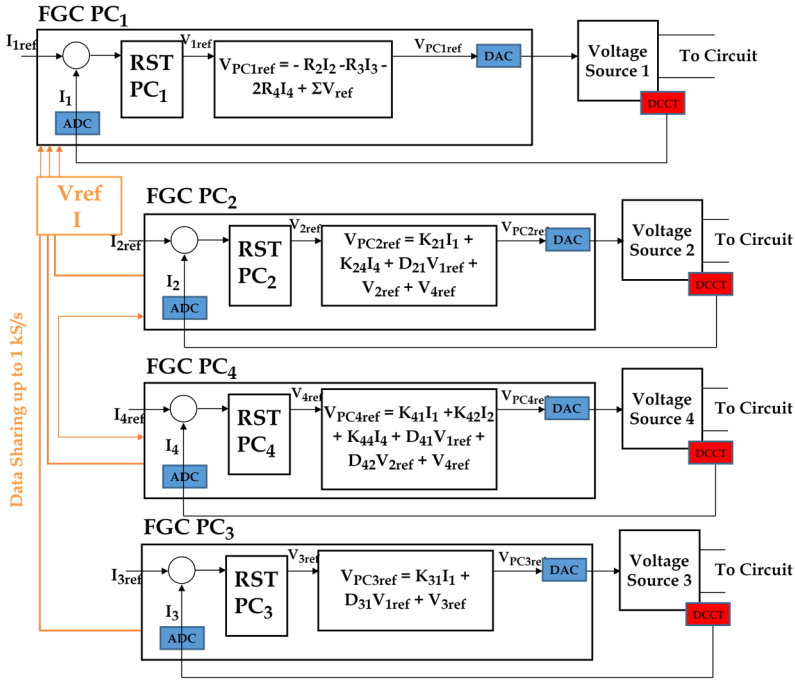

Fig. 8. Decoupling control architecture implementation.

branch. This solution will require the development of new libraries which will extend FGC control capabilities [13] beyond the current Single Input Single Output (SISO) paradigm. The state equation that describes the interaction

between the sub-circuits of the HL-LHC inner triplet is the following (with reference to Fig. 7):

$$\frac{dI}{dt} = \mathbf{A}\, I + \mathbf{B}\, V_{ref_{PC}} \tag{5}$$

where $I = [I_1\ I_2\ I_3\ I_4]^T$ and $V_{ref\_PC} = \left[V_{ref\_PC1}\ V_{ref\_PC2} V_{ref\_PC3}\ V_{ref\_PC4}\right]^T$.

In order to decouple the sub-systems, the reference voltages of the four converters need to be calculated as full state feedback as: $V_{ref\_PC} = \mathbf{K}\, I + \mathbf{D}\, V_{ref\_RST}$ by means of two decoupling matrices, **K** and **D**. This will *transform* the system from a MIMO (4x4) system into four SISO equivalent systems as follows:

$$\dot{I} = \mathbf{A}\, I + \mathbf{B}\left(\mathbf{K}\, I + \mathbf{D}\, V_{ref_{RST}}\right) = \mathbf{A}_d\, I + \mathbf{B}_d\, V_{ref\_RST} \tag{6}$$

where $\mathbf{A}_d$ and $\mathbf{B}_d$ are diagonal matrices and the decoupling matrices are calculated as: $\mathbf{K} = \mathbf{B}^{-1}\left(\mathbf{A}_d - \mathbf{A}\right)$ and $\mathbf{D} = \mathbf{B}^{-1}\mathbf{B}_d$. It can be proven that information sharing is needed between {PC1 and PC2}, {PC1 and PC3}, {PC1 and PC4} and {PC2 and PC4}; a possible implementation of the state feedback is then shown in Fig. 8. Preliminary simulations were performed and show satisfactory results [20].

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