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HARDWARE AND FIRMWARE DEVELOPMENT FOR ENHANCED ORBIT DIAGNOSTICS AT THE AUSTRALIAN SYNCHROTRON

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Abstract

The Enhanced Orbit Diagnostic (EOD) features will be an expansion to the existing Fast Orbit Feedback (FOFB) system that is currently in operation.

The new system will add the capability of online corrector-to-position response matrix calculation; this will significantly reduce the required measurement time. The new features will allow the injection of PRBS noise or sinusoidal signals into correctors, to characterise and monitor the FOFB system's parameters and performance and track it over time.

The system will be built based on a Xilinx ZYNQ System-on-Module (SOM) mounted on an in-house designed motherboard to which the existing FOFB daughter board is plugged into.

FOFB BASICS

The aim of the FOFB system is to reduce the RMS beam motion to under 10% of the beam size at all BPM locations up to 100 Hz and a unity gain bandwidth of greater than 300 Hz [1]. The FOFB system consists of four sub-systems:

(1) Libera beam position measurement and aggregation
(2) FOFB processor
(3) Corrector magnets and power supplies
(4) EPICS control system

A schematic of the system is shown in Fig. 1.

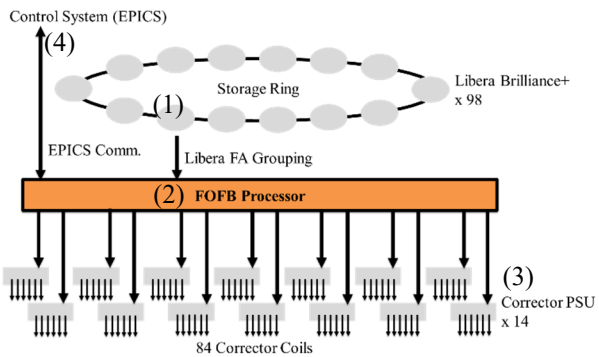

Figure 1: FOFB system architecture.

The FOFB processor firmware development was to develop all the interface modules and data processing modules in VHDL and use Matlab's Simulink™/HDL Coder™ combination to generate the proportional-integral handler module (PIH). The simplified system architecture is shown in Fig. 2.

The FOFB processor receives Fast Acquisition (FA) data from the BPMs, extracts the beam position information and translates this into corrector current values using an inverted BPM-Corrector response matrix, M^{-1}, provided through the EPICS control system. The feedback uses a proportional and integral handler with three harmonic filters in parallel. The corrector current values are sent to the magnet power supplies via optical fibres using a 10M baud serial protocol [2, 3].

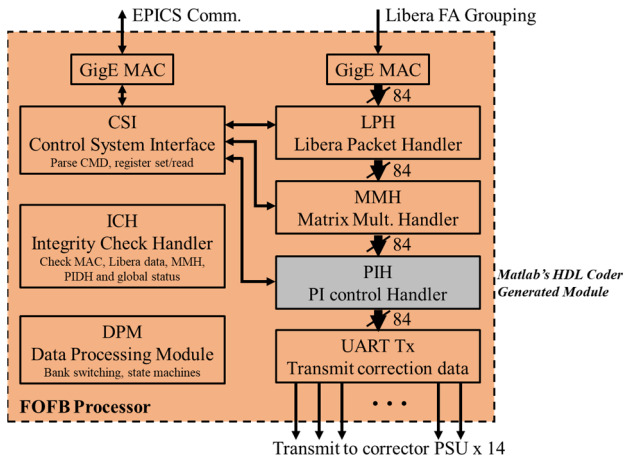

Figure 2: Simplified FOFB firmware architecture.

EOD HARDWARE

The EOD hardware system consists of three parts:

(1) EOD processor module
(2) EOD motherboard
(3) Existing FOFB daughter board

The FOFB processor employs a Hi-Tech Global HTG-V6-PCIE-240 development board (with a Xilinx Virtex6 FPGA on board) to do the real-time calculation. However the current FOFB computation logic utilizes all of the available programmable logic resources and due to the FPGA being released 10 years ago it is not economic for us to upgrade to a larger FPGA in the same series. As such we have chosen the Trenz Electronics TE0808 SOM (with a state-of-the-art Xilinx ZYNQ Ultrascale+ on board) as the new processor for the EOD project. It offers ~7 times resources of the existing unit and hence allow for the provision of additional functionalities.

The existing FOFB daughter board is equipped with 14 optical transmitters. They are drove by the 14 correction data streams from the ZYNQ processor.

The functional block diagram of the in-house designed 12-layer EOD motherboard is shown in Fig. 3. It provides the following functionalities:

1. Interconnection of the ZYNQ processor and the FOFB daughter board;
2. One PoE+ enabled Gigabit Ethernet port for the CPU portion of ZYNQ processor;

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3. 4 Gigabit Ethernet SPF+ ports for the FPGA portion of ZYNQ processor, two of them are White Rabbit synchronization compatible;
4. eMMC module to store the operating system files for the CPU portion of ZYNQ processor;
5. Five switching voltage regulators to power the EOD system. The power source can be switched between the PoE+ (for system power consumption ≤ 25W) and the DC input (for system power consumption > 25W).

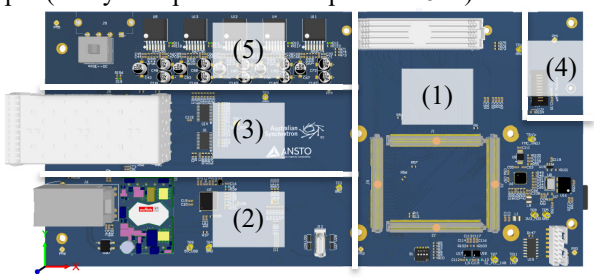

Figure 3: Simplified functional block diagram of the motherboard.

The 3D STEP models of the motherboard, the ZYNQ SOM and the FOFB daughter board is virtually assembled in Altium Designer to verify the design and to avoid any mechanical collision between components before releasing the motherboard PCB design for manufacturing. Their 3D effect is displayed in Fig. 4.

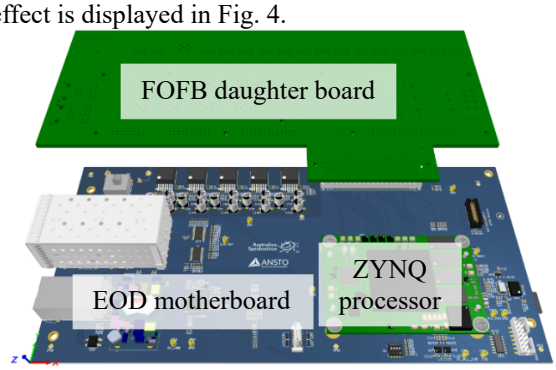

Figure 4: 3D effect of virtual assembly of the EOD system.

EOD FIRMWARE

The firmware requirements of the enhanced diagnostic features include:

- EPICS control to excite the fast corrector magnets with a sinusoidal waveform or white noise (PRBS).
- The magnitude of the noise and sinusoidal excitation of the corrector coil current is controllable from EPICS. The range is adjustable from -1 Ampere to +1 Ampere.
- The frequency and phase of the sinusoidal excitation is controllable from EPICS. The frequency range is adjustable from 1 Hz to 1 kHz with 1 Hz resolution. The phase resolution is 45 degrees;
- The duration of the noise and sinusoidal excitation is controllable from EPICS. The range of the duration is from 0.1 to 10 seconds with 0.1 second resolution;
- PRBS noise or sinusoidal excitations can be enabled or disabled;
- PRBS noise and sinusoidal excitations are mutually exclusive;
- Only one corrector coil out of 84 will accept the PRBS noise excitation at a time;
- Any six coils out of 84 will accept the sinusoidal excitations simultaneously. The current, frequency, phase and duration of the six excitations are controlled independently by EPICS;
- The FOFB calculation result is able to be monitored in real-time by sending out the data through a SFP Gigabit Ethernet port to EPICS.

The EOD firmware development will be based on the existing FOFB firmware by porting the VHDL source code to the ZYNQ platform initially without adding new features; then the enhanced diagnostic features will be integrated one by one.

According to the FOFB firmware architecture shown in Fig. 2, the noise and sinusoidal signal should be injected after the PIH module, as is shown in Fig. 5. The FOFB correction data can be disabled for pure noise or sinusoidal excitation. The FOFB correction data output is also at this point. The 84 parallel streams are packed exactly the same format as the Libera Brilliance+ FA grouping so that the same FA archiver system [4] and other diagnostic systems developed for the FA data can be directly used for analysis.

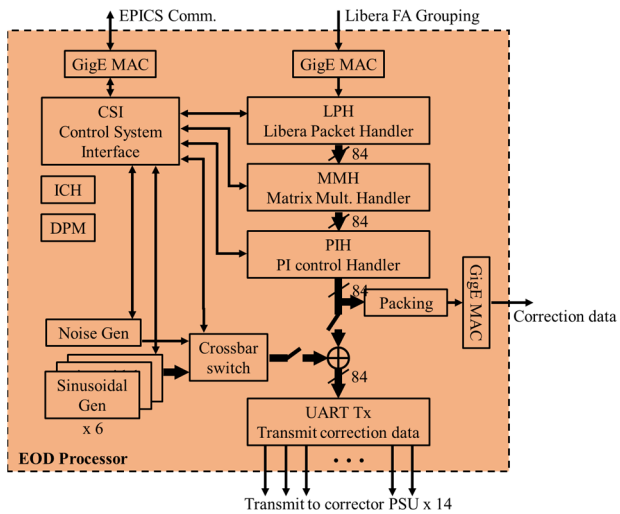

Figure 5: Simplified block diagram of EOD firmware architecture.

Noise and sinusoidal generation

The noise generation is based on a Linear Feedback Shift Register (LFSR) pseudo-random number generator. The period of sequence generated by the 12-bit LFSR is equal to 2^{12}-1.

The sinusoidal generation implements 6 independent Numerically Controlled Oscillators (NCOs) - also referred as Direct Digital Synthesizer (DDS). The block diagram of NCO is shown in Fig. 6 [5].

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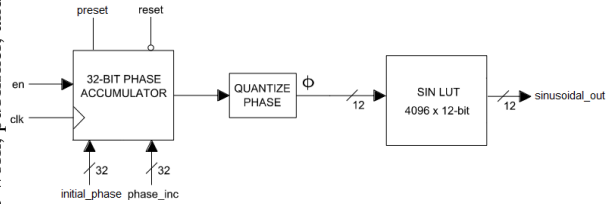

Figure 6: Block diagram of NCO.

The preset signal initializes the output sinusoidal waveform phase by writing the initial phase into the phase accumulator. On each rising-edge of the clk input (when en is high), the phase in the phase accumulator is incremented by the value phase_inc. This phase is quantized to 12-bits and passed as an address to a look-up table which converts the phase into a waveform. The look-up table is implemented as an array of 4096 x 12-bit samples over the range 0 to 2π. All output values are 12-bit signed numbers.

The phase and frequency of the output waveforms are controlled by the phase increment on a clock-by-clock basis. A change in the phase increment during normal circuit operation will affect a change in the output waveforms 2 clocks later. The phase increment may be calculated using the formula:

$$\Phi_{inc} = (F_{out} \cdot 2^{32}) / F_s + 0.5$$

where F_{out} is the desired waveform output frequency and F_s is the clk frequency. Note that the integer value of the phase increment must be used.

As an example, a 125 MHz clock input would allow a minimum NCO phase resolution of $2\pi/2^{12} = 0.0015$ degree, frequency resolution of $F_s/2^{32} = 0.0291$ Hz at the whole range from F_{out} = 1 Hz to F_{out} = 10 kHz. The requested phase and frequency resolution can be met.

The method for controlling the noise and sinusoidal amplitude in the digital domain is multiplying the signal by a configurable constant. This multiplication allows easy control of the coil current by reducing the maximum corrector PSU output.

Correction data output

The data payload of the UDP/IP packet in the Libera Grouping is an array of FA data sets from multiple Liberas in a group as shown in Fig. 7 [6].

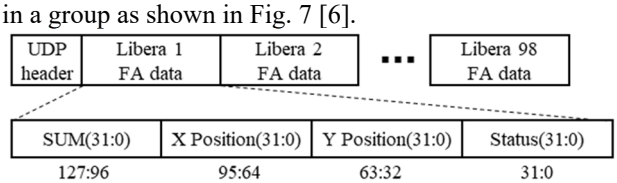

Figure 7: Libera grouping packet structure.

As the numbers of corrector coils in the X plane and Y plane are both 42 and the truncated correction data is 12 bits, only the first 42 FA data sets are filled with data and the remaining are zero padded. Inside each FA data set the SUM, Status section and X/Y Position section upper 20 bits are zero padded. Only the lower 12 bits of the X/Y Position are used, as is shown in Fig. 8.

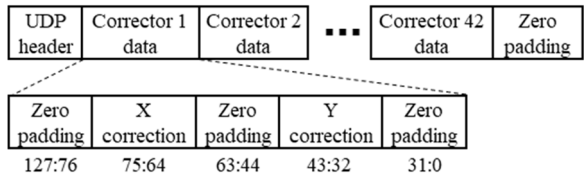

Figure 8: Correction data grouping packet structure.

FUTURE DEVELOPMENT

The ZYNQ processor has 4 integrated ARM Cortex-A53 CPU cores. We have the intention to port our EPICS IOCs onto them. With the embedded EPICS IOCs, the communication between EPICS and the EOD firmware can be simplified by replacing the Gigabit Ethernet interface and Control System Interface modules with the on-chip AXI4-Lite bus and memory mapping. This means the registers of the FPGA portion are given memory locations in the CPU's memory space and then can be written to and read from like any normal memory locations from the CPU.

CONCLUSION

The expanded processing capacity of the EOD system will allow research in a real-time diagnostic system that can provide information on the electron beam parameters that could be used during user operations. This information can be used to stabilize the photon beam size locally during insertion device movements.

To provide a smooth and low impact upgrade to the existing FOFB system, which is relied upon during user operations, the EOD is fully backwards compatible. This is done by upgrading the central processor and extending the EPICS interface with new diagnostic commands.

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