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# A NEW TYPE OF DIGITAL FREQUENCY MULTIPLIER*

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ABSTRACT

This article describes a new technique for frequency multiplication using digital methods. The method is primarily useful for low frequency multiplication, and generates equally spaced pulses, although there is a small error due to truncation.

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This note describes a new type of frequency multiplier, based strictly on digital techniques, which is primarily useful at low frequencies. Phase lock loops (PLL) are the conventional lower cost approach to frequency multiplication, using a divide by N counter in the feedback path, but PLL present design difficulties, and may have excessive jitter, particularly at low frequencies with large N. Digital frequency multipliers, or rate multipliers, exist, but these usually do not generate equally spaced pulses.

The multiplier technique described here is all digital and generates equally spaced pulses, although there is a small error due to truncation. The basic concept, shown in Fig. 1, is to measure the trigger interval T in the counter, then to use this information to generate N pulses for the next interval. Hence the pulse spacing is determined by the previous trigger interval, and true multiplication is achieved.

The system basically consists of a clock, of frequency $F_c$, which only has to be stable over the interval 2T, a divide by N counter, an accumulator counter, and a divide by M counter. The accumulator counter counts to M during the trigger interval; at the end of the cycle the count M is transferred to the divide by M counter and the clock rate $F_c$ is divided by M for the final output.

Hence

$$M = \frac{F_c}{N} \times T \tag{1}$$

$$\text{Output Rate} = \frac{F_c}{M} = F_c \times \frac{N}{F_c} \frac{1}{T} = \frac{N}{T} \tag{2}$$

which shows that the desired multiplication is achieved. An error occurs when M is truncated to an integer in measuring the trigger interval T. As a result, the intervals, although always identical, are not quite equal to $\frac{T}{N}$. It is easily

seen that the worst case error is when a full cycle is truncated from M; hence, from Eq. (1),

$$\text{Pulse Spacing Error, } E_s = \frac{N}{TF_c} \tag{3}$$

This gives the worst case error in the individual pulse spacing relative to the true pulse spacing, and shows that the relative error is proportional to N, and inversely proportional to T and $F_c$. For a given N and $F_c$ the relative error is cyclic in T, as shown in Fig. 2.

At the end of the period T there is a worst case accumulated time error given by

$$\text{Accumulated Time Error, } E_{AT} = \frac{N}{F_c} \tag{4}$$

which again shows that the error is inversely proportional to $F_c$ as expected.

The errors in a typical case are quite low. For example, when T = 1 s, $F_c$ = 20 MHz and N = 256, the worst case pulse spacing error is 0.00128%, corresponding to 0.05 $\mu$s. The accumulated time error at the end of the 1 s period is 12.8 $\mu$s, corresponding to 0.33% of T/N. For this particular case the cyclic variation of the error is shown in Fig. 2.

By using Eqs. (3) and (4) one can determine the necessary clock rate for a given error limit. This in turn determines the size of the accumulator counter M and the divide by M counter from Eq. (1).

FIGURE CAPTIONS

1. Simplified block diagram.
2. Accumulated time error for N = 256, $F_c$ = 20 MHz.

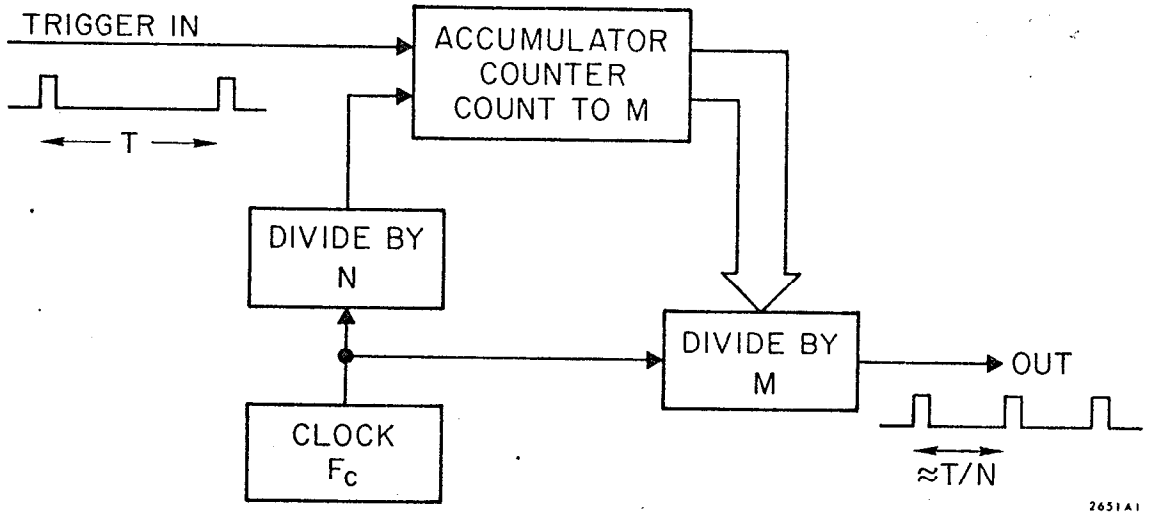
TRIGGER IN
T
ACCUMULATOR
COUNTER
COUNT TO M
DIVIDE BY
N
DIVIDE BY
M
OUT
CLOCK
Fc
≈T/N
2651A1

Fig. 1

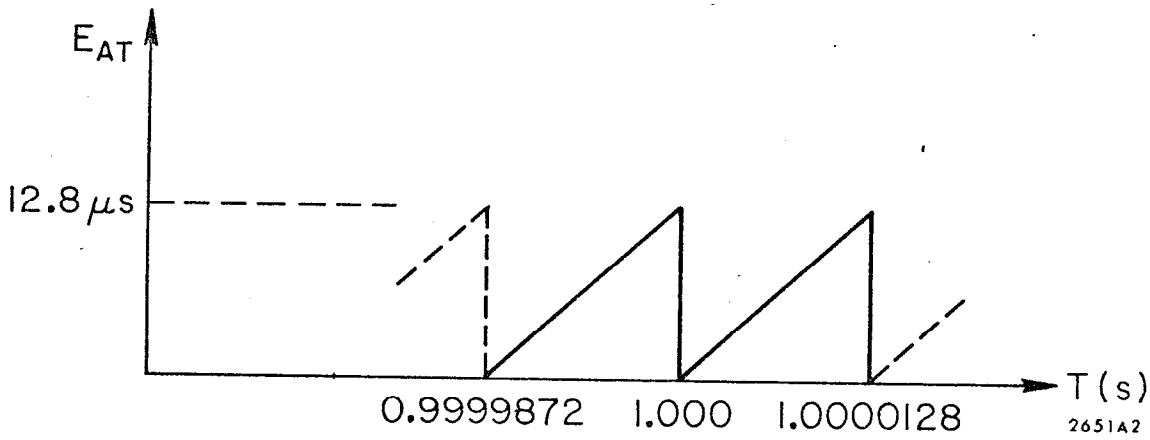
EAT
12.8 μs
T (s)
0.9999872
1.000
1.0000128
2651A2

Fig. 2