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THE DESIGN OF SILF FAST ORBIT FEEDBACK SYSTEM

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Abstract

The Shenzhen Innovation Light Source Facility (SILF), as a 4th light source, is an accelerator-based multidiscipline user facility planned to be constructed in Shenzhen, Guangdong, China. It has stringent requirement for beam orbit stability: the orbit fluctuations should be below 10% of the beam RMS sizes in both horizontal and vertical directions with a bandwidth around 500Hz. The fast orbit feedback system (FOFB) is designed to correct beam orbit in the storage ring, by calculating correctors strength change to correct beam orbit error detected by the beam position monitors (BPMs). The FOFB with field programmable gate arrays (FPGA) is supposed to be achieved, to reduce feedback latency and increase bandwidth. In this paper, the structure of SILF FOFB, the structure of its electronics system and its hardware and software subsystems are designed.

INTRODUCTION

The SILF is a fourth-generation medium-energy synchrotron radiation light source that envisions a future with over 50 beamlines. Its primary focus lies in supporting the development of domestic core industries, advancing frontiers in basic science research, and addressing strategic imperatives, including integrated circuits, bio-medicine, advanced materials, and advanced manufacturing.

The accelerator complex is composed of a 200 MeV linac, a booster with ramping energy from 0.2 GeV to 3.0 GeV, and a 3.0 GeV storage ring as shown in Figure 1. Two transport lines are designed to connect the linac, booster and storage ring. The circumference of the storage ring is 696 m, which includes 28 hybrid seven-bend achromat (H7BA) lattice periodic units to achieve the emittance below 100 pm·rad. The top-up operation mode (300 mA, 928 bunches) is considered, and a brightness of about 10^{22} s^{-1} mm^{-2} $m{\cdot}rad^{-2}$ $(0.1\%\ bandwidth)^{-1}$ is expected at the photon energy of 10 keV, as illustrated in Figure 2 [1, 2].

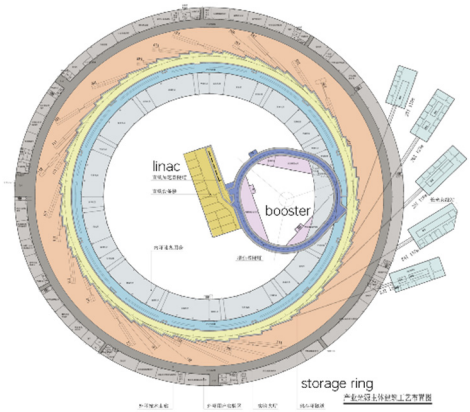

Figure 1: Schematic layout of the SILF project.

With the enhanced requirements of new synchrotron light sources and the fast development of electronic techniques, the beam orbit stability in μm level can be achieved by the FOFB with a bandwidth of several hundred Hz based on large-volume FPGAs. For SILF, there are 28 H7Bas with 12 BPMs and 12 fast correctors along the 696 m storage ring, 336 BPMs' data in both horizontal and vertical directions need to be collected and delivered to all of the FOFB sub-stations. It responds to orbital perturbations from 0.01 Hz to 500 Hz frequency range in feedback periods of tens of microseconds, which is different from slow orbit feedback system (SOFB) [3, 4].

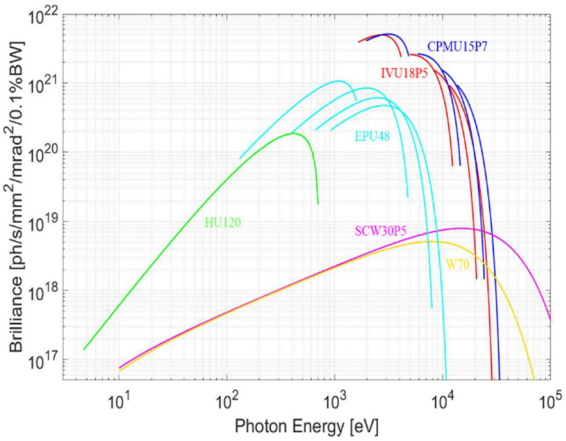

Figure 2: The available spectral brightness for SILF operated in the high brightness.

REQUIREMENT

There are many factors that affect the stability of the beam orbit, including the stability of the magnet power supply, ground vibration, temperature effects, etc.

According to ring accelerator physical design and requirements, there are BPMs to monitor the orbit and many correctors to correct the orbit in the storage ring. In order to suppress interference and keep the beam orbit stable, it is we adopt a high-intensity and high-speed orbit feedback system, a typical multiple-input and multiple-output (MIMO) system, to achieve long-term stable operation of the light source based on singular value decomposition (SVD) commonly.

The correction algorithm is based on an SVD of the orbit response matrix:

$$\Delta\overline{X} = R\,\Delta\overline{\theta} \quad and \quad R = USV^T$$

$$\Delta\overline{\theta} = VS^{(-1)}U^T\,\Delta\overline{X}, \tag{1}$$

where $\Delta\overline{X}$ is error that the current orbit is compared to the golden orbit, U and V are matrices whose columns form an

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orthogonal basis in BPM(X) and corrector magnet θ space, S is the diagonal matrix of singular values. The proportional-integrator (PI) control algorithm operates in this diagonal space and the relevant parameters can be adjusted for each mode separately. All multiplication and calculations stages are done for all eigenmodes at one cycle. Therefore, it is necessary to comprehensively consider the whole time consuming, including the speed of BPMs data acquisition, the delay of global BPMs data distribution and calculation, and other factors [5].

ARCHITECTURE

We adopt the architecture of daisy-chain based on 28 sub-stations, each sub-station is responsible to interact with local BPMs and fast corrector power supplies. The 336 BPM channels with two pieces of data transferred by each channel are divided into 28 groups equally, and data is collected by each sub-station with point-to-point connections first, then broadcasted to all of the sub-stations along the ring, as shown in Figure 3. The feedback logic of FOFB is shown in Figure 4.

The fast correctors are also divided into 28 groups equally. In total, 12 GTHs (RocketIO named in Vitex7 FPGA manuals) at a line rate of 2.38 Gbps are used in each FOFB sub-station to collect the data from the 12 BPM modules. The global transmission links are bidirectional along the ring to broadcast the BPM data to all sub-stations in only half a ring at a line rate of 4.76 Gbps in each direction.

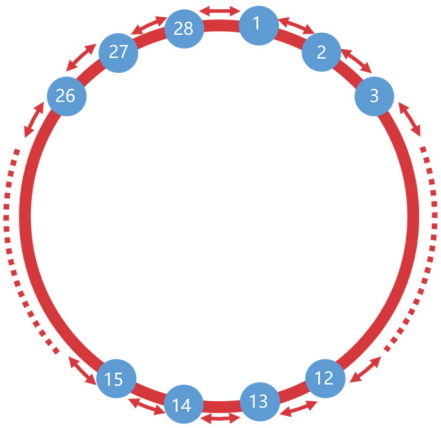

Figure 3: Layout of FOFB architecture.

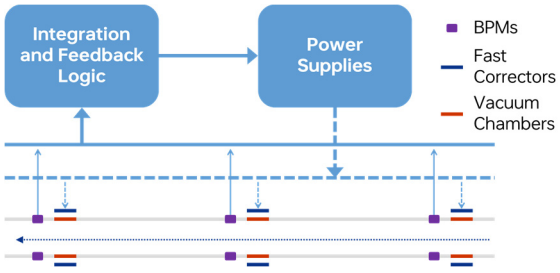

Figure 4: Feedback logic of FOFB.

SIMULATION

The feedback method based on the inverse response matrix and PID control is mature and applied widely, thus it is adopted in the implementation of the FOFB system. The FOFB applies feedback algorithm and parameters used, as shown in Figure 5 and Table 1. It is optimized to calculate the large matrix based on the singular value decomposition (SVD) taking the digital signal processing (DSP) modules of FPGA with parallel pipe-line. The FOFB establishes feedback simulation model, as shown in Figure 6.

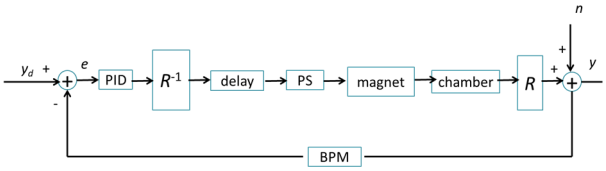

Figure 5: Feedback Algorithm.

Table 1: Parameters used of FOFB

Noun	Parameter
PID	*PI controller*
R	*response matrix*
Delay	*calculation delay 40μs*
PS	*step response: 70μs to 95% amplitude*
Magnet	*same as PS*
chamber	*0.8mm thick Inconnel 625, inner diameter 22mm*
N	*noise*
BPM	*delay 2.5μs*

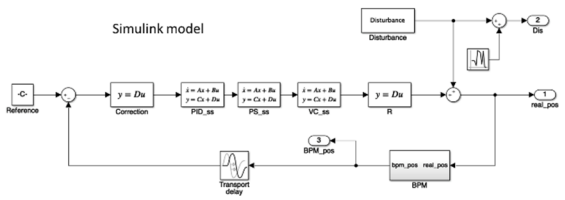

Figure 6: Simulink model of FOFB.

HARDWARE DESIGN

Considering the stability and reliability for long-term operation and future upgrade, the backplane of FOFB is adopt a large-capacity, high-density architecture.

The architecture of FPGA meets both demands of 4th light source, with RocketIO for high-speed data transmission and built-in DSPs for high-precision data operation. An FPGA with 80 RocketIOs and 3600 DSPs from Xilinx is chosen due to the overall evaluation of the requirements, the chip performance and the cost.

Therefore, the FOFB is designed as circular distributed synchronous architecture, where 28 sub-stations using XILINX Virtex7 devices with RocketIO channels and DSP units are evenly distributed on the storage ring, and each sub-station corresponds with 12 BPMs and 12 fast correctors, and with the same hardware and software function to obtain bias-data from BPMs data using 2.38 Gbps in the SFPs and send correct-data to the fast corrector power supplies using a serial point-to-point link around the storage

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ring, and each substation share BPMs data with daisy-chained using of 10Gbps in the SFPs.

The self-developed main logic backplane board and front board followed the ATCA mechanical size. For performance tuning and additional flexibility when adding or removing BPMs and fast corrector power supplies, or downloading new matrix, an embedded Ethernet controller is designed as a full hardwired TCP / IP providing internet connectivity to sub-station by using Serial Peripheral Interface (SPI).

DATA TRANSMISSION

A bit width of 32 between the BPM modules and the FOFB sub-stations is used to collect the effective 24-bit signed fixed-point beam position data. The beam-position data is then encoded into 64 bits for global transmission. The 8B/10B encoding is used to reduce the bit error rate during data transmission, thus the total transmitted bit width is 40 for the raw beam position data and 80 for the globally encoded beam position data. K28.5 codes are used for the phase alignment in each GTH link [6].

The beam-position data is transferred and stored in sequence in the global block memories. The group data is further divided into two consecutive parts for calculation. Consequently, there are total 56 groups of BPM data with 12 pieces of data in each group. For each group of data, we define the start address as the group address. For each substation, the globally encoded BPM data comes from 2 links in both sides concurrently, so the buffers are set for each link.

The group addresses are extracted from the global BPM data, according to the group address and the buffer identifier, the write control logic moves the data from the buffers to the global block memories with priority algorithm, the group address is written into the interrupt FIFO at the same time, as shown in Figure 7. The read control logic reads the addresses from the FIFO in sequence, according to which it reads the corresponding data from the global memories to the data calculation pipeline. Lock-protection is designed in the write control logic to avoid inconsistency. A 56-bit register is designed to indicate the successful reception of each group of data.

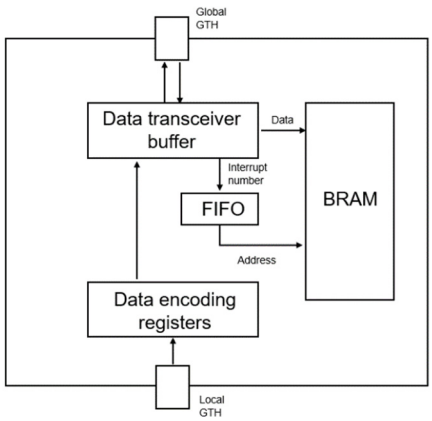

Figure 7: Logic architecture of data encoding and transmission of FOFB.

The parameters of inverse response matrix and PID control are also stored in block memories. All the block memories are used in dual-port mode to do writes and reads concurrently. Each group of BPM data and its corresponding parameters are stored in parallel in the block memories and can be read out simultaneously with one clock pulse.

CONCLUSION

The SILF project received approval from the Shenzhen Government on September 10, 2020. The feasibility study was successfully completed in 2022, and the preliminary design phase is currently underway. Detailed plans for the construction phase of the project are currently being developed. In order to reduce the system response time as much as possible and improve the effective feedback band-width of the FOFB system, we propose a hardware architecture that can quickly obtain all BPMs data in the storage ring, and quickly complete large data calculations, and send the setting to the fast corrector power supply in real-time, which also meets the main requirements of the SILF project.

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