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PROJECT PROGRESS OF LLRF FOR THE SUPERCONDUCTING RF SYSTEM OF HEFEI ADVANCED LIGHT FACILITY (HALF)*

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Abstract

The Superconducting RF system of Hefei Advanced Light Facility (HALF) can provide an accelerating electric field for the beam, and its stability is required to be of RMS ≤ 0.1% in amplitude and RMS ≤ 0.1° in phase. To achieve this, a LLRF controller is being prepared for the control of the HALF Superconducting RF system. This LLRF controller mainly consists of three modules of RF front-end, signal processing and the motor drive. The RF front-end downconverts the RF signal to the IF of 31.2375MHz (499.8/16), and then up converts the IF to the RF after being processed by the digital board. The LLRF includes four channels of down conversion (cavity sampling signal P_t, forward power signal P_f, reflected signal P_r and the reference signal P_{ref}) and one channel of up conversion (power source drive signal). LLRF can realize three control loops and one interlock protection, namely cavity frequency tuning loop, cavity field amplitude control loop and cavity field phase control loop. The project progress of the HALF LLRF system will be introduced in this manuscript in detail.

INTRODUCTION

A superconducting RF cavity will be used in the storage ring of Hefei Advanced Light Facility (HALF). Compared with a normal RF cavity, the superconducting RF cavity has many advantages, such as its low power loss, large beam aperture, good higher-order mode suppression performance [1], which has been widely used in other advanced light sources [1-2].

During the operation of superconducting RF system, the stability of its operation will be affected due to the existence of microphonics effect and beam load effect [3]. The excellent performance of the HALF superconducting RF cavity depends on the stable operation of the RF system, in which the stability of the accelerating voltage mainly depends on the control of the Low Level RF system. According to the physical design requirements of HALF storage ring, the amplitude stability of the cavity pressure RMS ≤ 0.1%, and the phase stability RMS ≤ 0.1°. At present, the project progress of the HALF LLRF for the Superconducting RF system is shown as follows.

WORKING PRINCIPLE AND COMPOSITION OF HALF LLRF

The 499.8 MHz superconducting RF system of the HALF storage ring is planned to adopt the digital Low Level RF system (LLRF), which is responsible for measuring and feedback control of the high frequency accelerating electric field in the superconducting cavity and the central frequency of the superconducting cavity, mainly composed of RF front-end, digital processing board, etc [4]. The composition of the whole LLRF control system is shown in Figure 1.

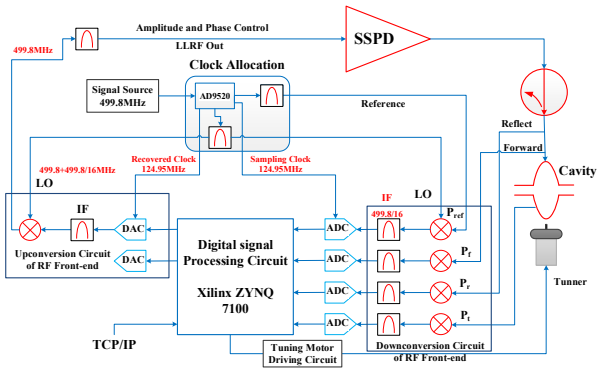

Figure 1: Overall structure diagram of HALF LLRF.

HALF LLRF can first perform analog down-conversion of the incident signal P_f, reflected signal P_r, cavity sampling signal P_t and reference signal P_{ref} from the signal source. After the intermediate frequency band-pass filtering, the high-speed ADC performs high-precision digital-to-analog conversion of the intermediate frequency (IF) signal, and then performs digital I/Q quadrature demodulation and CORDIC phase demodulation to obtain the amplitude and phase of the IF signal of P_t . After comparing the above signal with the IF signal of P_{ref}, the FPGA digital processing circuit conducts PI adjustment on the P_t IF signal, and then the DAC outputs the adjusted IF signal. After band-pass filtering, the RF front-end circuit performs the analog up-conversion to obtain a new drive signal, which is input into the solid-state power source for power amplification.

Table 1: Main technical parameters of HALF LLRF

Serial number	Technical parameter	Specific indicators
1	Phase loop	Closed-loop feedback control accuracy can reach RMS ≤ 0.1° (within 1s)
2	Amplitude loop	closed-loop feedback control accuracy can reach RMS ≤ 0.1% (within 1s)
3	Autotune	Tuning range can reach ±200kHz, tuning accuracy can reach 10Hz, and working bandwidth is 48Hz

At the same time, the FPGA signal processing circuit uses CORDIC phase discrimination to obtain the phase of

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P_f and P_t for comparison, to obtain the detuning angle, and then drives the motor for the frequency tuning to adjust the frequency of the superconducting cavity, so that it works at the center frequency of 499.8MHz.

According to the requirements of the physical design of HALF storage ring, the main technical parameters of superconducting main RF LLRF system and interlocking protection system are listed in Table 1.

DEVICE TYPE SELECTION OF THE KEY MODULE COMPONENTS

RF Front-end

For devices for the RF front-end, especially mixers and amplifiers, it is necessary to carefully consider SNR, noise figure and other requirements to select appropriate types, and determine operating points of the mixer and amplifier according to the calculation of noise figure.

Considering the parameters and functional requirements to be achieved, AD8342 active mixer is selected as the core device of the RF front-end circuit, with the main frequency range of 1MHz~3.8GHz, the maximum input P_{1dB}=8.3dBm, and the IP3 crossover point of 22.7dBm. In terms of interface, RF and LO can be easily converted to single-ended access, while IF port is the output of open collector and requires DC bias, the circuit of which is shown in Figure 2 [5].

The IF amplifier of RF front-end uses ADA4938. It is a low-noise, ultra-low distortion, high-speed differential amplifier, which is very suitable for driving high-performance ADC with resolution up to 16 bits, DC to 27MHz or resolution up to 12 bits, DC to 74MHz.

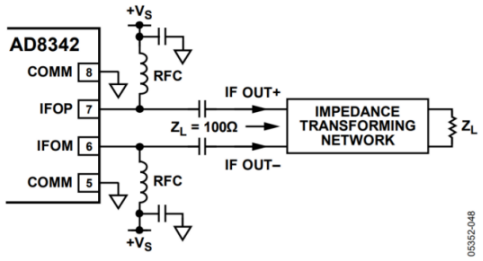

Figure 2: AD8342 bias circuit.

The RF amplifier for the up-conversion uses the PMA-5454+ low-noise single-ended amplifier of Mini-Circuits. Its bandwidth and noise figure are also considered in the selection. At the same time, it can also be replaced between different types of the same package and devices with the same pin electrical properties according to the actual needs.

After the working points of the mixer, IF amplifier and other main components are determined, the cascaded noise coefficient of the selected device is calculated. Then the SNR can be controlled in the range of 70~90dBc within the range of −10~10dBm RF input signal, which can leave a certain margin for the noise of the digital processing circuit. If the noise introduced by the digital system is ignored, the minimum value of the input RF signal can be further expanded to −18dBm.

Signal Processing Board

Clock distribution circuit

According to the overall structure of HALF LLRF in Figure 1, the frequency of IF signal is 499.8/16 = 31.2375MHz, and the frequency of system LO is 499.8/16 + 499.8 = 531.0375MHz. As to meet the requirements of the I/Q orthogonal sampling, the ADC sampling frequency should meet the formula of $4 / (4N+1) \times f_{IF}$. So when N=0 is brought in this formula, $4 \times f_{IF} = 124.95$MHz is obtained. Similarly, the DAC recovery frequency is also set to $4 \times f_{IF} = 124.95$MHz.

The clock distribution circuit is proposed to use the output clock generator chip AD9520. Its internal VCO frequency range is 2.53~2.95 GHz. Each three outputs share one output divider. The frequency division ratio is adjustable from 1 to 32. The frequency change caused by temperature change is generally in the order of tens to hundreds kHz [6].

Digital signal processing board based on FPGA

ADC sampling of the IF signal, digital signal processing and DAC recovery functions are all completed by the FPGA digital signal processing board. The main control chip of the board is Xilinx ZYNQ 7100. ZYNQ 7100 chip have a dual-core ARM Cortex-A9 processor and integrated a 28nm FPGA of high performance to achieve power consumption and performance level far higher than that of discrete processors or FPGA chips [7].

The ADC of the digital signal processing board adopts two LTC2185 chips with dual channels, 16bit bit width, and the maximum sampling rate of 125Msps. Its DAC adopts one ISL5927 chip with dual-channel, 14bit bit and has a maximum sampling rate of 260Msps. It can be seen that the selection of the above devices both can meet the requirements of ADC sampling and DAC recovery [8-9].

FREQUENCY TUNING AND AMPLITUDE AND PHASE CONTROL ALGORITHM

The control of HALF LLRF on the superconducting RF system mainly includes frequency tuning and amplitude & phase control. The realization of these controlling is based on the closed-loop feedback control, which includes frequency tuning loop and amplitude & phase control loop [10].

The Frequency Tuning Loop

The phase difference between the input RF signal P_f and the sampling signal P_t on the cavity is called the detuning angle φ of the RF cavity, which has the following relationship between P_f and P_t.

$$\tan\varphi = 2Q_L\left(\frac{\omega_r - \omega_c}{\omega_c}\right) \quad (1)$$

From this equation, it can be seen that the detuning state of the superconducting RF cavity can be obtained by measuring the detuning angle φ [11].

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When the detuning angle exceeds the set threshold, HALF LLRF will control the tuner to perform cavity frequency mechanical tuning on the superconducting RF cavity. The axial range design value of the tuner of the HALF superconducting RF cavity is ± 200kHz, with a sensitivity of 10Hz.

Amplitude and Phase Control Loop

The amplitude and phase of the RF acceleration field in the superconducting cavity are controlled by the LLRF amplitude and phase control loop. The reference signal P_{ref} and the cavity sampling signal P_t are downconverted with the RF front-end of the LLRF system, then the bandpass filtering is used to remove their higher-order harmonics, and then converted into a digital signal after ADC sampling. Four orthogonal I/Q components are obtained using the I/Q orthogonal demodulation algorithm, which can calculate the amplitude and phase of the intermediate frequency signals of P_{ref} and P_t.

The phase difference of intermediate frequency signals between P_{ref} and P_t can greatly affect the closed-loop, so FPGA is used to construct a digital phase shifter to adjust the phase of P_t and reduce the phase difference between P_{ref} and P_t. Then the I and Q components of P_{ref} and P_t are adjusted with the PI algorithm to obtain a new I/Q array. With the I/Q array, the signal recovery algorithm is used to obtain a digital sequence that can be converted into D/A, and finally restored to an analog intermediate frequency signal through DAC. Then, it is input into the RF front-end for upconversion. The intermediate frequency signal is upconverted as a driving signal, which is input into a solid-state power source. The power source then outputs a 499.8Mhz high RF power with stable amplitude and phase into the superconducting cavity, which can generate an equally stable accelerating electric field.

PC Control Software for HALF LLRF

In the near future, referring to the interface of SSRF LLRF (Figure 3), the PC control software of HALF LLRF of the superconducting RF system will be compiled with Labview for its working parameters configuration and real-time data monitoring [12].

Figure 3: SSRF configuration and monitoring interface.

SUMMARY

Based on the above progress, the members of the superconducting main high-frequency project team will comprehensively promote various construction tasks, including the detailed design, customization, processing, debugging and installation of HALF LLRF.

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