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J. Hoff et al.

Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510

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SMQIE: A Charge Integrator and Encoder Chip for the CDF Run II Shower Max Detector[1]

J. Hoff[2], G. Drake[3], A. Byon-Wagner[2], G. Foster[2], M. Lindgren[4]
[2]Fermi National Accelerator Lab*
[3]Argonne National Lab
[4]University of California at Los Angeles

Abstract

The Technical Design Report for the CDF II Detector calls for the development of an imbedded two-dimensional position sensitive detector sandwiched inside the electromagnetic calorimeter and placed at the shower maximum. The purpose of this detector is to aid in the identification of electrons and photons, to separate photons from π^0s, and to help identify electromagnetic showers. This detector is called the Shower Max.

In order to achieve CDF's goals for resolution, timing, power and economy, as well as to fit into the available space, a full-custom integrated circuit was required for the project - the SMQIE.

The SMQIE has been fabricated in a 1.2μm CMOS process using vertical NPN transistors in critical areas. It operates without deadtime. Its QIEs have eight ranges and an overall dynamic range of 13 bits. Its FADCs have a 5-bit resolution with a nominal LSB of 31.25 mV. Its Level 1 Trigger delays are 42 beam crossings or approximately 5.5 μs. Its data buffers hold up to four events, each of which can consist of four time slices. Finally, the chip accepts a maximum input charge up to 150 pC with a minimum resolution of 15 fC.

I. Introduction

Charge Integrator and Encoders or QIEs are a family of integrated circuits that have been under development at Fermilab for several years [1][2]. Simply put, they are analog-to-digital converters. More specifically, they convert an input charge into a number in scientific notation. This is achieved by splitting the input charge into multiple (typically eight) binary-weighted, non-overlapping ranges, integrating these split signals, and, based on these integrations, selecting a single range. The selected range is encoded into an exponent and the integrated signal in that range is converted into a mantissa by a Flash converter (FADC).

The SMQIE is the newest member of the QIE family, designed specifically for the Shower Max detector at CDF [3][4].

From its inception, the SMQIE was required to be "self-contained" and "easily used". "Self contained" means that the chip must require a minimum of external circuitry in order to operate. "Easily used" means that the SMQIE was constrained to use available power supplies and clocks. Therefore, unlike previous QIEs, the SMQIE operates simultaneously in a 0-5v range and at the beam-crossing frequency of 7.6MHz. Moreover, it monolithically integrates two complete channels each of which contain a QIE, an FADC, a data synchronizer, a Level 1 Trigger FIFO and a Triggered Data Buffer. This is far more digital circuitry than has ever previously been integrated with a QIE front-end. The complete block diagram is shown in Figure 1.

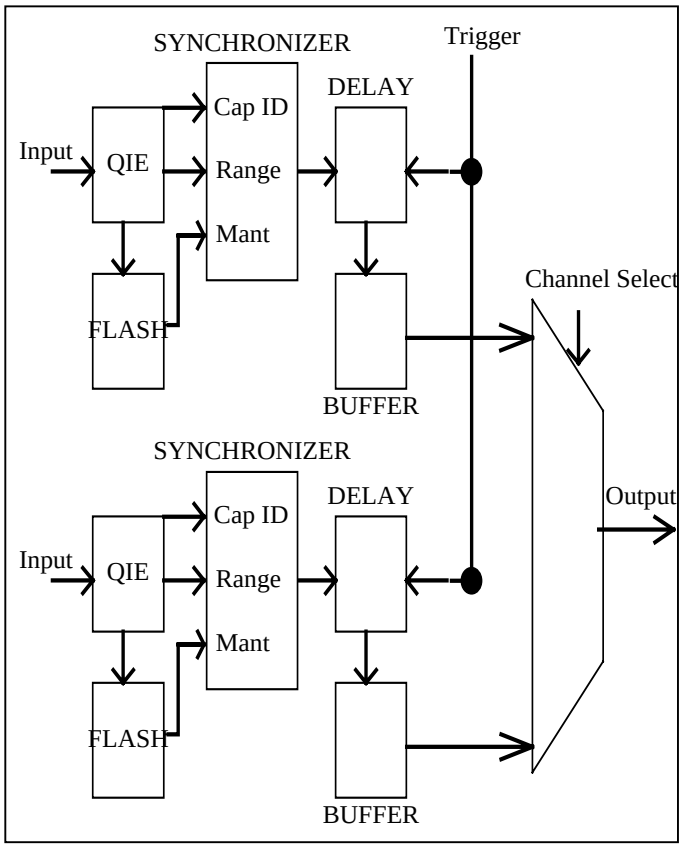

Figure 1: A Block Diagram of a complete SMQIE

The more specific requirements of the SMQIE are displayed in Table 1. In the following sections, each element of the channel architecture shown in Figure 1 will be discussed individually. Finally, the results of the entire chip will be shown and its performance relative to the design requirements will be discussed.

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Table 1 : SMQIE Design Specifications

Full Scale Input Charge	100 pC
Number of Ranges	8
FADC Resolution	5-bit
LSB Resolution on I/2	12.5 fC
Overall Precision	12.5 fC or 3% (whichever is greater)
Input Frequency	7.6 MHz (1/132 ns)
Output Voltage Levels	LVDS standard
Number of Channels	2

II. The QIE Front End

The architecture of the SMQIE front end is shown in Figure 2.

The Splitter divides the input charge into eight binary-weighted, non-overlapping ranges. It consists of 128 bipolar transistors in a common base configuration. The emitters are all joined to form the input of the QIE. The collectors are joined into groups of 64 (Range0), 32 (Range1), 16 (Range2), 8 (Range3), 4 (Range4), 2 (Range5), 1 (Range6) and 1 (Range7). Signal current is added to a bias current at the emitters of the Splitter to form the input current, I. At the collectors then are the currents I/2 (Range0), I/4 (Range1), I/8 (Range2), I/16 (Range3), I/32 (Range4), I/64 (Range5), I/128 (Range6) and I/128 (Range7).

The Cascode block in Figure 2 is essential to Splitter operation because it keeps the collector voltages constant ensuring a constant split ratio. In fact, the single Cascode block in Figure 2 is eight independent Cascode blocks, one per range. A single reference voltage is fed to all eight ranges, keeping all of the Splitter's collector voltages constant and equal, but each range has its own cascode transistor and its own cascode feedback amplifier to regulate those collector voltages. Both the cascode transistor and the feedback amplifier are scaled by range. This helps ratio parasitic charge loss among the ranges. For further information on parasitic charge loss see [2].

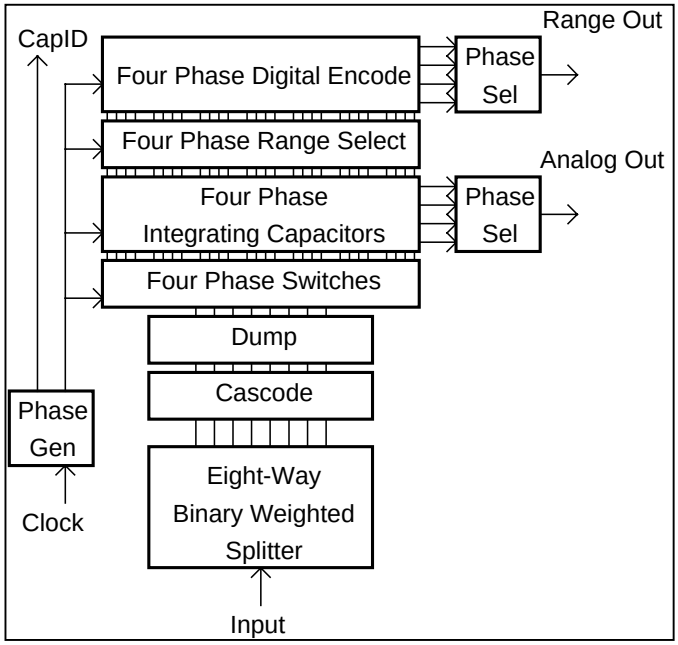

Figure 2: SMQIE Front End Architecture

For large current inputs, when the higher ranges are of interest, very substantial currents will flow in the lower ranges. These large currents can exceed the capability of the Cascode block to regulate the collectors of the Splitter, which, in turn, can effect subsequent time slices. The purpose of the Dump block in Figure 2 is to help eliminate excessive currents and prevent them from upsetting the front end.

The QIE process fits well into four phases. In phase one, a signal is integrated (Integrate Phase). In phase two, the integrated signal is evaluated and a range is selected (Evaluate Phase). In phase three, the selected range outputs its analog voltage (Output Phase). Finally, in phase four, the integrating capacitors are reset to prepare for their next event (Reset Phase). To take advantage of this, all of the blocks in Figure 2 above the Dump are pipelined into four phases to ensure dead-timeless operation. The Phase Gen block produces the appropriate phase signals for all blocks from a simple input clock. It also generates the Capacitor Identification (CapID) as a diagnostic.

The Four-Phase Switch in Figure 2 connects one integrating capacitor per range to the Splitter. Every clock cycle, the Four Phase Range Select chooses an appropriate range from the integrated signals on the capacitors that are in the Evaluate Phase. The Four-Phase Digital Encoder converts this selected range into a 3-bit number. During their Output Phase, the Phase Select block outputs these encoded range bits and the analog output for that range.

The 32 integrating capacitors (8 ranges times 4 phases per range) are all simple, open loop capacitors connected between the 5-volt power rail and the outputs of the Four-Phase Switch. Their design and layout are critical to performance since nonlinear parasitic capacitances must be balanced from phase to phase and from range to range in order to maintain linearity. Parasitic capacitances include the routing capacitance as well as the capacitances of the reset transistors, the Four Phase Range Select input transistors, the Four Phase Switch output transistors, and the Top Clamp (see Figure 3). The reset transistor is a simple pfet with its source connected to the 5-volt power rail and its drain connected to the anode of the integrating capacitor. During the reset phase, this transistor is activated and the capacitor is shorted to 5 volts. During all other phases, this transistor is inactive. The Top Clamp is a simple nfet transistor with its drain connected to the Dump Rail (5 volts) and its source connected to the anode of the integrating capacitor. It serves to augment the function of the Dump block in Figure 2. When an excessive current is flowing through a range, the voltage at the anode of the integrating capacitor will reach approximately one threshold voltage below the Top Clamp voltage. When this happens, the Top Clamp transistor begins to siphon the excess current away from the integrating capacitor. This helps a range to recover from overloads quickly.

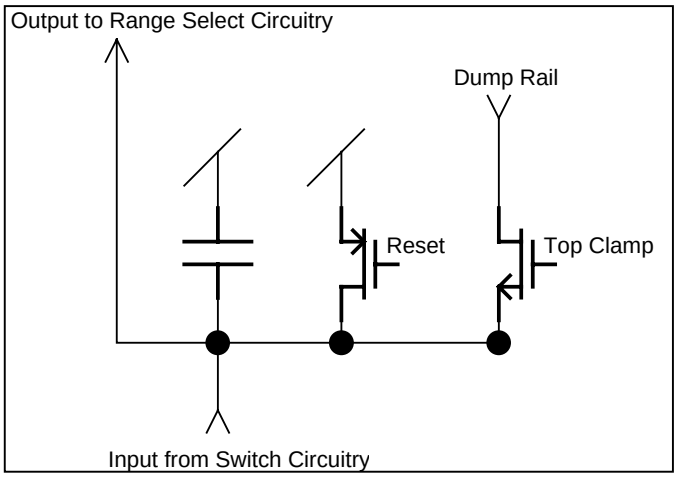

Figure 3: Integrating Capacitor Design

The total magnitude of the integrating capacitors, including parasitics, is defined by the required minimum resolution of the SMQIE (12 fC see Table 1). In order to understand this statement, it is necessary to understand how the SMQIE selects its range and analog output. First, the integrating capacitors are reset prior to the Integrate Phase. Therefore, the anodes of the integrating capacitors are at 5 volts. As charge is integrated on those capacitors, the voltage at the anode drops since the cathodes are tied to a 5-volt rail. The SMQIE is designed so that for any given input less than the full scale input charge, the voltages across the eight integrating capacitors will differ by factors of two and, and for any given charge, one and only one of the capacitor anodes will be between four and three volts. Four volts on any range would be converted by the FADC into 0 counts. Three volts would be converted into 31 counts. Obviously, if there is no input charge, Range 0 must be selected, and the FADC must output a zero. Therefore, in the absence of an input charge, the Splitter bias current must be large enough to bring the anode of the Range0 integrating capacitor to 4 volts in 132ns. Since the required resolution is 12 fC per count on the I/2 range, and there is a maximum of 31 counts, the I/2 range must cover 0 to 372 fC as the anode of the Range0 integrating capacitor drops from 4 to 3 volts. Therefore, since Q=CV where Q is charge (372 fC) and V is voltage (1 volt), the integrating capacitance, C, must be 372 fF. All Integrating Capacitors on all ranges are identical with the exception of the Range7 capacitors. These are made to be exactly double the capacitances of the other ranges (including parasitics). This doubling halves the sensitivity of Range7 and makes Range 7 handle twice the input charge as Range 6 in spite of the fact that they both receive I/128 currents from the Splitter.

The magnitude of the integrating capacitance defines the magnitude of the Splitter Bias current. In the absence of an input, the Splitter Bias current alone must be large enough to integrate 1 volt across the I/2 integrating capacitor. This means that the Splitter Bias current must be 6 μA (I/2 = C dV/dT where C is 372 fF, dV is 1 volt and dT is the beam crossing period, 132 ns).

When Range 0 integrates to 4 volts, the anode of the Range1 integrating capacitor is at 4.5 volts since it is being charge by I/4, the anode of the Range2 integrating capacitor is at 4.75 volts since it is being charge by I/8; etc. A full-scale Range0 input of 372 fC must place the anode of the Range0 integrating capacitor at 3. This would correspond to an average input current of 12 μA during one full Integrate Phase. This would place the Range1 capacitor at exactly 4 volts and the Range 2 capacitor at 4.5 volts, etc. By extension, it can be shown that regardless of the magnitude of the input charge, the integrating capacitor of one and only one range will be between 4 and 3 volts. The job of the Four-Phase Range Select is then to pick the first anode that has not dropped below 3 volts .

Note that unlike the KTeV chip [2], the choice was made not to use a differential QIE – i.e. a QIE with two splitters. In a differential QIE, the bias alone is supplied to one of the splitters whereas the sum of bias and the input charge is supplied to the other splitter. Range selection and analog output in a differential QIE are obtained from the voltage differences between the integrating capacitors of both splitters. The slower clock period (7.6 MHz as opposed to 53 MHz) as well as the less stringent resolution made the benefits of a differential QIE less significant to the Shower Max project than the increased complexity would have been.

Note also that the extremely small Splitter Bias current made for design problems especially with regard to the input impedance and the frequency response of the Splitter and the Cascode blocks. The solution was an excess current injector placed at the Splitter input and a series of scaled excess current extractors placed above the Dump block. These have been detailed elsewhere [5].

III. THE FADC

The SMQIE FADC is a straightforward 5 bit flash analog to digital converter. It has 31 comparators, which accept as input the analog output of the QIE front end. They also accept 31 unique reference voltages obtained from a simple voltage ladder between power and ground.

The output of the FADC is designed to flash 00000_2 for an input of 4 volts and 11111_2 for an input of 3 volts. This corresponds to the expected output range of the QIE. However, amplifier and comparator offset voltages can be considerable, and they can vary from run to run. Therefore, the FADC voltage ladder points corresponding to 4 volts (VladTop) and 3 volts (VladBot) are brought out to pads. If necessary, external resistors can be used to adjust the FADC ranges to correspond to the real, run-dependent QIE output voltages.

The FADC comparator used is a dynamic CMOS comparator similar to that found in [6]. It flashes on the positive edge of each clock cycle. This provides the QIE one full Output Phase (132ns) with which to settle the analog output voltage of the QIE onto the input of the FADC.

IV. TRIGGER PIPELINE DELAY

Though it represents a very significant percentage of the area of the chip (almost 10000 transistors), the Level 1 FIFO is actually very simple. It is a 10-bit wide, 38-stage deep FIFO.

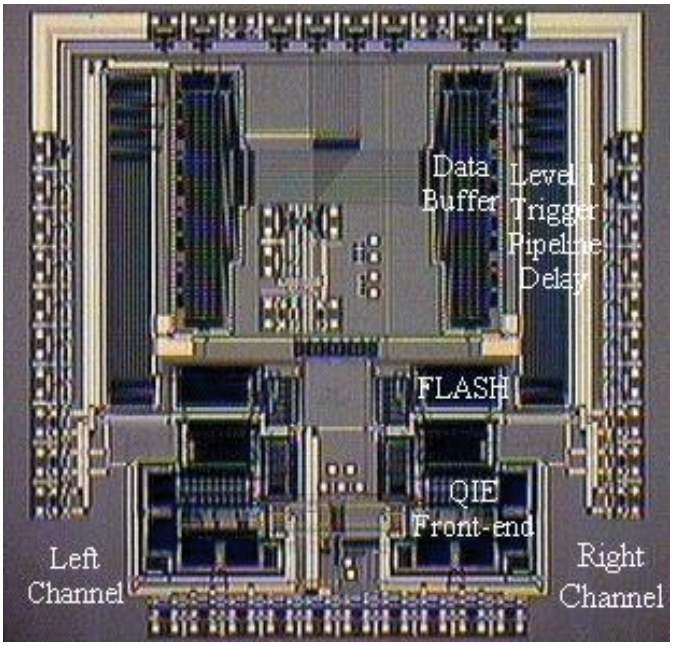

Figure 4: An image of a working SMQIE chip

All elements of the FIFO are synchronized to the falling edge of the BCO clock to ensure that all range and flash bits are fully stabilized before they are stored in the FIFO.

In order to be useful to both the Plug and Central Calorimeter systems, the SMQIE has to be customized to handle the outputs of either system. The Shower Max detector in the Plug calorimeter uses fast multi-anode photo multiplier tubes, which output all their charge in one BCO clock cycle (132 ns). The Shower Max detector in the Central calorimeter, on the other hand, uses slower strip chambers, which output their charge over four time slices. When a trigger is received, therefore, output from the Central Shower Max must be the sum of the triggered time slice and the three subsequent time slices. In order to accommodate this, the outputs of the 38th, 37th, 36th, and 35th stages of the FIFO are output to the Buffer.

V. The Buffer

The Buffer holds the data for up to four different triggered events. In order to accommodate both the Plug and Central Calorimeters, each triggered event consists of the triggered time slice and the three subsequent time slices. Data Acquisition (DAQ) hardware for the Plug is only required to access the triggered time slice. DAQ hardware for the Central must access all four time slices and sum their magnitudes.

By the time a Level 1 Trigger is received, the SMQIE must know into which of the four registers it must place the four time slices of data. This is given by the Write Buffer number. A parity bit is generated for each time slice as it is being loaded into the Buffer.

To the DAQ hardware, the SMQIE looks like a 32-word memory with 11 bit wide words. Access to this memory is completely asynchronous. The five bits necessary to access this memory are as follows (from most significant to least significant):

1. **Channel Select** (1 bit) – selects which of the two channels is to be output. Prior to this point, the channels are completely independent.
2. **Read Buffer Number** (2 bits) – selects which triggered event is to be output
3. **Time Slice Number** (2 bits) – selects which time slice of the triggered event is to be output. 00 is the triggered time slice. 01, 10, and 11 are the next three time slices respectively.

VI. The Final Design

The final design is shown in Figure 4. The inputs are at the bottom. The digital inputs and outputs are all done using LVDS-like (low-voltage differential signaling) drivers and receivers. The only major difference between true LVDS and the LVDS-like drivers used in the SMQIE is that the SMQIE drivers can be tri-stated making the chip disabled. Tri-stating does not, however, interrupt current flow in the drivers since this might inject noise into the chip. Instead, internal resistors are switched in between the positive and negative LVDS outputs when the chip is disabled.

The final design is 6.4 mm on a side. It was designed in a 1.2μm CMOS process and has approximately 30000 transistors.

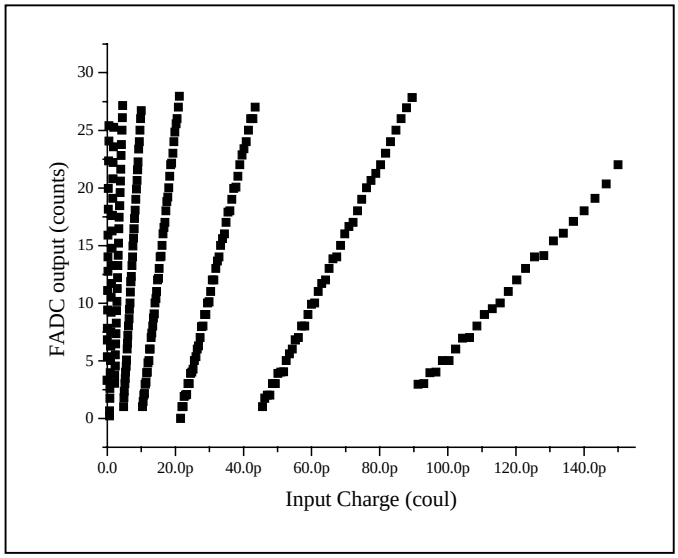

Figure 5: Typical SMQIE Output

VII. Test Results

The SMQIE has been extensively bench tested under conditions similar to the expected operating environment. Moreover, additional groups at Argonne National Lab and at the Fermi National Accelerator Lab are using the SMQIE in calorimeter wedge tests in anticipation of the start of Run II.

Figure 5 shows the output of the FADC as a function of fast charge input[1]. The ration of the slope (FADC output vs. charge) of a range to the slope of the next higher range should ideally be two. The accuracy of these "split ratios" in the SMQIE can be seen in Table 2.

Table 2 : SMQIE Split Ratios

Range	Slope	Ratio
0	4.30112e13	2.097
1	2.05122e13	2.013
2	1.01881e13	2.036
3	5.00374E12	1.987
4	2.51773e12	2.019
5	1.24693e12	2.023
6	6.16527e11	1.916
7	3.22532E11	-

Figure 6 shows an output charge reconstructed from Range and Mantissa values as a function of input charge. Each range has been individually calibrated. Also shown in Figure 6 is the fractional residual of the reconstituted charge. The vast majority of the residuals are well within the required ±3%. However, at very low input charges, a few residuals are as high as ±6%. This is due to the extremely small bias current forced on the SMQIE by voltage and frequency limitations. The low current flowing through the splitter and the cascode result in relatively high impedance at the collectors of the splitter transistors. For low input charges, there is some charge-loss into the next time slice.

The only real problem with the SMQIE is that the integrating capacitors were fabricated larger than the expected designed value. Of course, this is normal in modern VLSI processes in which the absolute value of a capacitance can vary by ±20% from run to run. Since the SMQIE's resolution relies on an absolute value in its integrating capacitors, the designers expect that the resolution will vary slightly from run to run. The principle effect of the larger capacitors is a change in the LSB resolution from 12.5 fC in I/2 to approximately 15 fC. This is not a significant problem, however, because increasing the gain of the pre-amplifiers between the detectors and the SMQIE can restore resolution. The larger capacitors also had the effect of increasing the maximum input charge to 150 pC.

VIII. Conclusion

The SMQIE is a multi-ranging integrator and range encoder with its own internal flash, pipeline delay and buffer. It has been designed and fully tested to operate at 7.6MHz over an input charge range of 0 to 150 fC. Finally, it meets the design requirements of the Shower Max Detector Project in all significant factors.

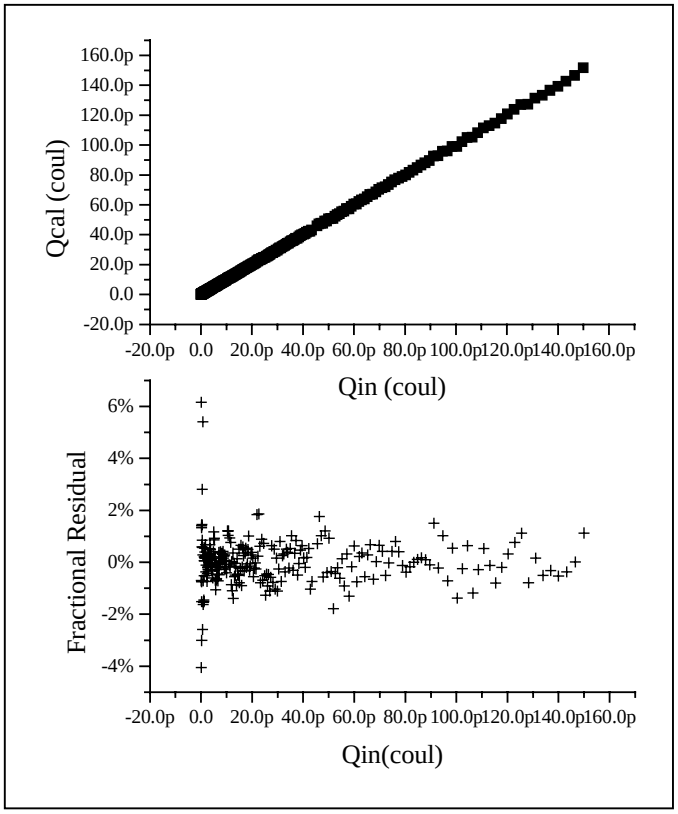

Figure 6: Reconstructed Charge Output vs SMQIE Charge Input

The SMQIE design team would like to acknowledge the invaluable help of several people. Ray Yarema and Tom Zimmerman acted as advisors throughout the project. Al Dyer did an excellent job of wire-bonding a large number of SMQIE chips for testing. Finally, Merle Watson drafted and stuffed, with endless patience, a whole flock of tester boards.

IX. References

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[4] The CDF II Detector Technical Design Report, FERMILAB-Pub-96/390-E, Chapters 8 and 9

[5] J. Hoff, "SMQIE: The Shower Max QIE Chip", FERMILAB-TM-2075

[6] N. Weste and K. Eshragian, Principles of CMOS VLSI Design, Second Edition, Addison-Wesley, 1993

[1] Fast charge input is a replication of the output of a photo multiplier tube. All charge is injected into the SMQIE in 50ns. Input capacitance is the same as that expected in the field.