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A Cryogenic Readout IC with 100 KSPS in-Pixel ADC for Skipper CCD-in-CMOS Sensors

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Skipper-CCD Sensors in Science

Charge-Coupled Device (CCD) image sensors, which operate by converting particle strikes into a localized "packet" of charge, are prevalent in both science and industry. Low noise readout of CCDs can be achieved through integrating the captured charge over a long period of time, but this technique is limited by low-frequency noise.

Skipper-CCDs overcome this challenge by reading the same packet of charge many times instead of performing one long integration, resetting between each read to cancel low-frequency noise. Skipper-CCDs offer best-in-class noise performance, and readout $\ll 1e^-_{rms}$ noise has been demonstrated with many samples.

A key challenge faced by all traditional CCD image sensors is readout speed, since charge packets are typically moved to the edge of the CCD pixel array for readout by peripheral electronics. Our work addresses this challenge by heterogeneously integrating a readout IC beneath the image sensor, effectively providing a dedicated ADC for every group of 3x3 pixels.

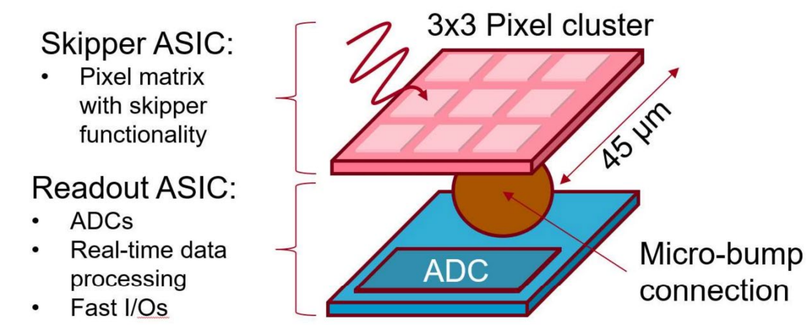
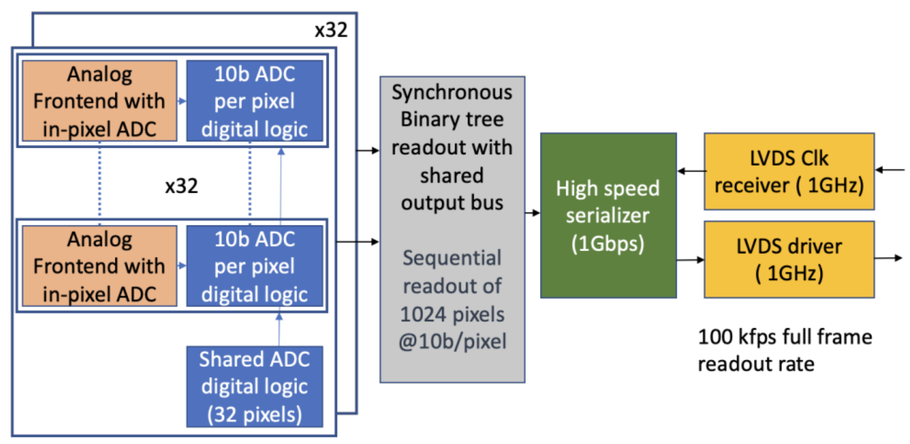


Illustration of the hybrid integration of the SPROCKET readout ASIC with a Skipper CCD-in-CMOS image sensor wafer.

The SPROCKET ASIC

The Skipper CCD-in-CMOS Parallel Read-Out Circuit (SPROCKET) is a mixed-signal front end design for the readout of Skipper CCD-in-CMOS image sensors. SPROCKET is fabricated in a 65 nm CMOS process, and each pixel occupies a $45\ \mu m \times 45\ \mu m$ footprint. SPROCKET is intended to be heterogeneously integrated with a Skipper-in-CMOS sensor array, such that one readout pixel is connected to a multiplexed array of nine Skipper-in-CMOS pixels to enable massively parallel readout.

Data captured by SPROCKET is read out (right) by a binary tree and serialized for off-chip transmission at 1 GHz. It is possible to read out all pixels in the array sequentially, but a parallel project is developing ML-based digital compression algorithms to enable higher frame rates.

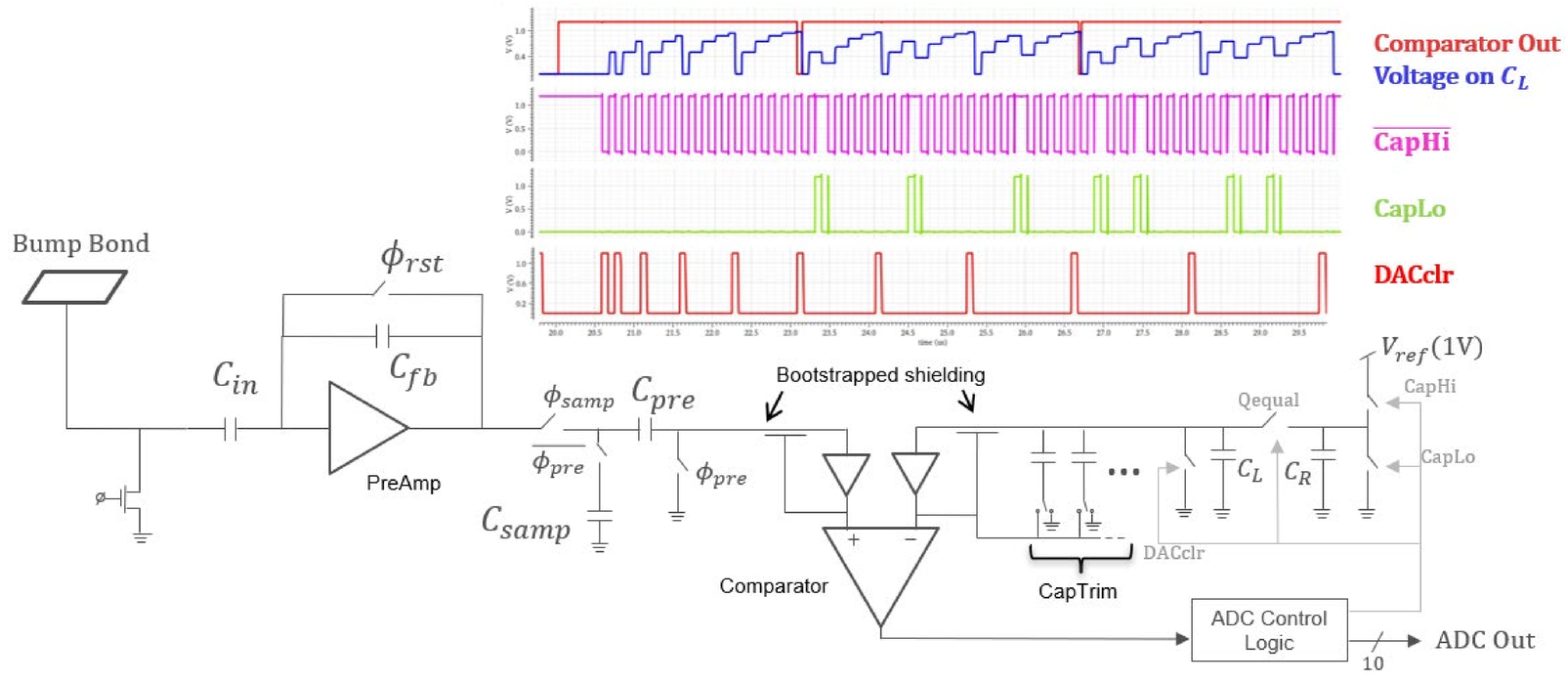


Block diagram of one SPROCKET chip quadrant consisting of 1024 pixels.

Low-Noise Front End

SPROCKET is designed to be compatible with an image sensor which contains an integrated source follower with gain $\approx 115\ \mu V/e^-$. This voltage is amplified by a capacitive-feedback preamplifier with a gain of 1 or 10, yielding a maximum sensitivity of $1.15\ mV/e^-$. The source follower and preamplifier dominate the noise of the system, which is simulated at $\approx 0.5\ e^-_{rms}$ per sample. ($\ll 1e^-_{rms}$ noise is expected from averaging multiple samples due to the Skipper-CCD principle explained above).

After amplification, capacitors C_{samp} and C_{pre} perform correlated doubling-sampling (CDS), which is critical to cancel reset noise from the Skipper CCD-in-CMOS and mitigate the low-frequency noise of the preamplifier.



Simplified schematic of SPROCKET with example control waveforms from one 10-bit ADC acquisition.

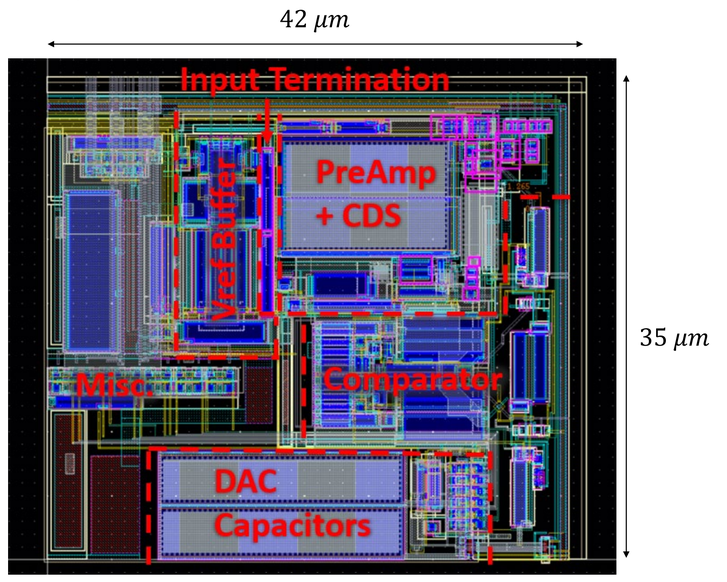
Compact 100 KSPS Serial SAR ADC

The sampled voltage captured by the front end is digitized by a 10-bit SAR ADC (left).

To achieve 10-bit accuracy in a small footprint, only two capacitors are used, C_L and C_R, which are digitally trimmed to match. Precise voltage references are generated from this pair of capacitors by sequentially charging C_R to either ground ($h_n = 0$) or V_{ref} ($h_n = 1$) and then shorting the two capacitors together to redistribute charge. The final voltage after N phases is:

$$\sum_{n=1}^{N} \frac{V_{ref} h_n}{2^{N-n+1}}$$

A comparator generates this final voltage to the sampled input voltage, and the result determines bit *N* of the digital approximation.



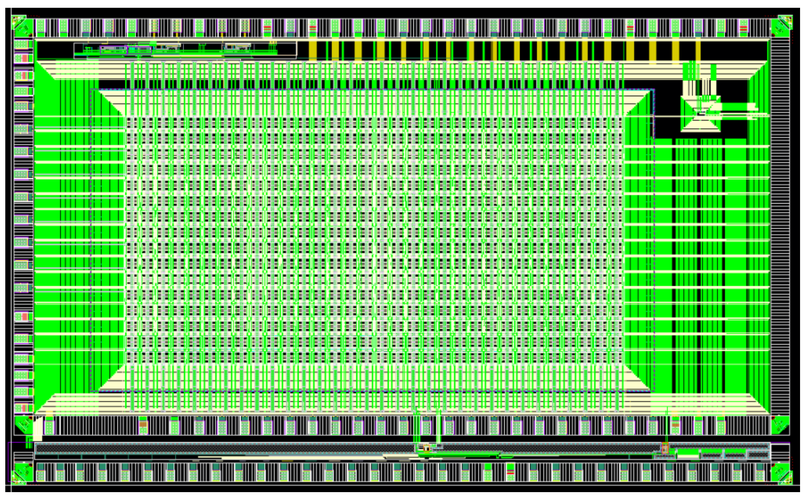
Layout capture of the analog front-end of a single SPROCKET pixel with individual blocks annotated.

Future Work

A 5mm x 3mm test chip (right) was submitted in September 2022. The chip consists of two mini-arrays of 32x32 SPROCKET pixels along with digital readout circuitry. One mini-array uses full readout, while the other uses zero-suppressed readout.

A November 2022 tapeout will prototype more efficient digital algorithms for readout, such as an ML-based autoencoder, and upgrade the front-end to accumulate multiple samples before digitizing, improving readout efficiency.

A final tapeout in 2023 will demonstrate a reticle-scale SPROCKET array with >1,000,000 CCD pixels.



Layout capture of the Fall 2022 SPROCKET test chip.

Further Reading

[1] F. Fahim et al., "A low-power, high-speed readout for pixel detectors based on an arbitration tree," IEEE Trans. VLSI Syst., vol. 28, no. 2, pp. 576–584, 2020. [Online]. Available: https://doi.org/10.1109/TVLSI.2019.2953871

[2] T. Zimmerman, G. Deptuch, and F. Fahim, "Compact, low power, high resolution adc per pixel for large area pixel detectors." U.S. Patent 11,108,981, issued August 31, 2021

In collaboration with Northwestern University

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