DEVELOPMENT OF A BPM SYSTEM USING A COMMERCIAL FPGA CARD AND DIGITIZER ADAPTOR MODULE FOR FETS

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Abstract

A series of Beam Position Monitors (BPMs) will be installed at the Front End Test Stand (FETS) at RAL as part of the 3 MeV Medium Energy Beam Transport (MEBT). The BPMs analyse 2 ms long, 60 mA beam pulses delivered to the MEBT by a 324 MHz Radio Frequency Quadrupole (RFQ). Initial linearity and resolution measurements from the prototype button BPMs are shown. The development of the algorithm for the processing of the BPM signals using a commercial PXI-based FPGA card is discussed and initial measurements of the electronics and signal processing are presented. The test-rig used to characterise each BPM and further develop the processing algorithm is described. The position and phase are measured several times throughout the duration of each pulse, and the measurements are made available via an EPICS server.

FETS MEBT BEAM-LINE

Eight BPMs are being installed in the MEBT to measure the beam's position and phase (see Fig. 1). A combination of two CERN-designed strip-line BPMs and six RAL-designed button BPMs will allow a direct comparison of both technologies. Other MEBT beam-line diagnostic instruments include current transformer toroids and a laserwire emittance scanner [1, 2].

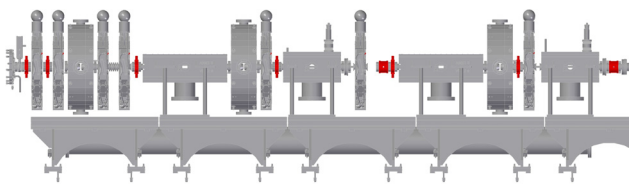

Figure 1: Location of BPMs within MEBT.

RAL BPM DESIGN

A button BPM, shown in Fig. 2, was designed in-house to fit between the quadrupoles in the compact MEBT lattice. Including KF40 flanges either side, the BPM is 44 mm long, with four button electrodes of 16.5 mm diameter spaced at 90° intervals on a bore of 40 mm. Positional and rotational alignment to the beam axis is ensured with a setting piece, keyed notches and external reference pins. To avoid radioactivation from 3 MeV beam-loss, beam facing parts are aluminium. Using matched SMA vacuum feedthroughs and a high button capacitance, Fig. 3. shows that the raw, unprocessed pickup signals give a good representation of the beam's longitudinal pulse shape. Tests on the wire rig (described later) show a position resolution of 100 µm is achievable.

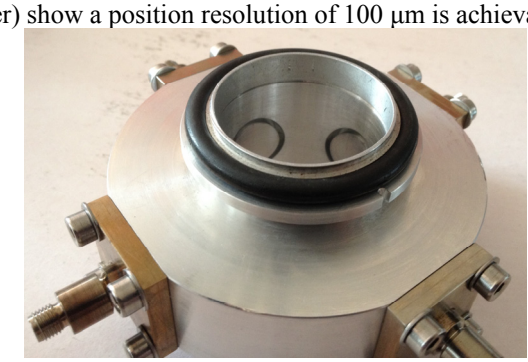

Figure 2: Button BPM with centering ring.

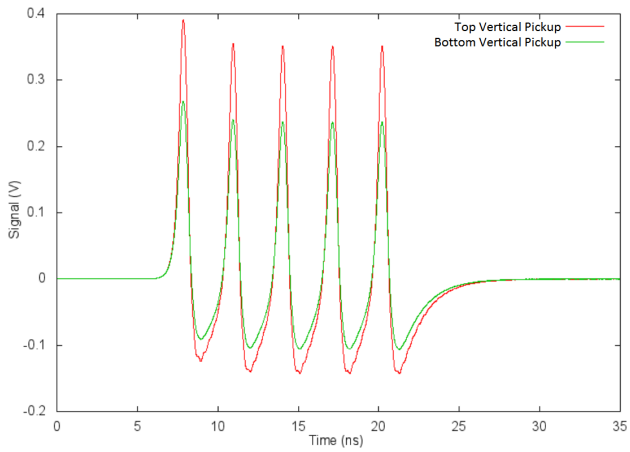

Figure 3: Simulated pickup signal for a 60 mA 3 MeV beam with five 324 MHz microbunches. A 1 mm offset gives 100 mV signal difference between pickups.

BPM POSITION CALCULATION

The position of the beam in each BPM is calculated in a FPGA with the position values being available every 26 µs, around 80 times during a 2 ms pulse.

Down Conversion and Acquisition

The output from each BPM electrode, of which there are 32 in total, is mixed with a local oscillator (LO) of frequency 313.875 MHz. Low-pass filtering results in an intermediate frequency (IF) of 10.125 MHz. The IF signals are sampled at a rate of 40.500 MS/s, exactly four times the IF. The accelerating RF of 324 MHz, the LO of 313.875 MHz and the sample clock are linked using a 10 MHz reference. The fractions LO/RF and RF/clock are simple integer ratios, of 31/32 and 8 respectively, enabling signal generators to be synchronised and phase

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locked using the standard 10 MHz reference common to many items of laboratory test equipment (see Fig. 4).

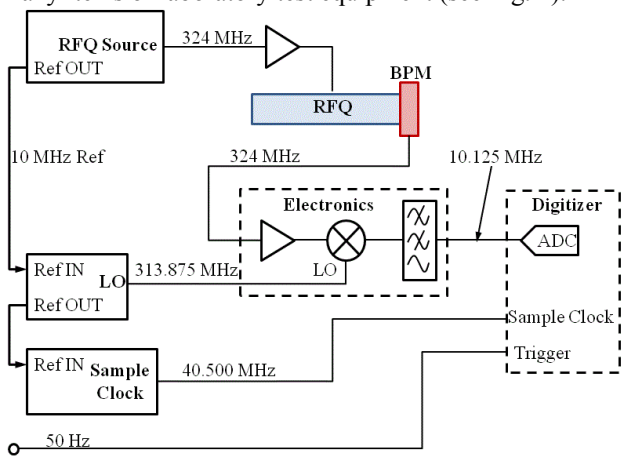

Figure 4: BPM clock reference (one electrode processing channel shown).

FPGA Card

The electrode IF signals are sampled simultaneously in a National Instruments (NI) NI-5752 12-bit digitizer module which is plugged into a NI PXI-7954R FlexRIO card. The PXI-7954R contains a Xilinx Virtex-5 LX110 FPGA is plugged into a PXI chassis containing a NI PXI-8105 Controller card running LabVIEW Real Time. The FPGA has an internal clock of 40 MHz. The calculated positions from the FPGA are streamed to the controller via the PXI backplane using one DMA channel.

Position Algorithm

The FPGA code is written using LabVIEW and makes extensive use of functions from the high-throughput maths palette [3]. Each stage of processing is buffered from the next using a FIFO which can be read from and written to in one FPGA clock cycle. The amplitude of each electrode signal is determined using I/Q sampling over a period of several cycles of the signal. Since the signal is sampled at four times its frequency, successive sample values can be put into one of four accumulators: I, Q, -I, and –Q. After 2^{10} samples, or 256 samples into each accumulator, the output of the accumulator is averaged by shifting right by eight bits to produce <I>, <Q>, <-I> and <-Q>. This is described in Fig. 5.

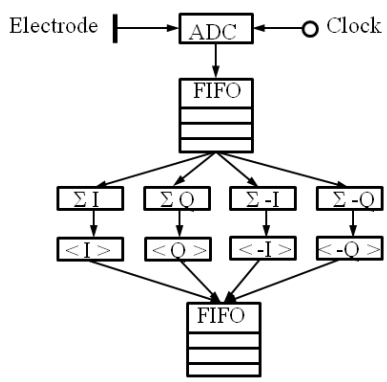

Figure 5: Acquiring and averaging I, Q, -I and –Q.

Each <I>, <Q>, <-I> and <-Q> value is then squared, added and then square-rooted to obtain the amplitude of the signal. The difference and sum of the amplitudes of opposing electrodes of each BPM are then calculated, and the position determined by dividing the difference by the sum and multiplying by a previously determined scaling factor. The relative phase of the each electrode signal is also calculated to enable the time-of-flight to be calculated.

FPGA Code Performance

The code to perform the addition and multiplication operations takes one FPGA clock cycle. The number of cycles required to execute the square root or division function is dependent upon the length, in bits, of the numbers that are being operated on. The division of two numbers or the square root of a number of length *N* takes *N+1* clock cycles. Once the signal has been digitized all numbers are represented using fixed-point type, with the length and increment determined by the maximum value possible at that point in the code. This minimises the length of the numbers used in length-dependent functions.

The multiply, square root, arctan and division functions required use all the DSP resources within the FPGA. As such calculations can only be performed on four electrodes at one time. The data from each of the eight BPMs' electrodes is processed in parallel up until the I, Q, -I and –Q have been averaged. The data is then serialised so that each BPM's amplitude and phase calculation is performed sequentially.

The FPGA code to calculate the beam position has been simulated to ensure correct functionality. The total processing time for one BPM is 52 clock cycles or 1.3 µs, or 10.4 µs for eight BPMs. The code can be optimised using pipelining techniques to allow an increase in performance for calculating the subsequent BPM positions [4]. It is estimated the total processing time for eight BPMs can be reduced to around 2.7 µs. Processing time can also be reduced by using shorter periods of sampling of the electrode signals, which is currently being investigated.

{The LabVIEW FPGA code has been tested both in simulations and compiled and downloaded to the FPGA card and works as expected - rewrite}.

BPM WIRE-RIG

A schematic of the BPM wire-rig is illustrated in Fig. 6. The BPM under test is placed on a KF40 flange mounted on a support frame and attached using a KF40 centering ring and clamp. A copper wire of width 0.35 mm or 0.50 mm is soldered to a BNC socket and mounted on the upper insulator of the frame. The wire is passed through the BPM and the lower insulator then terminated with a 50Ω load.

The frame to which the wire is attached is mounted on a pair of Newport UTS50CC moveable stages mounted at right-angles to each other. A signal source set to the RF accelerator frequency of 324 MHz at a level of 18 dBm (5

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V_{pp}) is attached to the BNC connector. The BPM electrodes are connected to an Agilent 54832D four-channel oscilloscope.

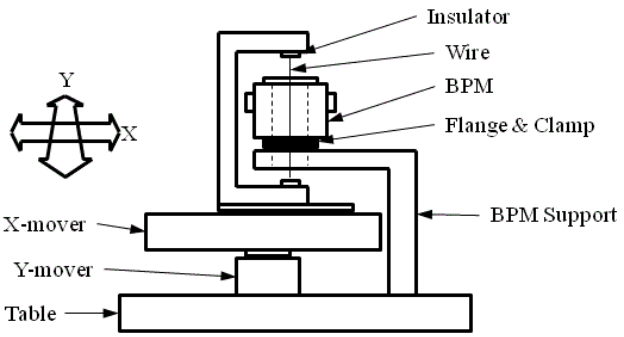

Figure 6: BPM wire-rig.

BPM and Wire Alignment

Before tests and characterisation begin, the wire and BPM are checked for verticality using a dial test indicator attached to a height gauge. Both upper and lower wire insulators are moveable along the frame, and the lower insulator has an off-centre hole and is rotatable to allow accurate alignment of the wire.

BPM Centre Determination

A DC voltage is applied to the wire and the continuity is monitored to determine when the wire touches the BPM bore. The mechanical centre of the BPM can be determined by moving the wire until it just touches a point (X1, Y1) on the bore of the BPM as shown in Fig. 7. The wire is then moved to points (X2, Y1), (X2, Y2) and (X1, Y2). The geometric centre (Xc, Yc) is then determined by the mean of each X and Y pair.

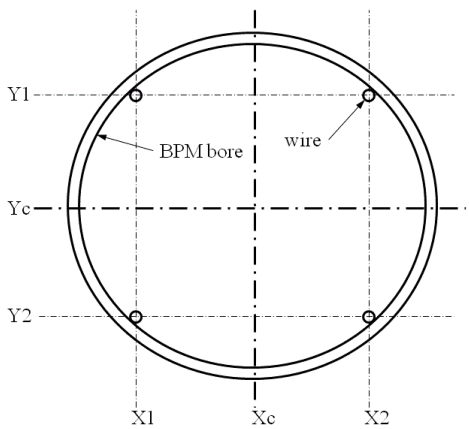

Figure 7: BPM centre determination.

The wire-rig is controlled by a LabVIEW program running on a PC. An array of points is created to which the wire is moved before reading the four oscilloscope waveforms. The amplitude of each electrode signal is calculated from the oscilloscope waveform at each wire position. The absolute wire position and calculated position are compared, with uncorrected results for the prototype button BPM shown in Fig. 8. The linear region is approximately 6 mm radius around the BPM centre.

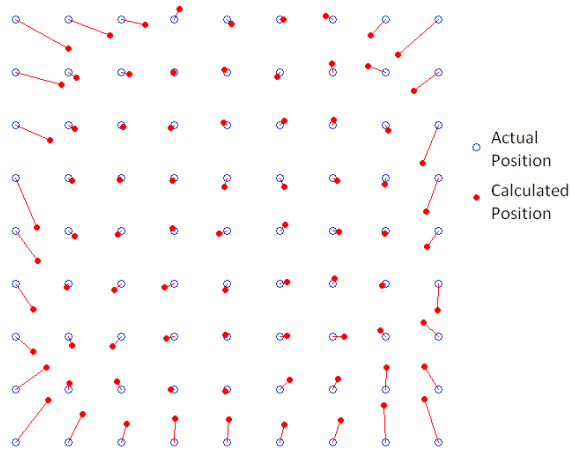

Figure 8: Actual and calculated wire positions for the BPM. Step size of 2 mm shown for clarity.

SYSTEM TEST

The output of a BPM mounted on the wire-rig is connected to the down-conversion electronics where a similar result to that shown in Fig. 6 is expected. The complete system is currently being assembled and tested and results will be available later in the year. The BPMs for installation at FETS are currently being manufactured and each will be tested and characterised on the wire-rig.

CONCLUSION

The wire-rig to characterise the BPMs has performed well on the prototype button BPM and successfully calibrated it to better than the required 100 µm resolution. The FPGA code performed correctly during simulation and gave the expected results when processing signals from a function generator. The complete signal chain from the wire-rig to the output of the FPGA card is currently being evaluated. The processing speed can be increased by using a more powerful FPGA card with almost no re-factoring of the LabVIEW code.

ACKNOWLEDGMENT

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REFERENCES

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