Evaluation of scalable gate architecture components for Si/SiGe spin qubits

Single-shot spin readout, enhanced charge sensing and noise spectroscopy

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1 Introduction

While the first quantum revolution, that resulted in indispensable electrical components such as a transistor or a LED, turned first quantum mechanical effects like the concept of an electron band structure to a noisy degree into a technology, the second quantum revolution is expected to make full use of quantum mechanical effects such as superposition or entanglement. Quantum computing is an example for an engine of this second quantum revolution and got greater attention for the first time, when mentioned about 40 years ago in a talk by Richard Feynman [1]. It took another 20 years until concrete concepts were developed, when for example in the year 2000 D. DiVincenzo, a quantum computation pioneer, formulated 5 criteria for a successful implementation of a quantum mechanical two-level system as a quantum processor [2]. A first simple algorithm of prime-factorizing the number N=15 into the factors 3 and 5 was then demonstrated in a liquid NMR platform in 2001 [3]. While this platform turned out challenging for scaling of the quantum processor, such results paved the way for the further development of quantum algorithms and the search for new qubit platforms.

It soon became evident that in many realistic quantum bit (qubit) implementations, the quantum mechanical two-level system is very fragile and prone to dephasing and relaxation, induced by interaction with the environment. However, a minimum level of qubit coupling is always required for manipulating, coupling and readout of the quantum information. This consideration as an example makes it apparent that the development of quantum computing is not exclusively an engineering task, but ever deeper understanding of the underlying physics has always been required.

Over recent years several physically completely different platforms emerged as serious candidates for the implementation of quantum computing. Such concepts comprise the quantum mechanical two-level implementation using superconductor circuits, a photon's degrees of freedom such as polarization, trapped ions or confined spins in semiconductors. Every platforms comes with specific advantages and drawbacks regarding the criteria for universal quantum computing.
At the time of the beginning of this PhD project, the state of research in quantum computation science across all these platforms was termed noisy intermediate-scale quantum (NISQ) era. The term designates that control of two level systems became as good that a new technology branch started to form and usage of a quantum mechanical two-level system for computation became accessible. In various promising qubit implementations, single qubit gates, the proof-of-principle for quantum computing, had been demonstrated and provided an opportunity to develop first quantum algorithms. Simultaneously with few working qubits in place, implementation and testing of error-correction schemes was pursued and gate fidelities were aspired to improve. But also scaling of the qubit systems to a size as large as necessary emerged as one of the most important tasks.

Right from the emergence of quantum computing, a single spin has been one of the most investigated platforms, as it provides a natural quantum mechanical two-level system and when for example confined within a semiconductor, this technology ansatz seemed to be compatible with the existing microelectronics industry and device fabrication techniques. Also the integration of both, a quantum processor as well as classical electronics on the same chip seemed auspicious. Within a semiconductor, the nuclear spin of a dedicated dopant atom can for example be used as the quantum mechanical two-level system, but also other implementations like an electrostatically confined electron or a hole are conceivable. Although the spin in such an implementation does not couple directly to electric fields, hyperfine interaction with the fluctuating surrounding nuclei of the host material turned out detrimental for the spin coherence time. Therefore, silicon soon started to be most-used material platform as it does provide only a small amount of nuclear spin carrying isotopes.
Especially gate-defined qubit devices based on a silicon/silicon-germanium quantum well heterostructure demonstrated tremendous progress recently. At the start of this PhD project, first two-qubit gates were performed [4]. Furthermore, single-electron spin coherence times of 20 µs and single-qubit gate fidelities of 99.9% [5] were achieved. Notably, by isotopically purifying the silicon host material, the coherence time turned out to be limited by charge noise instead of hyperfine interaction. Moreover, initial efforts of turning the qubit from the fundamental research level into a technology were pursued. Concepts for this intention were first industrially fabricated qubit devices, operation of

qubits at elevated temperatures, automated tuning of qubit devices, gate-based qubit readout [6] or long-range coupling of qubits via spin-photon interaction [7].
While all these efforts are important steps for entering the next era of universal quantum computing, a deeper understanding of the underlying quantum physics and improvement of the experimental control of the qubit system is still required to potentially push forward quantum computing into a widespread technology.
Especial importance can be attributed to the readout of the spin qubit, as the sensor receives a pivotal role in the examination and development of new aspects in the dynamically advancing field of quantum computing with single spins. A high fidelity spin qubit readout will be crucial for successful realization of upcoming tasks like intermediate-scale coupling of spin qubits or the strive to improve coherence and relaxation times to just name a few. Simultaneously, a strategy for the qubit readout has to be developed when the number of coupled qubits on a single chip will scale in the near term. As a third aspect, the sensor receives a leading role as part of a spin qubit device as under the background that the qubit coherence turns out to be limited by charge noise instead of hyperfine interaction, the sensor of a qubit device also provides a straightforward mean to measure the charge noise via spectroscopy of the sensor signal.
In this thesis we therefore focus on the sensor as one of the most important architecture components of a spin qubit device with the aim of developing a deeper physical understanding regarding its functionality and some of the above mentioned aspects. The thesis is organized as follows:

1. **Chapters 2** and **3** provide an overview of the different qubit platforms, before the here-used silicon quantum well heterostructure is introduced and a concept of electron accumulation and confinement in the quantum well is presented. Also, the basics of the qubit operation, such as the sensor dot formation, charge sensing of the qubit occupation or single-shot spin readout via spin-dependent tunneling are discussed. Moreover, technical aspects like the heterostructure growth, the difference between the accumulation- and the depletion-architecture gate design, an overview of the cryostats, the electrical wiring or the characterization of the noise in the empty setup are presented.

2. **Chapter 4** presents magnetospectroscopy measurements of Hall bar devices, with a focus on the stability of the accumulated electrons, gate hysteresis and the experimental control of the accumulation turn on voltage. The chapter also discusses an established model of interface trap states that limit the charge stability.

3. **Chapter 5** introduces a new operation principle and a new gate design for a sensor dot, capable of increasing the sensor output response for a single-shot spin qubit readout via spin-to-charge-conversion by an order of magnitude. The concept is

based on an asymmetric design of the capacitances between sensor dot and Ohmic contacts. The increased sensor signal significantly reduces the demands on the first ensuing amplification stage which may either be located on the same processor chip or at least at cryostat temperature in close proximity to the device.

4. **Chapter 6** addresses challenges for the tuning and the spin readout fidelity of an accumulation-type spin qubit device that uses a sensor quantum dot or a 1D-like channel with a partially discrete electron density of states (DOS) for an electron reservoir. We especially aim to compare the single-shot fidelity of the spin readout via spin-dependent tunneling to results measured earlier on a depletion-architecture spin qubit device that featured a 2D-electron gas with a continuous DOS as reservoir.

5. **Chapter 7** presents a study of charge noise power spectral densities in dependence of the accumulation voltage, measured in our accumulation-type sensor dot, against the background of charge noise limiting the qubit dephasing in current isotopically purified devices. We also use the noise analysis as a tool to characterize a new dilution cryostat setup that was installed with all related measurement equipment as part of this PhD project.

6. **Appendix:** Completes the preceding chapters 4-7 and provides additional information regarding the presented measurements.

2
Concepts

Currently, the efforts of implementing quantum computation have entered the noisy intermediate-scale quantum (NISQ) era. For the realization of the ensuing era of universal quantum computing however, millions of at least partially entangled qubits may be required. Currently, many different physical platforms for the implementation of quantum mechanical two-level systems exist. Of these approaches, each comes with certain advantages and drawbacks regarding the challenges of scalability, gate fidelity or the required technical overhead to just name a few.

2.1 Experimental platforms for quantum computers

This section provides an overview of 5 promising quantum computing platforms, which will all briefly be introduced. We focus on the most advanced and the chronologically first qubit systems here. This section does not have the intention of all-embracingly covering the whole research field, which is still vastly growing and there are many different approaches. Some concepts like NMR, CV centers or graphene based systems will not be discussed throughout the following section. The following section is inspired by the review article [8], but features many concepts that have developed over the past 14 years since the review article was published. Also ideas of the reviews [9, 10] are picked up.

Superconductors

The maybe most well-known approach, also outside the universitary research community, is encoding a quantum bit in a superconducting electrical circuit. This implementation of a qubit processor also demonstrates currently the largest number of qubits and is very present as not only universities and other research organizations but big IT service providers launched own quantum computing programs following this strategy. Starting in 2017 IBM made the usage of quantum computing accessible for everyone to use, first limited to simple algorithms on their 7-qubit quantum processors [11], but recently increased the processor to 127 qubits [12, 13]. Also Google demonstrated first quantum supremacy in 2019 [14, 15] on a chip featuring 53 working qubits and subsequently demonstrated error correction on 49 qubits in 2023 [16, 17].
The recent progress of superconducting qubits is well described in the two reviews [18, 19], on which this short summary here is based.
The simplest description of such a superconducting LC circuit seems obvious: The two levels required for the computation may be defined when the excitation energy is either stored within the capacitor or in the inductance and the potential is described by the quantum harmonic oscillator [8, 19]. To address individual states of the system however, some anharmonicity is required in order to distinguish the resulting harmonic states. This anharmonicity typically is introduced via the integration of a Josephson junction into the circuit [8, 19]. In combination with the Josephson junction different flavors of the superconducting loop have been demonstrated, each flavor engineering the potential in a different way. The most common approach, which is also pursued by Google and IBM, are transmon superconducting qubits [20]. Other implementations are termed flux or phase qubits [18].
The single and two qubit gate durations are as fast as a few tens of nanoseconds [17] and demonstrate high gate fidelity, exceeding 99% [21]. The coherence times of such qubits are significantly longer than the gate operation times. A pure dephasing constant $T_2 = 127\ \mu s$ [13] has been reported as well as a relaxation time of $T_1 = 288\ \mu s$ [13].

Photons

Photons have also been demonstrated to serve as a possible qubit candidate and will be introduced in the following. The explanation of photon based quantum computing here was mainly adapted from [22], [23] and the notes in [24].
There are different physical degrees of freedom to encode the qubit. Using the polarization of a photon as quantum mechanical two-level system allows for very simple single-qubit gate implementations using a birefringent waveplate [22]. Information encoding in the photon trajectory following the transition through a beamsplitter or exploiting the orbital

angular momentum are also possible implementations [25].
The availability of two-qubit interactions became possible by the Knill-Laflamme-Milburn (KLM-) scheme [26]. The authors marked also the field of a conceptually totally different approach towards quantum computation: The emergence of so-called "measurement-based" quantum computation.
Applied to photonic quantum computing this measurement-based concept enables two-qubit gates using only linear optical elements, like beam splitters and phase shifters, as well as single photon sources and detectors [26]. The approach by Knill et al. relies on the Gottesman-Chuang quantum teleportation concept and entangling with ancilla photons. A good explanation can be found for example in [22] and in [23]. Using the KLM-scheme, two-qubit gate fidelities as large as 99.69% and single-qubit gates of 99.84% were demonstrated recently in [27]. Incorporating the KLM-scheme, also 18 qubits using 3 degrees of freedom from 6 entangled photons were presented in [25].
Around the same time the KLM scheme emerged, also a second measurement-based concept was introduced, which is called the "one-way" measurement-based quantum computing ansatz [28]. This concept relies on a grid of with-each-other entangled photons as resource state, often called graph or in some special cases cluster state. The concept is well described in [29] and in [23] and was first experimentally demonstrated in [30].

Trapped Ions

The maybe lowest error rate when performing qubit gates is demonstrated on a third quantum computing platform employing trapped ions [31, 32]. Ions can be trapped and cooled in so-called Pauli traps using laser cooling and are typically arranged in a linear array. The ground state and an intrinsically stable exited state of the ions serve as two-level systems. Coupling of neighboring ions and lifting the degeneracy in resonance frequency is achieved by inducing a laser-controlled common and quantized motion of the string of ions [33]. Quantum algorithms have been demonstrated with up to 50 coupled qubits. Very long coherence times up to minutes [33] and large gate fidelities, exceeding 99.9% for two qubit gates and 99.99% for single qubit gates are reported at gate durations faster than 100 µs [33–35].
However, scaling seems technically demanding, as the technical overhead required for scaling to millions of qubits remains challenging at the moment. A good review for the current state of quantum computing using trapped ions can be found in [36]. Ideas for this short summary are adapted from [8] and the reviews [33, 35].

Topological quantum computer

Even higher fidelity and lower decoherence is predicted for topologically protected qubits. With Microsoft, also a big IT service provider pursues this ansatz [37].
In the original proposal, Kitaev suggested the usage of anyons for quantum computing [38]. To understand the concept of anyons, we look at the common wave function of two indistinguishable particles. Exchanging indistinguishable particles results in either the same wave function (1, boson) or in a wave function with negative sign (-1, fermion), because exchanging twice has to restore the original wave function: $(-1)^2 = (1)^2 = 1$. Non-abelian quasiparticles like anyons behave differently. Their wave function contains a history upon two-fold exchange as not the identical wave function is restored, but a certain phase factor is picked up. This is why often the term braiding is used in this context [39]. Possible candidates for the realization of these quasiparticles are predicted to emerge in the 2-dimensional fractional quantum Hall effect [40, 41] but also for the majorana zero mode at the nanowire-semiconductor to superconductor interface [42].
First experimental hints for the existence were reported in 2012 [43]. But the research field suffered a big drawback when multiple promising articles for the experimental proof of majorana fermions from the year of 2017/2018 [44, 45] had to be retracted 4 years later [46, 47]. Up to date, no experimental proof of non-abelian quasiparticles has been reported.
A short introduction to topological quantum computing, can be found in the reviews [48, 49], which served as a basis for this short overview.

Spin in semiconductor

As the last platform here, we introduce quantum computing using a spin confined in a semiconductor host material. This is the approach we pursue in our research group and also within this thesis at hand.
Using spins for quantum computation was postulated by Loss and di Vincenzo in the pioneering paper [50] as well as by Kane in [51]. Both articles envisioned technically different access and confinement of the electron spin.
Advantages of this platform are on the one hand the compatability with existing microelectronic industry, both in fabrication as well as considering the integration with current classical computer hardware. Both aspects are promising for an eventual scaling to millions of qubits. On the other hand, the spin is a priori insensitive to electric fields, providing protection of the qubit information, while the charge of an electron or hole can be controlled by electric fields for example for qubit initialization and readout [10]. With Intel, again a big microelectronics company supports this ansatz, and high device yield and state-of-the-art relaxation and dephasing constants have been published on

industrially fabricated devices [52].

For the spin confinement in the semiconductor host, there are different realization [53–55]: A single electron or hole can be confined electrostatically inside a semiconductor quantum dot as envisioned by Loss and DiVincenzo. Also the confinement of multiple adjacent spins is possible and the overlapping shared wave function may be used for the qubit encoding in the resulting singlet triplet basis. Depending on the number of sites and spins even more complex realizations are conceivable [10].
A second parallel ansatz is to incorporate a single donor atom like phosphor inside a silicon semiconductor as proposed by Kane. Both the phosphorus nuclear spin 1/2 as well as the excess electron can be used for encoding the qubit information.
Depending on the type of qubit encoding, the approaches for initialization, manipulation, readout and interaction with other qubits differ [9] and some basic properties and recent advances are displayed in the next section. Currently, devices featuring up to 6 qubits were demonstrated. Also, single and two qubit gates with fidelities exceeding the error correction threshold as well as T_2^* times of microseconds and seconds long T_1 times have been reported recently [10]. As this platform will be employed in the remainder of this thesis, the next section will present more details regarding latest efforts in this research field.

2.1.1 State-of-the-art of spin qubits in semiconductors

Single electron spin qubit in gate-defined quantum dots

A big advantage of using a single confined electron spin inside a quantum dot for quantum computing is the promising scalability prospect. Soon, first working qubit devices in doped GaAs quantum well heterostructures were reported. In this material system, the effective electron mass is comparatively low $m^* \simeq 0.07 \cdot m_e$. Hence the fabrication of metallic feature sizes of 100 nm sufficed to electrostatically define potential minima in the quantum well. By metallic gates and applied gate voltages the electron number stored in these quantum dots as well as tunnel barriers to electron reservoirs or between neighboring quantum dots could be controlled. Using the singlet-triplet basis of two entangled neighboring electron spins as a two-level system, first electrically controlled Rabi oscillations were demonstrated [56], which however were limited by short dephasing times of only $T_2^* \leq 10$ ns. Hyperfine interaction with GaAs host nuclei caused the fast dephasing of the quantum state. Recently, the dephasing time in this material system has been improved by pulsing techniques but remains still comparatively short with reported dephasing times of $T_2^* \leq 100$ ns [57].
Soon, the focus turned to silicon which naturally features only 5% ^{29}Si isotopes. The

remaining ^{28}Si and ^{30}Si isotopes do not posses a total nuclear spin and hence do not cause dephasing of the electron spin via hyperfine interaction. Also further isotopical purification as low as only 60 parts per million (ppm) remaining ^{29}Si is technically possible for the silicon base material [58, 59]. Two approaches using silicon as host material emerged. In the first ansatz, the electron spin is confined in a silicon/silicon-germanium quantum well heterostructure, in the second ansatz, a quantum dot is formed at the silicon to oxide interface (CMOS) interface.
For both approaches, the qubit readout is performed by linking the spin information and the electron charge and spin-dependent tunneling constitutes the readout process. The linking can be implemented either by alignment of the Zeeman split spin states to the Fermi energy of an electron reservoir or using Pauli spin blockade in a double-dot system. Charge tunneling or the absence thereof is either detected via a sensor quantum dot, RF reflectrometry or gate dispersive readout. Spin manipulation of the qubit in turn can be implemented by applying a resonant microwave signal via a nano-stripline (Electron spin resonance, ESR) or artificial spin-orbit coupling in a magnetic field gradient (Electric dipole spin resonance, EDSR).
Long coherence times of $T_2^* = 120$ µs [60] have been reported. Both single [5, 60–62] and two-qubit gates [4, 63, 64] with fidelity beyond the threshold for fault tolerant operation [65–67] have been reported recently.
For scaling, which may be a promising advantage of this material platform, some concepts like the spider-web array [68] have been proposed, but the available cooling power as well as the electronics close to the qubit device remain under discussion.

Hole spin qubit

Tremendous progress has been achieved in recent years by using the spin of holes. A big advantage holes in Ge/SiGe or CMOS structures have compared to electrons is their p-type wave function character, resulting in no overlap with the host nuclei, eliminating the contact hyperfine interaction. The large intrinsic spin-orbit coupling in germanium makes hole qubits susceptible to electric noise but also makes the use of magnetic field gradients redundant and allows for very fast gate operations. Single hole confinement in CMOS structures is possible with coherence times of $T_2^* = 1$ µs, lower than for electron spins [69]. In that material system single qubit gates with fidelities >99.9% were demonstrated. Also two-qubit gates on a device with up to 4 qubits have been demonstrated recently [70] [71] [64].

Donor spin qubit

As a last semiconductor platform for potential quantum computation using spins we want to introduce single dopant atoms in a semiconductor environment. The fundamental proposal by Kane in 1998 [51] used the nuclear spin of a single dopant atom and qubit coupling was proposed via the excess electron and hyperfine interaction with the nucleus. Here, we mainly focus on phosphorus in silicon, following the two reviews [9, 10].
Nowadays, both the electron and the nuclear spin are used individually as quantum mechanical two-level systems. Decoherence times of 270 µs for the electron spin [72] and T_2^* of 840 µs for the neutral and 3.3 ms for the ionized dopant nucleus [73] at single-qubit gate fidelities exceeding 99.9% [72] have been reported. Just like the quantum dot spin qubits, the readout of such qubits is performed via spin-to-charge conversion using a sensor dot in the vicinity of the qubit dot [9]. A challenge for this platform is scaling and the implementation of two-dopant interaction as the donor placement so far typically is performed by implantation or STM placement [10]. Last year two-qubit gates using two donor dopant atoms with fidelities exceeding 99% were demonstrated [74].

2.2 Gate-defined quantum dots in a silicon quantum well heterostructure

In this section we introduce all concepts leading to the confinement of a single spin inside the quantum well of a semiconductor heterostructure. We highlight some of the advantageous properties by using silicon compared to different semiconductor materials, and outline briefly the basics of characterizing a 2-dimensional electron gas (2DEG) in the quantum well by magnetotransport measurements. Subsequently, we discuss the physical properties leading to the formation of quantum dots in the quantum well and analyze the resulting consequences for the energy levels of a confined spin. A more detailed introduction, also comprising other spin-qubit related fundamentals like the spin manipulation, is given in my Master's thesis [75].

2.2.1 Formation of a 2DEG in a quantum well by heterostructure engineering and electrostatic band bending

Using silicon as a host material for gate-defined quantum dots provides many advantages compared to other semiconductor materials. Foremost, existing microelectronics technologies are promising for industrial large scale of quantum processors. Also, the

integration with classical technologies on the same chip seems possible this way. In contrast to for example GaAs, only 4.7% of the naturally occurring silicon isotopes carry a nuclear spin. These ^{29}Si isotopes can further be isotopically purified, leading to substrate materials with a remaining ^{29}Si concentration as low as 60 ppm, limiting the hyperfine interaction with the host material to only $O(10)$ non-zero nuclear spins [59]. Moreover, the low spin-orbit coupling in silicon also turns out beneficial for long coherence times. For our qubit devices we will confine a single electron spin inside the quantum well of a Si/SiGe heterostructure, which will be introduced in the following.
With lattice constant of a_{Si} = 5.331 Å and a_{Ge} = 5.657 Å [76], silicon and germanium are arbitrarily mixable in an alloy [77]. Figure 2.1a shows the band structure of silicon and Figure 2.1b the band structure of germanium [79]. The band gap of silicon is 1.11 eV. The band structure has a valence band maximum at the Γ point and a six-fold degenerate conduction band minimum along the [100] direction between the Γ and X point, as shown in Figure 2.1c. For germanium, the band gap is significantly smaller with only 0.66 eV. The valence band maximum is also at the Γ-point, the conduction band minimum at L-point.

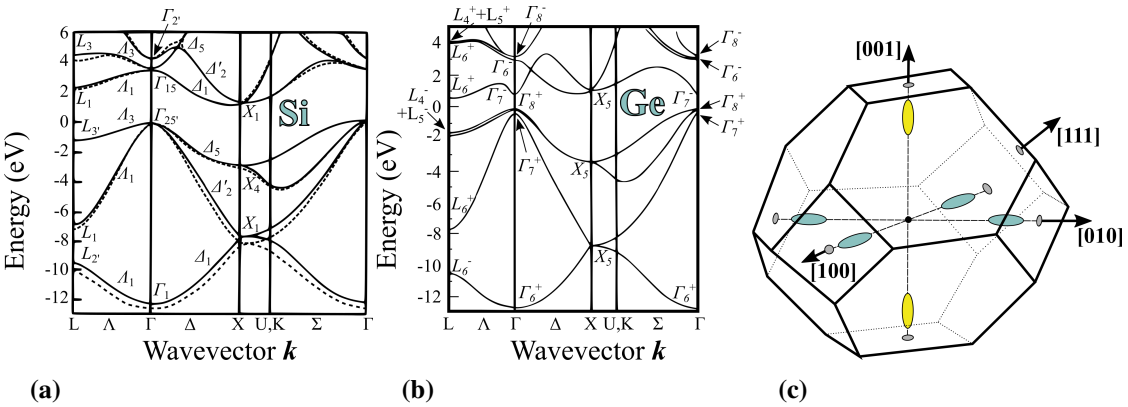


Figure 2.1: Silicon and germanium as spin qubit host materials. (a),(b) Band structures of silicon and germanium. Diagrams taken from [78]. **(c)** Illustration of the conduction band minima in a Si and Si/Ge alloy with silicon concentration ≥ 15% along the Γ to X-point ([100]-direction). Figure adapted from [79].

We utilize the miscibility of both elements to engineer a heterostructure, that features an around 10 nm thin layer of silicon between two Si_xGe_{1-x} barriers. In our samples, the heterostructure is grown on a silicon substrate and the structure is capped by 1 nm of silicon, to prevent oxidation of the SiGe barrier. A typical cross section as well as the energy of the conduction band minimum along the growth direction is shown in the upper

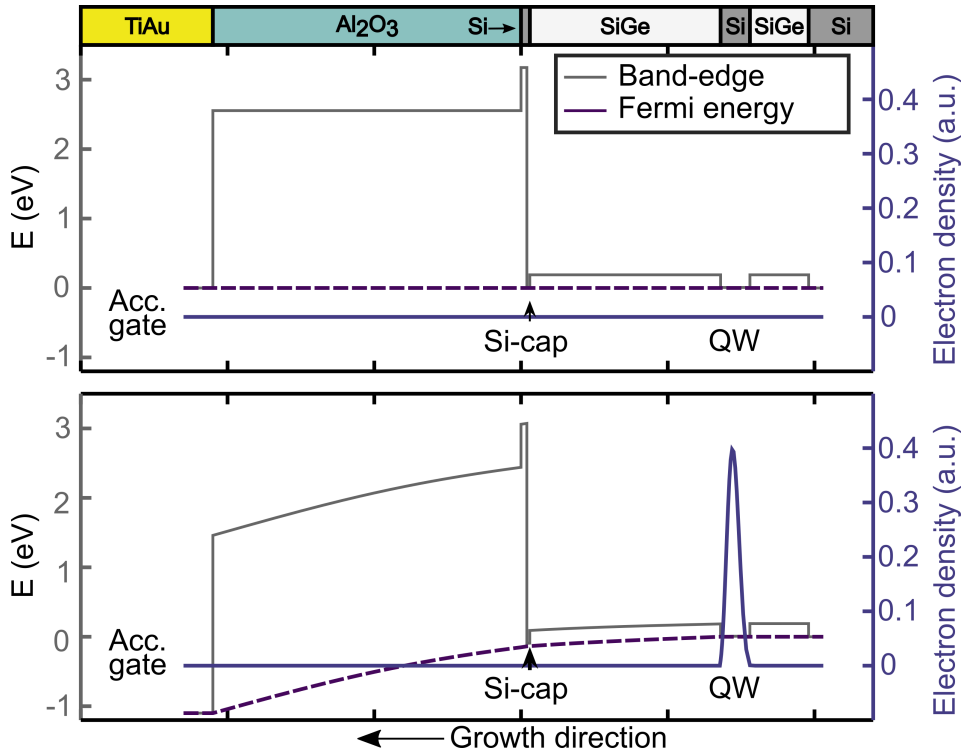


Figure 2.2: SiGe heterostructure. Simulation from Floyd Schauer [80]. The simulation shows the potential energy of the conduction band-edge minimum as grey curve, the Fermi energy of the system as dashed purple line and the electron density as blue curve. The heterostructure stack also includes a thick oxide and metal gate layer. The upper panel of the simulation shows the energies without application of a voltage to the TiAu accumulation gate. The lower panel illustrates the configuration for a positive voltage applied to the gate. By applying the gate voltage, the conduction band edge is bent energetically below the Fermi energy resulting in a finite electron density inside the quantum well.

panel of the simulation in Figure 2.2, which was performed by Floyd Schauer [81]. Note, that for the quantum well, the conduction band forms a potential minimum in energy, although silicon intrinsically has a larger band gap. However, as the quantum well is only a thin silicon layer of a few atoms in height, its lattice constant adapts to that of the SiGe barrier, lowering the silicon band gap by the induced strain and resulting in a staggered type II band alignment [77]. Also note, that due to the strain, the sixfold degeneracy of the conduction band minimum is lifted, resulting in an energetic reduction of the 2 valleys along the growth direction [82], which was already indicated by the false

color in Figure 2.1c.
The simulation shows, that the conduction band intrinsically is not populated by electrons, as the Fermi energy lies inside the band gap. To accumulate electrons there are mainly two approaches: On the one hand, a doping layer can be integrated into the heterostructure gate stack of which donor atoms provide electrons to the quantum well. This approach has worked well but has the drawback that ionized donor atoms remain, which lead to scattering of electrons during transport through the quantum well or equivalently can enhance qubit device instability. On the other hand, electrons can be accumulated electrostatically inside the quantum well by a positive electric field provided by a gate electrode. The process is well described in [83] and also in my Master's thesis [75]. Here, only a brief discussion on the consequences of applying a positive electric field to the heterostructure will be given.
We add a metallic gate, isolated by an oxide layer, on top of the heterostructure in Figure 2.2. By applying a positive voltage to this gate, the Fermi energy and the conduction band minimum are bent and lowered electrostatically, as shown in the lower panel of the simulation in Figure 2.2. The band bending results in the band edge being pulled below the Fermi energy inside the silicon quantum well. Consequently, an electron charge density forms in the quantum well. Both simulations in the figure were performed by Floyd Schauer [81]. The situation can be compared in a simplified model to a plate capacitor with the metallic gate on top of the heterostructure stack and the quantum well of the structure being the two corresponding plates.

2.2.2 Heterostructure analysis by magnetotransport

By band bending electrons can be accumulated in the quantum well and the density of this 2DEG is controlled by the applied gate voltage. By performing transport measurements in a magnetic field and a four-point measurement geometry, we are able to deduce the electron density as well as the mobility of the charge carriers. The following derivations are well described and adapted from the textbooks [83] and [77].
In a low magnetic fields (typically < 1 T) transport is described by the Drude model: The model provides a relation of conductivity, charge carrier density and mobility. By application of a magnetic field, the conductivity tensor obtains a non-zero component perpendicular to the applied current and magnetic field (Hall effect). The relations for the resistivity tensor, the inverted conductivity, are

$$\rho_{xx} = \frac{m^*}{n \cdot e^2 \cdot \mu} \tag{2.1}$$

$$\rho_{xy} = \frac{B}{n \cdot e} \tag{2.2}$$

in which the mobility is defined as $\mu = \frac{e\tau}{m^*}$, e is the elementary charge, here neglecting the sign for simplicity, m^* the effective mass and n the charge carrier density. By measuring both resistivities in a 4-point geometry we can experimentally access both 2DEG characterizing quantities n and μ.

From the spatial confinement along the growth direction (z), the electron dispersion is quantized and forms a series of sub-bands with free in-plane motion (x,y). Increasing the magnetic field, Landau level quantization steps in: By increasing the perpendicular magnetic field along z, the states will condense in Landau levels with energy $\hbar\omega_c(n + \frac{1}{2})$, independent of the in-plane momentum k_x, k_y.
We also introduce the filling factor

$$\nu = \frac{h}{e} \cdot \frac{n_{2DEG}}{B} \tag{2.3}$$

counting how many Landau levels are occupied. With increasing magnetic field, the density of states per Landau level increases and hence the filling factor decreases. In this regime, the quantum Hall effect describes the course of the resistivity in a transport measurement and plateaus with $\sigma_{xx} = 0$ and consequently $\rho_{xx} = 0$ form for the longitudinal resistance, while the transversal resistance $\rho_{xy} = \frac{1}{p}\frac{h}{e^2}$ is quantized by integer p, whenever a Landau level is completely filled. We will measure such quantum Hall effect features in this thesis and also calculate the filling factor ν.

While for transport through the 2DEG in the silicon quantum well in the Hall bar a single metallic gate sufficed for accumulating a global electron density, we now aim for isolating single electrons in quantum dots to form our spin qubit. This requires local electron density control and new concepts for a 0-dimensional electron system apply. In the next section we introduce the basic physical principles resulting from such a 0-D confinement of an electron and introduce important concepts for operating a qubit device.

2.3 Single-electron physics in Si/SiGe

We now try to modulate the continuous charge carrier density inside the quantum well with the aim of forming a potential minimum for locally trapping electrons. This potential minimum we call quantum dot. In the following description, we do not go into technical or fabricational details about this confinement, but rather highlight the consequences and

how isolated electron spins can be used in a qubit device. All tuning in the following is performed electrostatically by gate voltages. This allows us to form electron reservoirs and tunnel barriers for loading and unloading the quantum dot. More details are provided in section 3.1.3. Here, we focus on the resulting physics when confining electrons in a quantum dot.

2.3.1 Coulomb blockade: Single energy states according to electron occupation

Figure 2.3a shows a very simplified approach towards this goal by introducing a global topgate (TG) and two additional, smaller gates underneath. These two gates screen the positive electric field of the global TG and create a potential minimum in between. In the quantum well underneath accordingly an electron island forms. To the left of the island an electron reservoir is formed where the global accumulation gate is not screened. The island, which we call quantum dot, is tunnel coupled to the reservoir and electron exchange can take place, as indicated by the red arrow. The tunnel barrier is sketched by the equivalent RC connection, which size and tunnel rate may be controlled by the above lying local gate. Therefore we call this gate a barrier-forming gate or just barrier gate, in contrast to the TG.

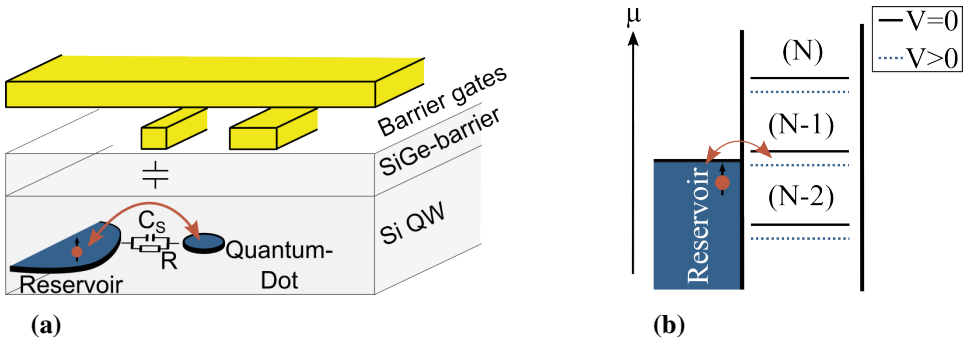


Figure 2.3: Electrostatic formation of a quantum dot. **(a)** Sketch of the heterostructure and a simplified two-layer metal gate stack. **(b)** Discrete energy levels of the quantum dot depending on the amount of quantized electron charges stored on the quantum dot.

The resulting energy can be described in a simplified form with a semi-classical ansatz, in which the electrostatic energy of the electron island depends on both, the number of electrons stored on the island as well as the resulting gate voltages, in our sketch mainly the gate voltage of the above lying global TG. As the electron charge is of course

quantized, single energy levels depending on the number of electrons form, as illustrated in Figure 2.3b. The figure shows the chemical potential μ, which increases by a discrete amount the more electrons are stored on the island. The potential can be capacitively controlled by the applied gate voltage V, lowering the potential when increasing the voltage. The charge on the island is in the so-called "Coulomb blockade", so it remains constant, unless the chemical potential of the next state is lower than the Fermi energy set by the electron reservoir. This concept allows also the storage of only a single electron charge on the island by corresponding gate voltage tuning.

Transport through a quantum dot

Transport through a single quantum dot is illustrated in Figure 2.4a, which resembles the device of Figure 2.3a, but this sketch shows two reservoirs which are tunnel coupled to a quantum dot in between. We term the reservoirs source and drain and apply a bias voltage to the drain reservoir, shown in the sketches in 2.4b and 2.4c. Due to the Coulomb blockade of the quantum dot, transport via sequential tunneling only sets in, when an energy level is energetically tuned right into the bias window. If no energy level is available, current is blocked. This configuration of a quantum dot coupled to two reservoirs is termed single electron transistor (SET).
A characteristic measurement for this SET is the so-called "Coulomb diamond" measurement, sketched in Figure 2.4d. The figure shows a simplified measurement of the current through this SET, varying the gate voltage (here $V_{plunger}$) and the bias voltage V_{bias}. Only for non-zero bias voltage, the bias window between source and drain opens up and current is allowed, but also only when an energy level is available. The regions in which current is allowed are the yellow triangular shapes, the blockade configurations the blue diamonds. The larger the bias window becomes, the wider the regions, in which current is conducted, grow. Eventually, the bias window becomes as large as the separation of two consecutive energy levels, so no Coulomb blockade occurs any more. A cut through the measurement for a fixed bias voltage is shown in the inset in the bottom right corner, in which peaks in the transported current emerge. Note, that for each peak an additional electron is loaded onto the island.
Figure 2.4e also shows a current measurement of the SET for a constant bias voltage. In this measurement, two gate voltages are varied. Instead of peaks like in the inset before, this measurement shows diagonal lines whenever current through the SET is conducted. Each line corresponds to an energy level inside the bias window and accordingly the SET remains in constant occupation in between two lines, here indicated by the white numbers in brackets. The Coulomb peaks form diagonal lines because of gate cross-coupling of the two varied gates: Increasing one gate for example $V_{Plunger}$, the second gate V_2 has to be decreased to keep the conducting dot level inside the bias window. Note, the

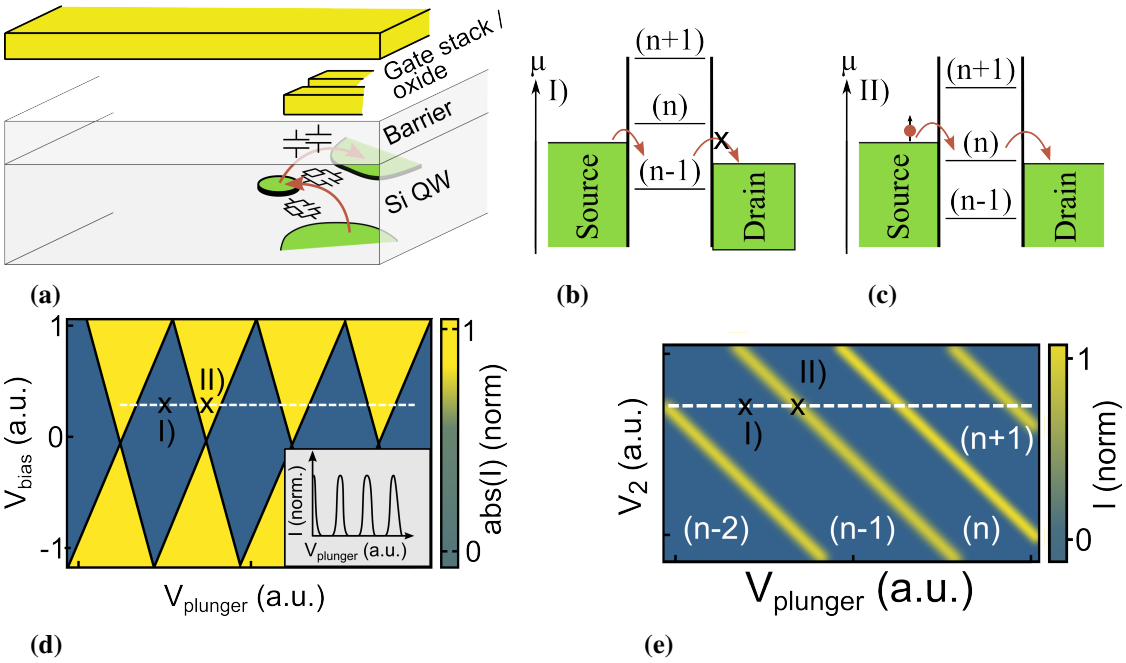
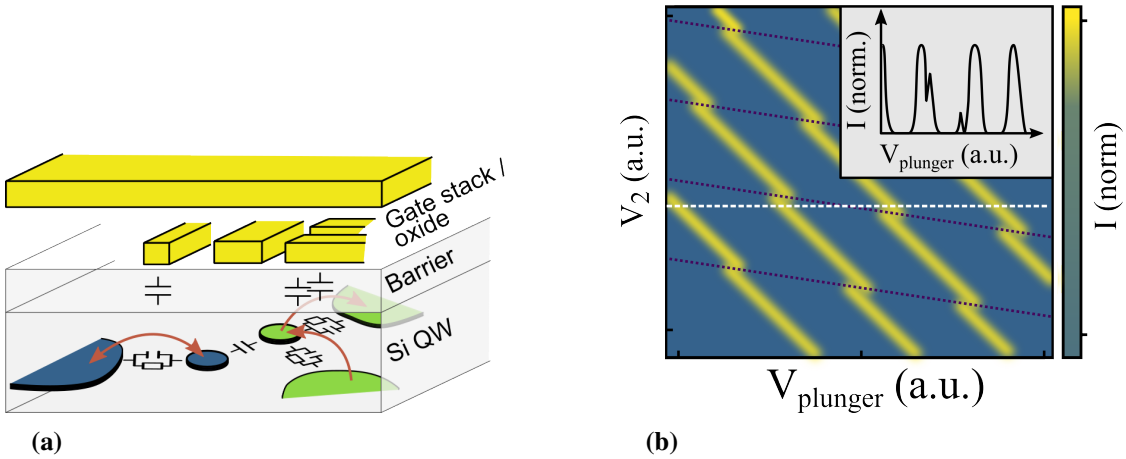


Figure 2.4: Transport through a single quantum dot. **(a)** Sketch of a quantum dot, tunnel coupled to two electron reservoirs. **(b),(c)** Energy diagram for Coulomb-blocked transport **(b)** and transport via sequential tunneling **(c)**. **(d)** Coulomb diamond measurement. Current through the SET is blocked in the blue diamond-shaped configurations. The Inset shows a linecut through the measurement, in which single peaks emerge when current is conducted. **(e)** Charge stability diagram. Current is conducted for the configuration along the yellow diagonal lines. In between two consecutive lines, the electron occupation of the SET remains constant, indicated by the white numbers.

white horizontal dashed line equals the configuration of the white horizontal line in Figure 2.4d.

2.3.2 Readout of a spin qubit via charge sensing

We can use this SET as very sensitive electrometer to perform a charge state readout of a proximal qubit dot. The situation is sketched in Figure 2.5a
The figure shows a device featuring both, a SET on the right hand-side in green and a capacitively coupled quantum dot in blue, which is tunnel coupled to a third reservoir. The current through the SET as function of two voltages $V_{plunger}$ and V_2 is shown in



(a) (b)

Figure 2.5: Charge sensing. **(a)** Sketch of a device featuring a SET (green) and a second quantum dot that is tunnel coupled to a reservoir (blue). **(b)** Charge stability diagram. The yellow diagonal transport lines of the SET are chopped by leaps in the gate voltage whenever the second quantum dot changes its electron occupation (dashed purple lines).

Figure 2.5b. Similar to Figure 2.4e, we observe lines along which current through the sensor SET is conducted (yellow diagonal lines) whenever an energy level is tuned into the SET bias window. In contrast to the previous figure, the yellow lines shown here now do have kinks following also parallel lines, indicated by the purple dashed lines. These purple dashed lines originate from the capacitively coupled second quantum dot: Whenever an electron tunnels onto the dot, the electrostatic potential for the SET is slightly lowered, resulting in a voltage jump within the measurement. A line-cut through the measurement along the white dashed line is shown in the upper right insert. In the insert, the voltage jumps emerge as kinks along the Coulomb peaks as a function the single gate voltage.
Via the detection of such kinks in the sensor current we gain insight on the electron occupation of the qubit dot. Crossing one of the purple dashed lines in the measurement is equal to a variation of the second quantum dot occupation by one electron.
Detection of the second dot occupation via this charge sensing is reasonable as soon as we lower its electron occupation down to a few or even a single electron, as in such a configuration direct transport measurements are no longer possible.
Note that also the charge sensing lines have a diagonal slope due to cross coupling of the varied gates. Depending on the geometrical location of sensor and qubit dot, the slopes of transport peaks and charge sensing lines may vary.

2.3.3 Spin qubit in a magnetic field

So far we introduced discrete energy levels of the quantum dot which arise due to an occupation of the quantum dot with a discrete charge carrier number. We derived the energy level structure from a semi-classical approach. In this section we now want to analyze the energy structure of a single electron occupation level, considering also quantum mechanical effects.
Like mentioned in Figure 2.1c, the sixfold conduction band minimum in silicon along the [100] direction in the Brillouinzone is lifted due to the strained growth of the silicon quantum well, leaving the two lowest-energy valley states along the growth direction lowered in energy. Moreover, the electron wave function is not centered inside the quantum well, but slightly pulled to the upper quantum well interface due to the band bending and the applied positive electric field. As a result, the remaining two-fold degeneracy of the valley states along the growth direction is also lifted. This lifting of the degeneracy is sketched in Figure 2.6a [82]. We denote the energy of the splitting of the lowest two valley states as valley splitting (E_V).

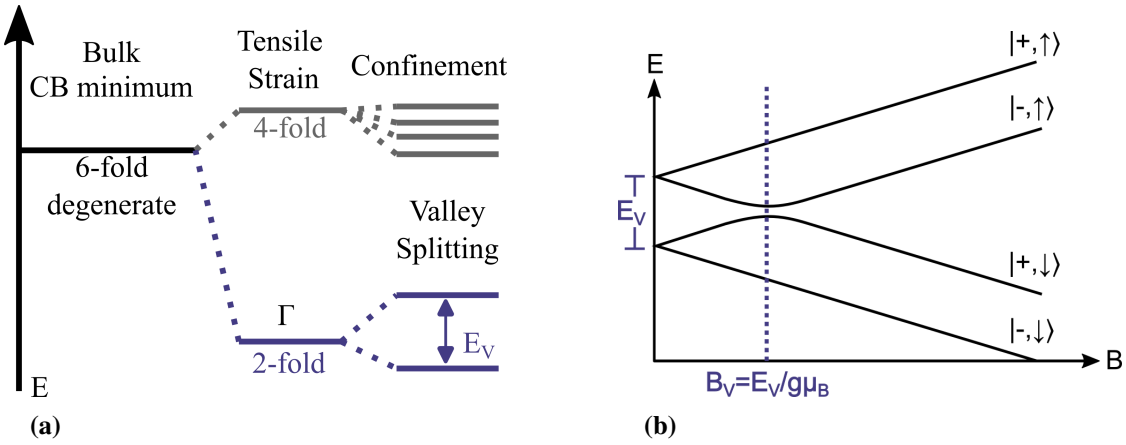


Figure 2.6: Energy states of a spin qubit in a magnetic field. **(a)** Lifting of the degeneracy of the silicon conduction band minima. Figure adapted from [82]. **(b)** Valley and Zeeman splitting as a function of the external magnetic field.

Moreover, also the spin degeneracy is lifted by the application of an external magnetic field. We will use the resulting spin up and spin down states for implementing our two-level system intended for quantum computing. The energies of spin and valley states as a function of the applied magnetic field are shown in Figure 2.6b. The figure marks the crossing point at which the Zeeman splitting matches the valley splitting. Typical values for the valley splitting energies can range from only a few µeV to more than 200 µeV [58].

Right at the crossing point, a spin up electron can energetically relax very quickly to a spin down electron, so this relaxation hotspot must be avoided in the operation of a qubit device. Typically, a large valley splitting is desired so that quantum computation can be performed at magnetic fields below the crossing point.
We emphasize, that in this description we focused on the (n=1) state of the quantum dot. Adding a second quantum electron to the system, the additional electron cannot simply occupy the second lowest spin and valley state, but the charging energy to fill up the next charge-quantized state has to be overcome.

Spin manipulation via coupling to the electron spin

For our qubit implementation we are going to use the two lowest spin-split states of the qubit electron from Figure 2.6b. To visualize the driving of the electron spin, oftentimes the spin rotation is presented in the so-called Bloch sphere as illustrated in Figure 2.7. In this presentation, the surface of the sphere marks all pure spin states and the spin up state is illustrated at the north pole and the spin down state at the south pole. The Figure

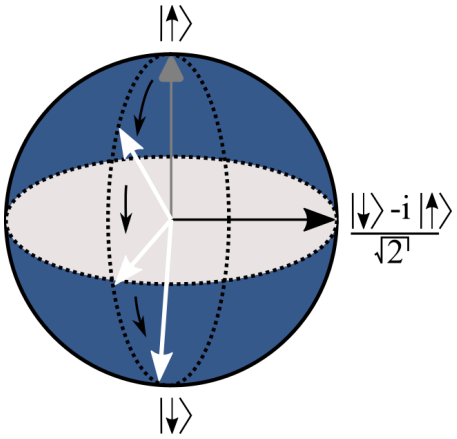


Figure 2.7: Bloch Sphere. Visualization of Rabi oscillations.

here shows a potential driven rotation between the spin up state and the spin down state, a so-called Rabi oscillation. To drive such a qubit rotation, a coupling to the electron spin is required. As the spin does does not directly couple to electric fields, there are different approaches. For systems with large spin orbit coupling (like GaAs or holes in Si), a resonant AC electric field applied to a plunger gate suffices to resonantly wiggle the electron wave function and via spin orbit coupling the electron resonantly sees a varying AC magnetic field modulation. In silicon this large spin-orbit coupling is not given, so we typically incorporate a small magnet into our metal-gate stack, which induces a magnetic

field gradient. Application of an AC electric field can drive electric dipole spin resonance (EDSR) by wiggling the electron wave function in the magnetic field gradient.
A second approach is to incorporate a microwave stripline in the gate stack and to directly apply a resonant AC magnetic field next to the qubit dot.

Single-Shot spin readout

Readout of the qubit spin is challenging as the small magnetic moment of the spin cannot be detected directly. Therefore, we refer to a concept called spin-to-charge conversion [84, 85]: We link the spin orientation to the existence or absence of an electron tunneling event, which we can detect by our SET charge sensor. In our single dot system, we realize this conversion, by tuning the spin-split energy levels such that the lower-energy spin down state is tuned below the Fermi energy of the reservoir during the readout and the spin up state remains higher in energy. An illustration of a complete single-shot spin

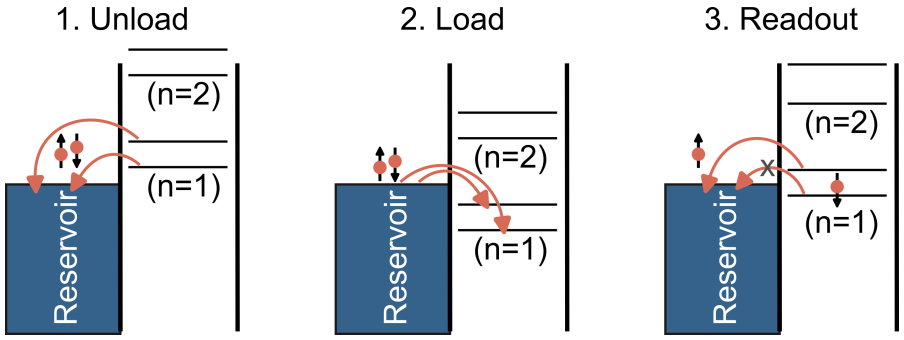


Figure 2.8: Single-shot spin readout. The measurement sequence consists of three phases: First the qubit is unloaded and subsequently an electron of arbitrary spin orientation is loaded onto the quantum dot. During the readout, spin up and spin down orientation are distinguished as only the spin up electron can tunnel to the reservoir, while a spin down electron remains confined on the qubit dot.

readout measurement cycle is shown in Figure 2.8. The measurement sequence consists of three consecutive phases. In the first phase, the qubit dot is unloaded by pulsing both spin states of the (n=1) electron above the Fermi energy of the reservoir. In the second phase, both spin states are pulsed below the reservoir energy so that a single electron of arbitrary spin orientation can tunnel onto the qubit. During the readout process, a loaded spin up electron will tunnel out of the dot into the reservoir and eventually gets replaced by a spin down electron. Note, with this technique we can identify the spin orientation of a single electron once at a time. Hence we call this scheme a single-shot readout measurement.

Qubit initialization and readout: The role of the reservoir

The reservoir plays a decisive role for the qubit initialization and readout: So far we treated the reservoir as a perfect 2D reservoir with a continuous distribution of states and considered the initialization of an empty dot by 50% spin up and down orientation, respectively. Also the possibility of tunneling to the reservoir during the readout to discriminate spin up and down was considered without restriction, assuming a continuous density of both spin states in the reservoir. The situation however changes when a proximal SET is used as a reservoir and the qubit dot alignment to discrete energy states of the reservoir has to be considered. The role of the density of states within the reservoir will be discussed in the main text of this thesis in more detail.

Readout of a two-dot system via Pauli spin blockade (PSB)

The readout scheme may also be implemented differently for the operation of two tunnel coupled qubit dots, both occupied by a single electron. This readout protocol is for example described in the review [9]. Both electron wave functions will entangle, forming singlet and triplet states. When the electrostatic energy is tuned such that both electrons occupy the right quantum dot, the spin singlet S(0,2) state typically is lower in energy compared to the three triplet states T(0,2) as due to the Pauli exclusion principle some excitation, like the valley splitting energy, has to be overcome for the symmetric spin triplet states. By the application of a magnetic field, the T_+ and the T_- triplet states are energetically split off and the neutral T_0 and the singlet state S form an effective two-level system [56]. A three-phase single-shot spin readout could then be designed by tuning into the (0,1) state for unloading of the system, followed by random initialization by tuning into the (1,1) configuration. Tuning the system subsequently into the nominally (0,2) configuration constitutes the spin readout: Triplet states are blocked to tunnel from the (1,1) state into the (0,2) state, called Pauli spin blockade (PSB). The S(1,1) state however will tunnel into the S(0,2) state [86, 87].

3

Setup and measurement techniques

3.1 Fabrication

All measurements presented in this thesis have been performed in undoped silicon/silicon-germanium heterostructures featuring a strained and buried silicon quantum well in which electrons are accumulated in a 2DEG by electrostatically lowering the first accessible conduction band sub-band below the Fermi energy. All experiments are conducted at cryogenic temperatures below 2 Kelvin. Before presenting measurement results in the upcoming chapters, this chapter introduces the technical background of all experiments. First, the heterostructure growth and post-growth processing of the devices will be presented, before subsequently all three cryostat systems, in which the experiments were performed, are introduced. Finally, the focus is directed towards the measurement equipment and the electrical wiring inside our laboratory environment is presented.

3.1.1 Epitaxial growth of the heterostructure

The heterostructures of all our devices are grown via epitaxial growth: A monocrystalline growth of the semiconductor material under very low background pressure. Two different approaches for growing the material are common in the semiconductor industry and during both processes the alloy concentration of germanium and silicon can be controlled and layers as thin as a single monolayer of the semiconductor can be grown onto the substrate. For the fast industrial chemical vapor deposition (CVD) the semiconductor material comes as a compound with a volatile bond. The deposition is conducted in a vacuum chamber in which the volatile bond diffuses when the compound adsorbs to

the surface. At the University of Regensburg we have adopted an alternative epitaxy approach to the CVD growth. In our research group we have the possibility to grow a heterostructure via molecular beam epitaxy (MBE).

MBE

The following description has similarly been elaborated during my master's thesis in [75]. For the MBE growth the source material comes as highly purified solid state material and no precursor compound is required. The solid source material is evaporated by an electron beam inside an ultra-highly evacuated chamber. The growth in the ultra-high vacuum chamber and the absence of a precursor ensures a long mean free path of the evaporated atoms or atom clusters and ensures a very low impurity density during the growth. Inside the MBE chamber, the substrate surface is heated and evaporated atoms adsorb to the surface and cluster to begin the horizontal layer growth. Diffusion of atoms on the sample surface suppresses crystal defects. By controlling the source material flux with shutters in front of the effusion cells, mono-atomic layers can precisely be grown and the heterostructure be engineered. Also, isotopically purified source materials of silicon with a residual ^{29}Si concentration as low as 60 ppm are available at the University of Regensburg. MBE growth details are for example well described in the thesis of Dr. Christian Neumann [88] as well as in the thesis of Dr. Floyd Schauer [81]. Here, only a short overview is given [75].
The heterostructure is grown on a silicon substrate on top of which a relaxed SiGe graded buffer is grown, increasing the germanium concentration from 0% to 30%. The graded buffer is terminated by a constant composition layer. This total SiGe virtual substrate provides a thickness of about 4 µm and by grading the germanium concentration, threading disclocations induced by strain tend to relax towards the side and not vertically. Following the constant composition layer the about 10 nm thick strained silicon quantum well is grown. The heterostructure stack is completed by an additional 35-45 nm SiGe buffer and a 1 nm Si cap to prevent oxidation. A typical cross section of the heterostructure is illustrated in Figure 2.2.

3.1.2 Sample fabrication

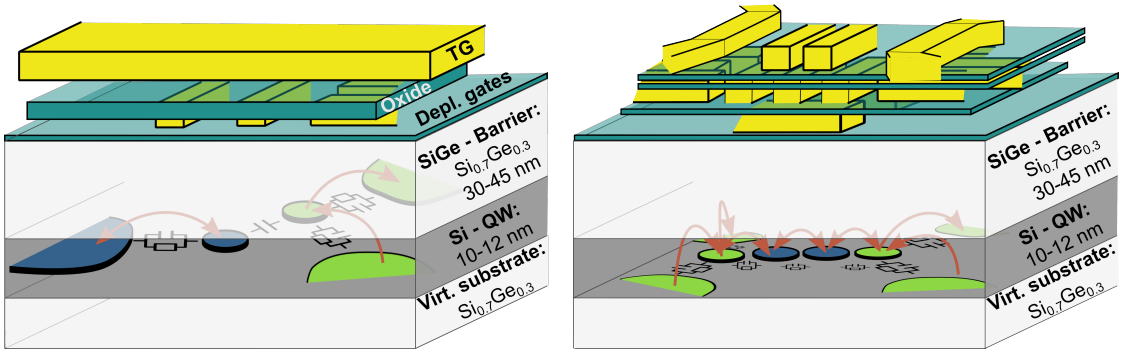
The MBE growth at the University of Regensburg is typically performed on 2 inch or 3 inch wafers. To fabricate a fully working qubit device from this heterostructure, additional post-processing steps are required. These routine sample fabrication has also been a larger part of this PhD project and the most important steps are briefly described here.
Ohmic contacts to the quantum well, which is buried by an about 40 nm thick SiGe barrier

under the sample surface, are defined locally by ion implantation of phosphorus atoms at a dose of $5{\cdot}10^{15}$ atoms/cm^2 at an energy of 20 keV and an angle of 7°. We observed that this ion implantation recipe is sufficient for contacting a quantum well buried as deep as 50 nm and that there is no need for a combination of the phosphorus atoms with larger arsenic atoms for ensuring a continuous contact also through the surface-near barrier. We also observed that a single acceleration voltage suffices and no higher- or lower-energetic ions are required for penetrating different depths in the sample to ensure a continuous electrical connection. Only for extraordinary deeply buried quantum wells changes to the sample recipe may be considered.
Upon implantation the single crystal is destructed. In order to heal crystal defects and simultaneously to integrate dopants into the crystal lattice and to activate these dopants, the implanted samples undergo a rapid thermal anneal (RTA) at a temperature of 700°C for only 15 s with a rapid thermal ramp. This annealing bears the risk of blurring the quantum well edges for a too large thermal budget. We achieved very good results with this short annealing procedure.
There is currently an ongoing development with first promising results in our research cooperation together with the RWTH Aachen University for substituting the thermal anneal with local laser annealing. Results can be found in the Master's thesis of Isabelle Sprave [89]. The idea of the laser annealing procedure is to only locally apply the thermal budget and the quantum well distant to the ion implanted regions remains unaffected.
Following the ion implantation and the crystal annealing, typically a first oxide layer is deposited onto the sample via atomic layer deposition (ALD) at 300°C. The rather high temperature during this ALD process contributes to suppress crystal defects in the oxide, but does not bear the same risk of blurring heterostructure interfaces as the RTA. There are also ongoing projects of growing this first oxide layer in an MBE process, before the heterostructure even leaves the MBE chamber. But this MBE grown oxide is prone to take damage during a regular RTA, so progress relies on a working laser annealing recipe.
The metallic gates on top of the sample are lithographically defined, mostly by electron beam lithography and for the fan out towards the sample edge, the structuring is supported by UV lithography. The lift-off process of the lithography is performed in a wet-chemical process. The used recipes and fabrication details are similar to those in the appendix of the thesis of [81, 88].

3.1.3 Qubit device: Accumulation vs. depletion mode

Two main approaches of confining and controlling single electrons in a silicon quantum well heterostructure were present for the design of the metal gate stack on the sample surface at the beginning of this thesis. One approach we will call depleting-mode architecture. This approach has been very successful for the first spin qubit devices. Also

during my master's thesis we extensively measured a depletion-mode device [58, 59, 75]. With the beginning of this thesis, a second approach that we will call accumulation-mode architecture emerged. Both approaches differ in the way the metal stack on the sample surface is designed and the gate voltages are tuned and consequently also differ in the way electrons are accumulated in the quantum well. As both working types are employed during this thesis, they are introduced and discussed in the following.



(a) **(b)**

Figure 3.1: Depletion vs. accumulation type of a qubit sample. **(a)** Illustration of a depletion-mode device. A global topgate (TG) for electron accumulation is designed across the whole quantum well, but it's electric field is locally screened by an underlying depletion-gate layer. As a result quantum dots are formed in the gaps between the depletion gates. **(b)** Accumulation-mode type illustration. No global topgate is present in this device. Each resulting quantum dot is defined directly underneath an individual gate, here in the third of three isolated metallic gate layers.

The depletion-mode architecture of qubit samples is sketched in Figure 3.1a. The figure illustrates the quantum well and the upper SiGe-barrier of the heterostructure. For simplicity the Si cap as well as the ion implantation are not drawn here. The figure illustrates a gate stack and two oxide layers fabricated on top of the sample. Characteristic for this depletion-mode architecture is a global topgate (TG) covering the whole active region of the sample and serving for the charge carrier accumulation in the quantum well. The local electron control is realized by the lower lying depletion gate layer. This metal layer screens the positive electric field of the TG locally, forming barriers and only allowing a quantum dot formation in between gaps of this depletion gate layer. Electron reservoirs are therefore formed everywhere, where no depletion gate is positioned directly above. The sketch in the Figure 3.1a is very much simplified as only two quantum dots

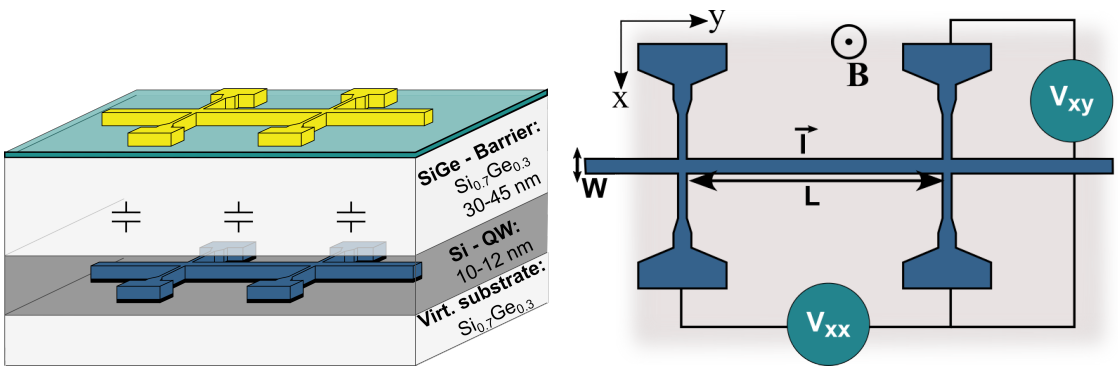
are drawn by only four depletion gates. Three depletion gates separate the quantum dots from the respective reservoirs and one depletion gate forms the inter-dot separation. The device is designed here to only allow a capacitive inter-dot coupling but allows tunnel coupling to the respective reservoirs. The green quantum structure forms a SET, which operates as a sensor for the device, while the blue quantum structure may serve as the qubit confining quantum dot and the related reservoir. Note, as all reservoirs are induced by the large TG we expect 2DEGs to form in the reservoirs.

The accumulation-type sample in Figure 3.1b does not feature a global TG. The sketch illustrates a sample with three metallic gate layers, all separated by oxide from each other. Here, each of the two blue quantum dots in the center of the quantum well has an own, dedicated plunger gate in the third metallic gate layer directly above. Also, the two quantum dots at the ends of the sample have a dedicated accumulation gate in the third layer. The second gate layer features gates which are used to form tunnel barriers in between the quantum dots and again each barrier has its own gate directly above. This is characteristic for the accumulation-type of devices. The first gate layer, often called screening layer, consists here of two horizontal and parallel gates, that have a gap in between. These two gates confine the electron accumulation to the channel in between, resulting in quantum dot formation exclusively inside the gap of these screening gates. The accumulation gates for the sensor dots fans out towards the edges of the sample, inducing 2DEGs for the sensor dots' reservoirs. Note, the blue quantum dots no longer feature a separate 2DEG reservoir but are loaded from neighboring quantum dots. This peculiar difference has been introduced in section 2.3.3.

The accumulation-type realization promises better tunability and less crosstalk between gates, but comes with the cost of a more complex fabrication as the pitch between gates becomes smaller and three gate layers compared to the two from the depletion type must be fabricated. For both types working qubit devices have been demonstrated, but the community trends towards employing the accumulation type design.

3.1.4 Hall bar sample

In contrast, a Hall bar device, which will be used for quantum Hall measurements throughout the thesis, does not require a complex gate stack. For this type of device, we typically fabricate a single gate on top of the sample surface, isolated by a 20 nm thick Al_2O_x layer like shown in Figure 3.2a.
The gate voltage induces a 2DEG in the quantum well in the shape defined by the gate geometry. Here, we drive a current I along the length of the Hall bar device. This current is indicated in the top view in Figure 3.2b. The geometry has pairwise connections along



(a) (b)

Figure 3.2: Hall bar device. **(a)** Single-gate induced 2DEG in Hall bar shape in the quantum well. **(b)** Top view of the Hall bar geometry. Voltage probes along and perpendicular to the Hall bar channel are indicated.

the Hall bar axis separated by length L and width W. If a magnetic field B is applied perpendicular to the 2DEG plane, the accumulated electron density and mobility can be calculated following the formulas in section 2.2.2, considering the width to length ration W/L, which amounts to a factor of 13 in our samples.

3.2 Cryostat

All transport experiments are conducted at temperatures below 2 K, so in a thermal environment in which the thermal noise does not disturb the measurements of quantum mechanical effects like the quantum Hall effect, Coulomb blockade or spin physics. In our laboratory we have three different cryostat systems available, all with different advantages and suitable for different device measurements. This section starts by introducing two cryostats using liquid helium for the sample cooling and then introduces a cryostat that uses a certain phase transition of helium isotopes for cooling to temperatures below 10 mK.

3.2.1 Liquid helium cryostats

To illustrate the working principle of the two cryostat systems using liquid helium, Figure 3.3 illustrates the dependence of the boiling point of four different gases/liquids on the pressure. While nitrogen has a boiling temperature of 77 K at atmospheric pressure, the temperature of ^{4}Helium at the same pressure is much lower at about 4.2 K, making

helium much better suited for our transport experiments. The graph also visualizes that a reduction in temperature is possible by reducing the gas pressure, allowing to reach a temperature below 2 K with technically available pumping techniques using ^{4}Helium. Even lower temperatures are available by using the ^{3}Helium isotope, which has a natural occurrence of only 1 ppm and is extremely precious. Both helium isotopes are the main coolants in the following two cryostats.

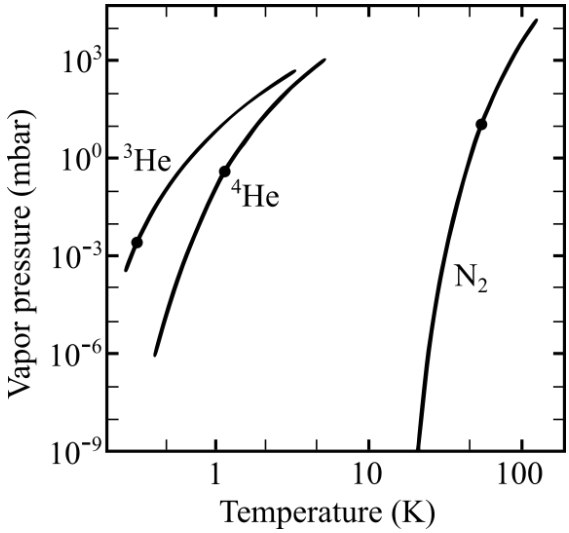


Figure 3.3: Boiling temperature of helium and nitrogen. Adapted from [90].

Dewar setup

The cryostat with the shortest sample exchange duration is sketched in Figure 3.4a. The setup consists of a ^{4}Helium bath, typically in a helium container filled with liquefied helium and a magnet rod featuring a smaller chamber inside a magnet coil. The smaller chamber, which we call the sample space, is filled with helium and the pressure inside can be controlled by the needle valve to the reservoir and a pump. Temperatures as low as 1.4 K can be reached inside the sample space. We prefer pumping at this small volume instead of the ^{4}Helium reservoir as pumping on liquefied helium in general comes with the drawback that a large amount of liquid helium is evaporated thereby.
A sample can be dipped into the sample space from above. All measurement lines are fed through the magnet rod. Both, sample and magnet rod, are grounded at a single point and loops are avoided by using isolated outputs of the measurement equipment. The cycle time of exchanging a sample is only a couple of minutes.

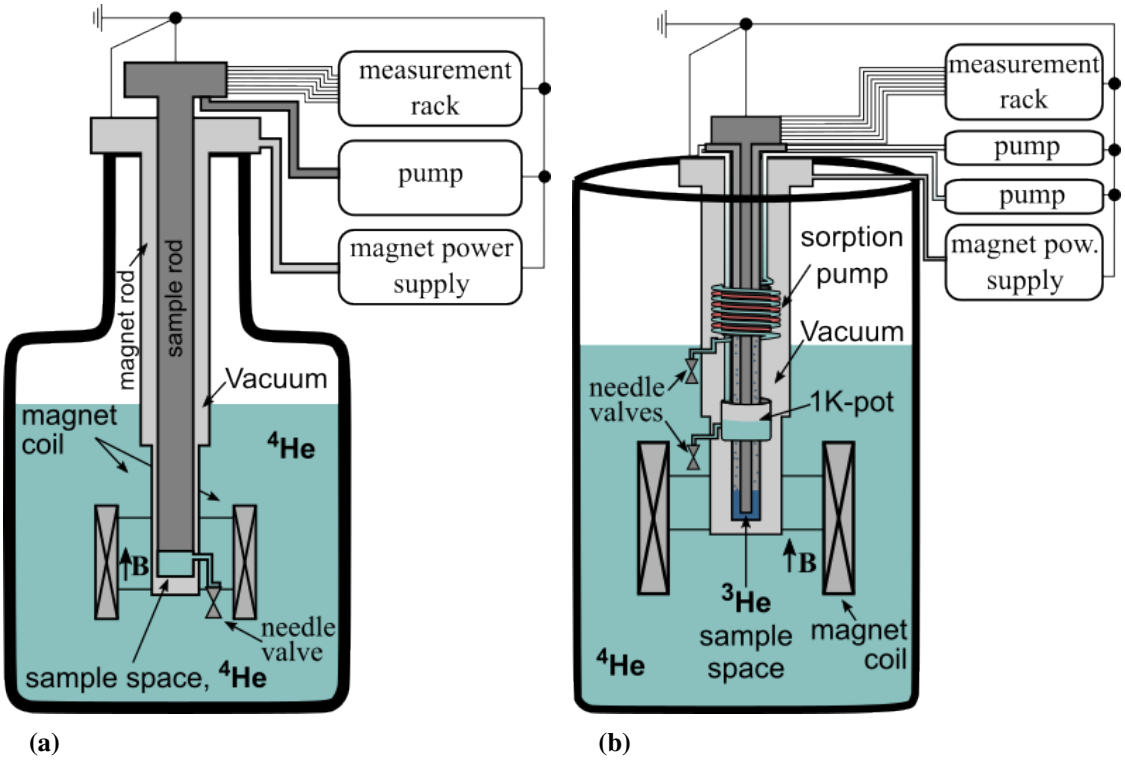


Figure 3.4: Liquid helium cryostats. (a) Dewar setup. The cryostat features a sample space that can be filled with liquid ^{4}Helium and the pressure can be reduced to reach temperatures as low as 1.4 K. Figure adapted from Martin Wieand [91]. **(b)** ^{3}Helium cryostat. The cryostat uses liquefied ^{3}He in the sample space to reach temperatures as low as 350 mK.

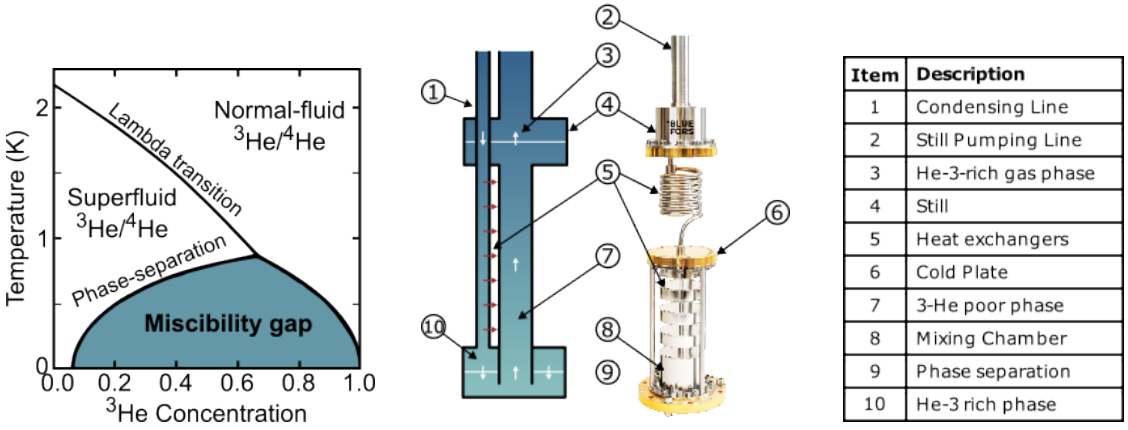
^{3}He cryostat

The big difference of the ^{3}Helium cryostat in comparison to the dewar setup is that the sample space is filled with liquefied ^{3}Helium instead of ^{4}Helium. The cryostat, which is sketched in Figure 3.4b, features two independent helium reservoirs. The large outer vessel is filled with liquefied ^{4}Helium and the insert is filled with ^{3}Helium. The larger outer ^{4}Helium reservoir cools a magnetic coil and is also used to control the temperature of a sorption pump in the insert. This membrane soaks up gaseous ^{3}Helium in the insert when cooled by ^{4}Helium from the reservoir and ^{3}Helium is released when the temperature is increased by a heater around the membrane. Helium from the large outer ^{4}Helium reservoir is also used to fill an additional small vessel around the ^{3}Helium insert, which is labeled "1K-pot" in the figure. The temperature of this vessel is controlled via the pressure

by a second pump and a needle valve towards the ^{4}Helium reservoir. Temperatures as low as 1 K are achievable here. Evaporated ^{3}Helium from the sorption pump will condense at the inner interface of the 1K-pot and ^{3}Helium insert and condense in the ^{3}Helium sample space. The pressure of this sample space is then controlled by a balance of heating and cooling the sorption membrane and hence the ^{3}Helium pressure. Temperatures as low as 350 mK are achieved.
Similar to the dewar setup, we chose a single point at the cryostat, typically the breakout box, for a common grounding point, from which the ground potential is distributed to all associated measurement equipment. A sample can be dipped into the ^{3}Helium sample space again above. The duration for a sample exchange is about 24 hours because the sample rod has to be evacuated before a cool down to not contaminate the precious ^{3}Helium.

3.2.2 Dilution cryostat

The coldest temperatures in our laboratory are reached by not using the temperature dependence of liquefied helium isotopes on the gaseous pressure, but by using a mixture of both isotopes and an endothermic phase transition between them. This phase transition can withdraw heat from the environment basically without any physical limit, so the temperature at the coldest stage of such a dilution cryostat is set at the equilibrium of cooling power by the aforementioned phase transition and the heat load from outside the cryostat.
Figure 3.5 illustrates the working principle of such a dilution cryostat. Figure 3.5a shows three different phases of a ^{3}He and ^{4}He mixture in dependence of the temperature and the ^{3}He concentration. The most relevant phase of the mixture is the blue highlighted phase for temperatures below 800 mK. Here, no arbitrary mixture of both isotopes is present any more. The helium will enter a ^{3}He poor phase mixture with exactly 6.4% ^{3}He. The remaining ^{3}He will condense almost purely as a second and separated liquid on top of the ^{3}He-poor mixture. Strikingly, it requires energy for ^{3}He atoms to condense from the ^{3}He-rich phase into the ^{3}He-poor phase. This is the basic working principle of a dilution cryostat to reach ultra-cold temperatures below 10 mK [92].
In a cryostat, this endothermic phase transition does not pose the only cooling process. The main cooling from room temperature to about 4 K is performed by two pulse tubes, that use the compression and expansion of helium as coolant to reach around 4 K and provide a much larger cooling power compared to the helium phase transition.
To reach a temperature below 800 mK for kicking off the endothermic mixing process, the mixture is condensed by compressing it and is fed into the dilution cycle, sketched in Figure 3.5b with explanation in 3.5c. The resulting heat following the compression is exchanged via heat exchangers and the helium mixture condenses after a flow impedance.



Item	Description
1	Condensing Line
2	Still Pumping Line
3	He-3-rich gas phase
4	Still
5	Heat exchangers
6	Cold Plate
7	3-He poor phase
8	Mixing Chamber
9	Phase separation
10	He-3 rich phase

(c)

Figure 3.5: Working principle of the dilution cryostat. (a) Phase diagram of a ^{3}He^{4}He-mixture, adapted from [90]. **(b)** Dilution unit of the cryostat. Figure adapted from the Bluefors LD System Manual [92]. **(c)** Table, labeling the dilution unit.

This will provide condensed helium in the mixing chamber. Almost pure ^{3}He is brought via the condensing line into the mixing chamber, in which it is forced to cross the phase boundary resulting in cooling of the system as explained at the beginning of this section. ^{3}He is removed from the mixing chamber by pumping at the still, which is at a temperature of about 1 K, evaporating solely ^{3}He but not ^{4}He and via osmotic pressure ^{3}He from the mixing chamber is fed into the still chamber. The so-removed ^{3}He is again fed into the mixture via the condensing line, completing the cooling cycle [92].

3.3 Electrical equipment

After introducing the working principle of the cryostats, in this chapter the focus is directed on the electrical wiring of the samples in the respective cryostats. As the dewar and the ^{3}He setup resemble each other, both are discussed together, before the dilution cryostat and subsequently all the single measurement components are introduced separately.

3.3.1 Electrical connecting concepts in the different measurement setups

Dewar and ^{3}He system

In both liquid helium cryostats, the sample is glued and bonded into a 20-pin ceramic sample carrier which is screwed into the sample rod, contacting the sample carrier from the backside with spring contacts. Measurement lines are fed through the sample rod and the sample is lowered from room temperature slowly down the cryostat until the sample enters the sample space with liquefied helium.
Both cryostat systems are designed similarly regarding the electrical connection. They feature 20 DC lines each. RF-frequency signals cannot be passed onto the sample in both setups. The measurement lines from the sample space to room temperature are twisted pair loom wires which do not pass a filter before contacting the sample. Electrical shielding of the measurement lines is given only by the outer sample rod. A typical material for the twisted pair loom wire is manganin in our laboratory. Loom wires are suitable because they offer a good immunity against fluctuating magnetic fields through conductor loops along the loom wire. Such fields may induce currents, but because of the twisting, fluctuating magnetic fields induce currents with exactly opposite sign in neighboring conductor loops. In both systems there is no dedicated thermalization of the wires despite wraping the loom around inner parts of the sample rod.
In general, a coaxial measurement line may also be considered, because it would offer a shielding against electric field fluctuations, but we experienced that while thermalization of the outer conductor of a coaxial line is straightforward, it turns out to be very difficult for the inner conductor of a coaxial measurement line.
The loom wire coming from the sample space terminates in a breakout box at room temperature which offers Fischer or BNC connectors. Here, measurement devices can be connected, typically via a switchbox, simplifying the plugging of measurement devices and also allowing to ground each measurement line.
For avoiding ground loops, we set a common ground point at the breakout box in both setups, indicated in Figure 3.4. We then have to take care that no second ground connection is given by any of the used measurement equipment, as two ground connections lead to a ground loop. All equipment should either be exclusively grounded to the dedicated grounding connection at the breakout box or must be electrically isolated from this point. Typically, the measurement equipment like Lock-In amplifier or DC-voltage source do have isolated outputs for that regard. The pumping line can be isolated by interrupting a metal corrugated tube by a short isolating Teflon piece. Special care has to be taken when integrating a measurement PC into the electrical circuit, as the PC typically constitutes a second ground connection. There are generally two solutions in that regard: Either

the measurement equipment has to be electrically decoupled from the PC via optical separators or the PC must fully be integrated into the ground circuit while interrupting the additional ground connection from the power cable via an isolating transformer. Both approaches have been applied in our laboratory and do work. A ground loop can be detected very simple: After removing the common ground connection at the breakout box, the electrical circuit should have a resistance larger than 1 MΩ to ground.
If a ground loop is present in the system, it appears with enhanced 50 Hz noise due to the the AC voltage from power sockets of all electrical devices. We observed that besides best efforts, we could not totally suppress the 50 Hz noise. Therefore, in any DC measurement, we emphasize to integrate a signal only over integer multiples of these power line cycles. We also observed what we call undershoot in DC measurements stemming from a potential ground loop, described by Carlo Peiffer in his Master's thesis [93].

Dilution cryostat

For the mixing cryostat the wiring is illustrated in Figure 3.6. The upper half of the figure shows an overview of the electrical devices. Illustrated are the AWG, the DC source, the analog-to-digital-converter (ADC) with both amplifier and IV-converter/amplifier, which will all be introduced in detail in section 3.3.3, as well as the microwave signal generator (Rhode & Schwarz, SMW 200A).
The bottom half of the figure shows an image of the cryostat inside. 6 different temperature and shielding stages are visible, with temperatures decreasing from the outer to the inner stages or equivalently from top to bottom. The figure shows the room-temperature plate, the 50 K stage, the 4 K plate, the still plate, the cold plate and the mixing plate. At the mixing plate we reach temperatures below 7 mK base temperature. For the wiring we incorporate three different types of measurement lines from room temperature to the sample mounted at the mixing plate. High-frequency signals are conducted via coaxial SCuNi/CuNi wires. For the measurements presented in this thesis, we have not used these lines in the experiment so far, but they will become essential when driving a qubit at frequencies approaching 20 GHz. They are specified to an attenuation of 9.5 dB/m at 10.0 GHz at room temperature and 4.6 dB/m at 10.0 GHz for 4 Kelvin. The coaxial lines are thermally anchored via attenuators at the 4 K plate with 20 dB, at the still and cold plate with 6 dB, respectively, and with 3 dB at the mixing plate.
The system is additionally equipped with 12 twisted pairs of PhBr as well as 12 twisted pairs of Cu-NbTi/CuNi DC lines, making 48 DC lines in total. The DC lines are thermalized by gold-plated copper bobbins at each temperature stage and there is no additional electrical shielding of the lines. The signal via the DC lines is filtered by a filter mounted on the mixing plate, which was installed during this thesis. The filter was manufactured by QDevil (Quantum Machines). The filter is built in multiple stages. It

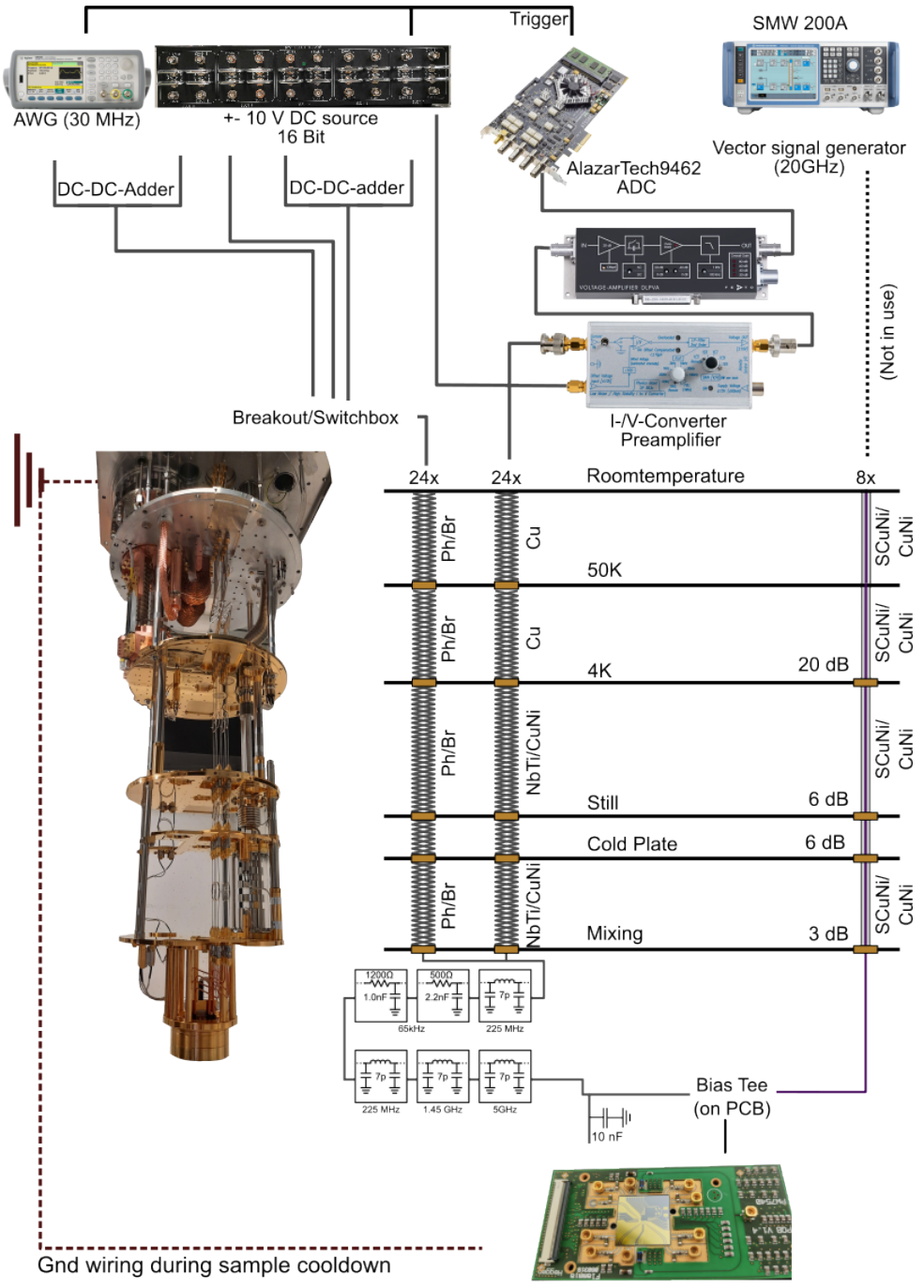


Figure 3.6: Overview of the electrical wiring around the dilution cryostat. Picture of the PCB by Dr. Arne Hollmann [94].

consists of an audio frequency (RC) filtering board, followed by a radio frequency (RF) filtering stage. The RC bank consists of one reflective 7-pole Pi filter stage and two dissipative RC filter stages, which are all individually shielded. The cutoff frequency of this lowpass is specified to 65 kHz if taken stand-alone and has a total serial resistance of 1.7 kΩ. The second RF bank consists of three 7-pole Pi filter stages for attenuation above 225 MHz with a total resistance of only 2 Ω.
In our system, we do have an additional 10 nF capacity to ground on the PCB sample holder, reducing the low-pass cutoff frequency to about 8.35 kHz. Details on the sample integration into the system via the PCB sample holder will be given in 3.3.2. Additionally, we add a current adder (DC-DC-adder) at room temperature, discussed in section 3.3.3, with resistance of about 100 Ω, reducing the total low-pass cutoff further to about 7.8 kHz in total.
The figure highlights the possibility to cool a sample with grounded contacts interruption-free via a second set of DC wires in the system, which are disconnected from the sample upon connection to the mixing plate.
To avoid any ground loops via multiple grounding contacts, the top plate of the cryostat at room temperature poses the only connection to ground potential and from here the ground is distributed to all measurement devices. We decouple the measurement PC from the grounding circuit by installing a differential amplifier in front of the PC-mounted ADC. The connection from the measurement PC to the remaining measurement equipment is optically isolated.

3.3.2 Printed circuit board (PCB)

For the integration of a sample into the dilution cryostat we use a printed circuit board designed at the RWTH Aachen University. It features 57 DC lines that are filtered by 10 nF to ground. The PCB also features 8 bias-tees (10 MOhm, 3 nF) to 8 HF lines with SPMP connector, combining RF frequency and DC signals onto one common measurement line. It additionally features 2 HF lines without bias-tee, 2 RF tank circuits (820 nH, 1 kOhm, 10 nF) and a laser diode which all will not be used in the experiments within this thesis. The bias-tees are specified to a loss of only 4 dB at 20 GHz. The center of the PCB provides space for a 20 mm x 20 mm interposer or direct installation of a sample. Using the interposer, which is a metal structured piece of silicon, may help for avoiding electrostatic damage of the sensitive sample during bonding or installation into the cryostat, as the silicon shortens all contacts at room temperature, but becomes isolating at cryogenic temperatures. The interposer is also designed to provide wave guides for less attenuation of high frequency signals. The qubit sample may either be bonded directly to the NiPdAu contact pads of the PCB or first onto the interposer and then to the PCB, which will require 2 bonds per line. Special care has to be taken when

working with the SPMP connectors for the RF signal, because those are very fragile when connecting. The PCB is screwed to the sample holder for thermal contact. The sample in turn is thermalized mainly via its bond wires.
We plan to use two different PCB sample holders, one for in-plane and one for out-of-plane magnetic field orientation.

3.3.3 Digital-to-analog converter (DAC) and arbitrary waveform generator (AWG)

DC voltage source and DC Adder

As main DC source we use a custom-build 20 channel ±10 V, 16 bit resolution DC voltage source (Concept from RWTH Aachen). The source provides a resolution of $\Delta V = \frac{20}{2^{16}}$ V $\sim$ 300 µV. This resolution may be sufficient for tuning gates like the TG or the screening gates, but turns out to be too rough for the source-drain bias or certain plunger gate voltages, which require better voltage resolution. A simple solution for biasing the Ohmic contacts is to use a voltage divider (with a factor of 1/1000 in our experiments). As the serial resistance of the voltage divider adds to the resistance of the investigated structure, it should not exceed 1 kΩ. Moreover, a 1/1000 voltage divider limits the maximum bias from ±10 V to ±10 mV, but allows for 0.3 µV resolution, suitable for biasing Ohmic contacts in our samples. Note, for the source drain current we denote the contact which is connected directly to the voltage source the "source" contact, the second contact which is connected to the I/V conversion and amplifier we call "drain" contact. We can also bias the drain contact via the I/V converter, which features a 1/100 voltage divider, providing a ±100 mV bias at 3 µV resolution.

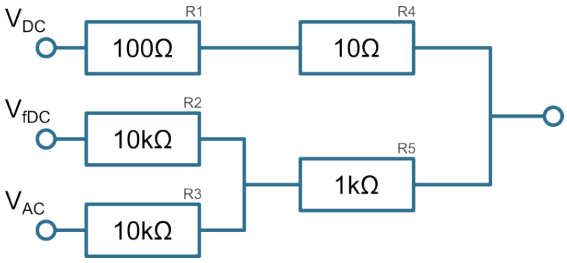


Figure 3.7: Voltage adder. Passive component consisting of resistors at room temperature adding three voltage sources onto a single measurement line.

For an increased voltage resolution, while maintaining the ability to apply voltages exceeding 1 V, we implement a concept, described by Felix Borjans from the RWTH Aachen University [95] illustrated in Figure 3.7. This passive component allows us to

combine voltages from three sources on the left side of the figure to a single measurement line on the right-hand side. The adder consists of only resistors at room temperature. In the illustrated application, we use it to combine one AC and two DC sources to a potential plunger gate that requires both AWG modulation as well as good voltage resolution and a rather large voltage bias. In the figure, both the V_{DC} input as well as the V_{fDC} connection are connected to a 300 µV resolution channel of our voltage DAC. The third connection V_{AC} on the left-hand side is connected to the output of the AWG. The resulting voltage V_{out} can be calculated using Kichhoff's laws:

$$V_{out} = V_{DC} - (2 \cdot V_{DC} - V_{fDC} - V_{AC}) \frac{R1 + R4}{R1 + R2 + R4 + R5}$$
$$= 0.0099 \cdot V_{fDC} + 0.0099 \cdot V_{AC} + 0.9802 \cdot V_{DC} \quad (3.1)$$

The result of the calculation can be interpreted as follows: V_{DC} basically sets the voltage of the output line by up to ±10 V and fine modulation can be achieved by V_{fDC} and V_{AC}, each dividing the input voltage by about 100, thereby also improving the resolution by the same factor.
Note, that total resistance of this adder limits the bandwidth of the AWG modulated DC line to a maximum of 7.8 kHz (3 dB damping at cutoff frequency). This type of DC adder works also for two inputs of the 16 bit DAC, allowing a fine gate voltage resolution on a measurement line without AC modulation, if required.

AWG

For the arbitrary waveform generation we incorporate a Keysight 33522A model with two analog output channels and a sampling rate of up to 250 MSa/s at 16-bit resolution, allowing the generation of 30 MHz square pulse bandwidth, clearly exceeding our setup-given bandwidth of about 7.8 kHz. For the AWG operation, we set all filters off and set the sample rate to 10^7 samples/sec. For programming all measurement routines, we define a driver which allows us to set the voltage offset and the amplitude voltage of the AWG signal in mV, already accounting for the subsequent voltage adder. We define signals of 10 data points length, corresponding to a duration of 1 µs for the chosen sampling rate at an output value between -1.0 amplitude to +1.0 amplitude. We used these type of signals to construct a sequence of up to many seconds length by repeating subsequent signals. For example, repeating a single signal 1000 times instructs the AWG to output a constant voltage for 1 ms, without the need to pass exceptionally many identical data points (10.000) to the AWG. During the construction of sequences, we also implemented waiting times and commands, instructing the AWG to wait for a trigger signal (for example from the ADC) to synchronize readout and voltage pulse sequence application.

3.3.4 Sample readout circuit

A challenge for all DC transport measurements is the need to measure very small currents on the order of 1 nA. In our setup we perform such low-current measurements by the incorporation of an operational amplifier based I/V-converter and subsequent digitizing of the amplified output voltage by a PC-integrated analog to digital converter (ADC). To interrupt ground loops, we plugged a differential amplifier in between measurement PC and I/V-converter.
In our setup we use the SP983C I/V-converter from Basel Precision Instruments and typically set the 2^{nd} order lowpass filter to a cutoff frequency of 30 kHz and the gain to 10^7 V/A. At this gain the maximum bandwidth is 90 kHz. A higher amplification may be desirable but comes with the cost of a limited bandwidth. For the next higher gain of 10^8 V/A, it is limited to 20 kHz. The implications of the amplification stage on the noise level will be discussed in the following section 3.4.
Following the I/V converter and its first amplification stage is a FEMTO DLPVA-100-F differential amplifier. We utilize its lowest amplification by a factor of 10, as we intend to only interrupt the PC ground by its installation. The bandwidth of the differential amplifier is set to 100 kHz, therefore not limiting our measurements. The amplified voltage signal finally is digitized by an AlazarTech ATS9462 digitizing card, which can record up to 180 MSamples/s on 2 channels with 16 bit resolution. The input range can be adjusted between ±0.2 V to ±16 V. Typically we set the input range to ±2 V, corresponding to ±20 nA with our total amplification of 10^8 V/A. We typically record with a measurement speed of about 10 kSamples/s. We use the 1 MΩ input impedance and use the ADC's trigger channel to synchronize all experiments: We program the digitizing card to always send out a trigger pulse when it starts to record. Also delays of this trigger may be implemented depending on the triggered device and the length of the trigger line.
For recording data, we implemented two main functions: We either record for 100 ms with the configured sampling rate and average the data to perform a single readout or we record a buffer of a desired range, which provides an array of sample points according to the configured sampling rate and buffer length. In both cases it is important to average always over integer multiples of the power line cycle to suppress noise at 50 Hz. Down-sampling of the data is also implemented in our measurement routine, which means recording at a larger sampling rate, but only returning data by averaging for example every 100 sample points and thereby effectively reducing the sampling rate by 2 orders of magnitude to save computational space.

3.4 Noise floor measurement of the setup

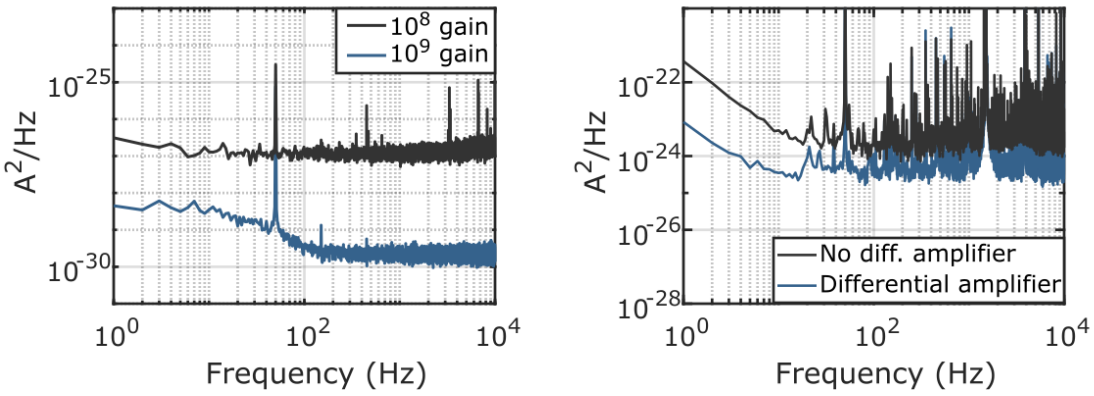
In the last section of this setup-introducing chapter we now perform a noise characterization measurement of our dilution cryostat setup with the aim of comparing different gain amplification settings of the I/V-converter and to demonstrate the importance of including the differential amplifier into the readout circuit.

Mathematical definitions

We perform a noise characterization by recording a continuous signal with our readout circuit and then transform this signal via a Fourier transformation to gain the power spectral density of the readout signal. Here, we perform the noise measurement in our dilution cryostat system without an installed sample, so we consider those measurements as measurements on an infinitely large resistance, giving inside in the minimal noise floor possible in the setup.
We transform into the frequency domain using a direct Fourier transform algorithm and normalize the resulting power spectral density (PSD) by squaring the transformed signal and dividing the result by (FS·NS), where FS is the sampling frequency and NS the number of sample points of the signal. In the conversion we have to take care that we are dealing with a single sided spectrum so we multiply by an additional factor of 2.
As the results remains unaffected in our analysis when using a Welch power spectrum ansatz, which allows to use different window functions, we omitted this approach.

Noise floor of the measurements for different amplification configurations

The measurements presented in Figure 3.8a demonstrate the importance of using the appropriate readout configuration. The figure shows two PSD spectra recorded in the dilution cryostat setup without a conducting sample. The two curves differ in the configuration of the I/V converter. For the blue PSD, the amplification of the I/V-converter was set to 10^9 and the lowpass filter to a cutoff frequency of 30 Hz. For this measurement we record a value of the noise amplitude at 10 Hz of 5-6 fA/$\sqrt{\text{Hz}}$ which is equivalent to the specification, given by the manufacturer of the I/V-converter. As no sample was connected during this measurement, we expect this value to be the lowest achievable in the system. We denote this value as the noise floor.
Currently this 10^9 A/V amplification is not viable for our experiments: For this gain factor, the I/V-converter is technically limited to a bandwidth of 1.2 kHz independent of the additionally used low-pass filter. This bandwidth is too small for recording single-shot spin measurements in our system, for which we desire a temporal resolution preferably faster than 100 µs.



(a) **(b)**

Figure 3.8: Noise floor characterization. **(a)** Measurements in the dilution cryostat for two different amplification settings of the I/V-converter. **(b)** PSD of the system with and without differential amplifier for ground decoupling.

The second largest amplification stage of the I/V-converter at a gain of 10^8 A/V offers a bandwidth of 20 kHz, which seems applicable for our measurements. The second, grey graph in Figure 3.8a shows the PSD recorded for this amplification and a lowpass cutoff frequency of 10 kHz. Clearly the noise floor is lifted to a value of about 30 fA/$\sqrt{\text{Hz}}$ at 10 Hz. For our planned measurements, this amplification gain is still not applicable, as the ensuing differential amplifier, that we only installed for interrupting the ground connection towards the measurement PC, has an input range of ±1V. Therefore with an amplification of 10^8 A/V at the I/V-converter, we are limited to 10 nA in all experiments, which we easily cross in our routine measurements. So we eventually decide to use only the third highest amplification of 10^7 A/V at the I/V-converter, for which we certainly are not bandwidth limited, as the possible maximal bandwidth is specified to 90 kHz, but this results in a baseline slightly lower than 1 pA/$\sqrt{\text{Hz}}$, much larger compared to the other two presented noise floors. The impact of the noise floor on all measurements will eventually be discussed in the final chapter of this thesis. For the remainder of the thesis we will use a 10^7 A/V gain at the I/V-converter in combination with an additional gain factor of 10 stemming from the differential amplifier. The lowpass filter is set to a cutoff frequency of 30 kHz.
The differential amplifier cannot be removed from the readout circuit as illustrated by Figure 3.8b. The figure shows a measurement with the I/V-converter set up like discussed and a second measurement with one amplification stage higher but without the differential amplifier. So both measurements have the same total amplification of $10^7 \cdot 10$ A/V, but the PSD recorded with installed differential amplifier has an order of magnitude lower

baseline compared to the measurement without the differential amplifier.
Most desirable would be a setup, in which the larger amplification of $10^8 \cdot 10$ A/V at the I/V-converter can be used without limitations, but this requires changes to the ensuing differential amplifier which cannot be omitted at the moment.

4

Hall bar study of the electron density

To characterize a 2DEG we usually refer to Hall bar device measurements as these devices are easier to fabricate due to the fewer amount of required fabricational steps and the significantly larger feature size which is more fault-tolerant in the fabrication process. Moreover, and without going into detail, Hall bar devices demand no particular gate voltage tuning and the devices typically endure many thermal cycles and are not prone to electrostatic discharge. So Hall bar devices constitute a simple means to study the characteristics of a heterostructure and many observations can be transferred to qubit device measurements.
In this chapter, we present studies on different samples with the focus first on the gate voltage induced charge carrier accumulation following the capacitor model and also the limits of this concept when the $n_{2DEG}(V_{TG})$ dependence enters a non-linear and hysteretic regime. We then present measurements of the temporal stability of the electron density right after accumulation (several minutes up to one hour) in the different regimes and present strategies to shift the accumulation turn-on voltage solely by gate voltage adjustments.

4.1 Stability of the accumulated electron density

4.1.1 Different gate voltage dependent regimes

Following equation 2.2, a 4-point Hall bar measurement provides a direct measure of the electron density which can be derived from the slope of the transversal resistivity in a magnetic field sweep.

Figure 4.1 shows the so-calculated electron density of a typical heterostructure as a function of the applied topgate (TG) voltage.

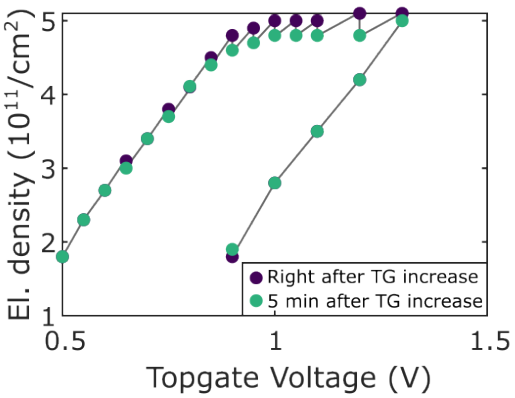


Figure 4.1: Typical $n_{2DEG}(V_{TG})$ dependence following the gate voltage induced electron accumulation. Three different regimes in the electron accumulation can be distinguished: For voltages below about 800 mV, the electron density increases linearly with the applied gate voltage. The density then eventually saturates and does no longer increase with enhancement of the gate voltage. Reducing the gate voltage, after this non-linear regime has been reached, the electron density again decreases linearly but with a hysteresis depending on how far the gate voltage has been increased into the non-linear regime before.

Starting from a TG voltage of about 500 mV, a current in the Hall bar is induced by occupying the quantum well with electrons. The figure shows a single continuous measurement series of the electron density, calculated from the transversal Hall resistivity. For each gate voltage two successive measurements of the electron density were performed, before the gate voltage was increased to the next higher value. The purple-colored data points present the calculated densities derived from a measurement that was recorded directly after increasing the gate voltage, while the turquoise data points were recorded about 5 minutes after a gate voltage increase.
The figure can now be separated into three different regimes. In the gate voltage range between 0.5 V and 0.8 V the density increases linearly with the applied voltage. In this voltage regime, the accumulation of electrons in the quantum well can conceptually be compared to a plate capacitor with the quantum well and the metallic topgate being the corresponding plates. The density increase terminates and the density remains constant at a value close to $5 \cdot 10^{11} \frac{1}{\text{cm}^2}$ for a topgate voltage exceeding 1 V. Reducing the voltage then again, the density decreases along a hysteretical course, not following the initial accumulation curve. Nonetheless, the decrease is again linear with the same slope as for

the initial accumulation.
This course has been observed before in a silicon quantum well and a model has been set up in [96, 97] and also in other heterostructures like described in [98]. Exceeding 1 V, electrons may occupy defect states at the oxide interface, screening the electrical field from the topgate and hence prohibiting an increase in the 2DEG electron density. These defect state electrons remain trapped when the gate voltage is decreased, leading to the hysteretical behavior.
The measurement also shows that for both linear regimes (the initial accumulation as well as the hysteretic de-accumulation), there is no significant density relaxation within the first minutes of measurement time. This is in strong contrast to the saturation regime in which a significant density drop is measured already within 5 minutes after a gate increase.
This measurement suggests to operate any gate-defined device in the linear gate voltage regime and to not drive the accumulation voltage too large, to prevent filling of trap states which in turn may lead to an unstable electron accumulation. In chapter 7, we will show that this activation of electrons also enhances charge noise in a gate-defined qubit device.

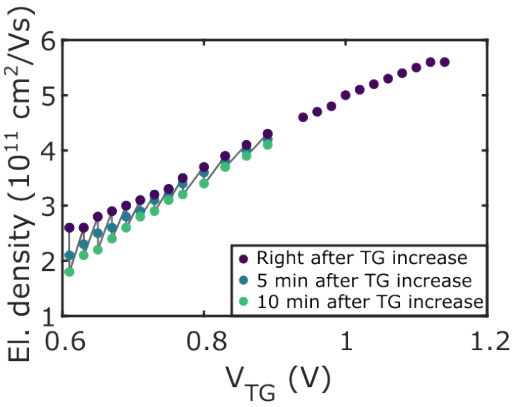


Figure 4.2: Electron density stability for low densities. At the onset of electron accumulation, we observe a significantly enhanced density instability. By further increasing the gate voltage into the linear accumulation regime the density relaxation is less pronounced.

In a next measurement of a sample on the same heterostructure we analyze the stability of the electron density at the other side of the accumulation spectrum, right when a first current in the 2DEG is induced. Figure 4.2 shows the $n_{2DEG}(V_{TG})$ dependence at the beginning of the linear accumulation regime. The applied voltages and densities can be compared to the device measured in 4.1, but the required gate voltages are about 100-200 mV larger compared to the previous measurement. The figure shows a continuous measurement that features three sets of data points for each gate voltage: The

measurement of the electron density right after setting a new TG voltage is colored in purple, the corresponding measurement 5 minutes later in blue and a third measurement after 10 minutes in green.
The measurement shows, that the accumulated electron density is more prone to density relaxation for low gate voltages and consequently a low electron density. The larger the gate voltage (and the carrier density) is set, the lower the density decreases over the first minutes. At a voltage of 900 mV, a reduction in density is barely measurable in the experiment.
An electron density measurement for yet lower gate voltages, which always takes a couple of minutes, has not been possible, as the density and hence the current through sample decreases such, that no significant current measurement was possible in that time span.
An explanation for that enhanced instability for low electron densities is given in [96]: The heterostructure is not ideally homogeneous, but has rather local potential minima. In a figurative sense, the quantum well features sort of local electron puddles. Transport along the Hall bar is possible by electron hopping between neighboring puddles, but only if a significant electron density is accumulated within the quantum well, continuous transport along the Hall bar occurs.
We however want to note, that we do not exclude temporal effects in this consideration here.

4.1.2 Effects of the oxide quality on the stability of the charge carrier density

To conclude the discussion about the electron density stability, Figure 4.3 presents a third $n_{2DEG}(V_{TG})$ measurement on a device from the same heterostructure. This measurement differs significantly from the previous two measurements. The graph shows the end of the linear regime for $V_{TG} < 2000$ mV and the regime of saturated carrier density for larger voltages. While the density is comparable to both previous measurements, the required gate voltage for its accumulation is significantly larger. Furthermore, we observe not only an unstable density in the non-linear regime, but also already in the linear regime. From both observations we conclude that for this Hall bar device, we have a bad oxide layer separating the metallic gate from the semiconductor heterostructure. This explanation can also be derived from the slope of the linear portion of the measurement, which is about 2-3 times flatter compared to Figures 4.2 and 4.3. As all three devices here were fabricated on the same heterostructure and nominally feature the same oxide thickness we deduce from that slope that the dielectric constant of the oxide is significantly lower, which also hints at a bad oxide quality.
We observed a bad oxide quality from the ALD process from time to time in our devices.

Bad oxides tend not only to promote the trapping of electrons, but also to allow leakage current between the gate and the heterostructure at comparably lower voltages.

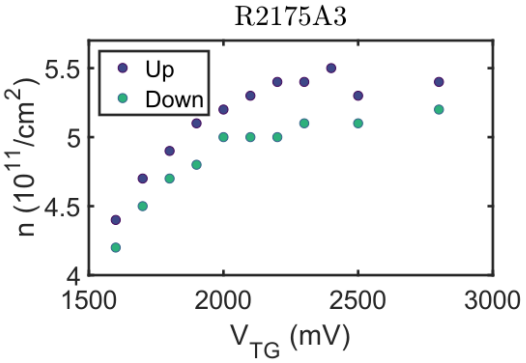


Figure 4.3: Electron density stability of a Hall bar sample with bad oxide quality. The electron density relaxes already along the linear accumulation branch. Also large voltages are required for the electron accumulation, both hinting for bad oxide quality.

As a quick intermediate summary of this section we want to note, that the most stable operation of 2DEG electron accumulation was achieved by a high-quality oxide layer and within the linear gate voltage regime of the accumulation, neither right at the onset nor in the non-linear and saturated regime.

4.2 Handling interface trap states in gate-defined quantum devices

In the previous measurements we observed experimental hints for charge trap states, that may be located at the interface to the oxide or inside the oxide itself. In this next section we want to discuss how to proceed with a device once the non-linear saturation regime has been reached and how to handle such interface trap states.

4.2.1 Reset of charge carriers

Following the band bending model described in [96, 97] we now attempt to un-charge the interface trap states at the oxide by either reducing the gate voltage or even by applying a negative voltage with the idea to bend the conduction band the reverse direction and hence to force electrons out of trap states. This experiment is performed in a Hall bar

device and shown in Figure 4.4. The figure shows a single measurement cycle. Following

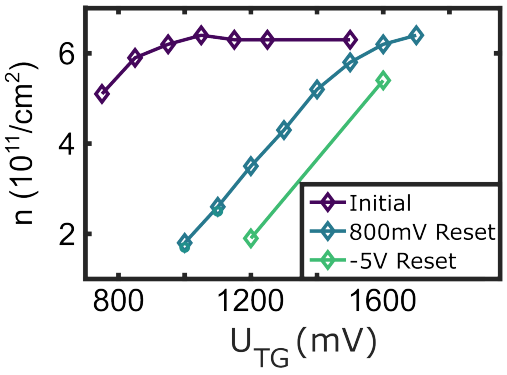


Figure 4.4: Reset attempt of the interface trap states by reverse band bending. Following driving the device into the nonlinear accumulation regime, charged trap states at the oxide interface remain charged despite lower bias application to the topgate.

the purple curve, the Hall bar sample is driven into the non-linear accumulation regime by increasing the TG voltage above 1 V. Subsequently, we decrease the TG voltage to 800 mV to try to discharge the trap states. Upon an anew voltage increase, marked by the blue measurement curve, we observe a shift in the whole accumulation branch, as the initial linear regime now extends as wide for positive gate voltages as the sample has been pushed into the saturation regime before. The electron density saturates above that threshold voltages at the same value as it has for the purple path before the reset attempt. Subsequently we perform a second reset attempt by setting the TG voltage to -5 V for a few minutes. Increasing it again and trying to measure the electron density n, we analogously observe, that the linear accumulation branch shifted to more positive gate voltages, very similar to the first reset attempt.
By this measurement we observe that a total reset of these once charged trap states at cryogenic temperatures seems not possible. Upon a thermal cycle of the sample and an anew cool down cycle however, the initial accumulation curve (purple in Figure 4.4) can be recovered.

4.2.2 Biased cooling

A natural question that appears now is, if there are already charges trapped at the oxide interface when the sample is cooled down. Tobias Weinberger [99] and Floyd Schauer [81] performed a study revealing that there are already charges trapped without explicit gate

voltage application. They also showed that by applying a bias at room temperature and during the device cool down, the trapped charge configuration can be modulated. A measurement series of the current accumulation for different cool down bias voltages is shown in Figure 4.5. The presented measurement was performed by Tobias Weinberger and Floyd Schauer.

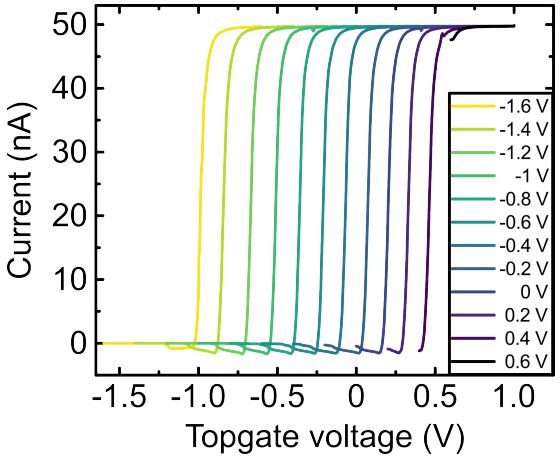


Figure 4.5: Biased cooling. Figure and measurement from Tobias Weinberger [99]. The turn-on voltage can be shifted by application of a cool down bias voltage at room temperature.

The figure shows that depending on the cool down bias, the accumulation curve shifts along the gate voltage axis as a result of freezing a different interface trap state configuration. Once the sample is cooled down, this trapped configuration remains frozen, unless the accumulation saturation regime is reached and further charges are trapped at the interface. Therefore bias cooling turns out as a deterministic measure of tuning the accumulation turn-on. This tunability can turn out beneficial if a certain voltage threshold cannot be crossed in a device operation, e.g. because of leakage current, but also if for example too many trapped charges prohibit a 2DEG accumulation in the quantum well in the first place.

4.2.3 Illumination of the sample

In their studies the authors also demonstrated a second and independent measure to shift the accumulation turn on by illuminating a device at cryogenic temperature with a red LED. They showed that independent of the hysteresis or applied gate voltage, the quantum well in a heterostructure stack can be tuned right before the onset of a 2DEG accumulation by the illumination. Increasing the topgate by just a small amount they demonstrated

electrons to be accumulated immediately.
Illumination of the sample has been applied to qubit devices frequently [100]. However, the illumination will excite electrons in the whole heterostructure, so we assume also a significant population of the interface states by that measure. In the measurements it turned out as a probabilistic process and to be not reproducible, so we recommend the illumination only if all other measures to accumulate a 2DEG inside the quantum well have failed.

4.3 Summary

In this chapter we analyzed the dependence of the electron charge carrier density $n_{2DEG}(V_{TG})$ on the applied topgate voltage V_{TG}. Despite the hysteretical character of this dependence, we observed that for most of the linear branch of the electron accumulation, the density turned out to be stable on a timescale of a few minutes while right at the onset as well as when driven into the non-linear saturation regime, electron density relaxation occurs. We explained the density relaxation in the non-linear accumulation regime by trapping charges at the semiconductor-oxide interface. The chapter then introduced biased cool down of a sample as a technique to manipulate the charged traps and thereby allows for tuning of the accumulation turn-on voltage. We also observed that the quality of the oxide can affect the density relaxation. For a lower oxide quality we observed density relaxation also in the linear section of the electron accumulation branch.

So far, in this chapter mainly the dependence of the charge carrier density on the applied gate voltage has been discussed. There is an extensive section in the appendix of this thesis, also presenting longitudinal and transversal resistivity measurements on Hall bar devices. In the appendix, the focus is directed towards the analysis of the electron mobility. Especially the longitudinal resistivity is analyzed as a function of the electron density for large magnetic fields, when the electrons condense in two or even only a single Landau level and the filling factor ν approaches $\nu = 1$. Also technical aspects of the 4-point Hall bar measurements are discussed, regarding the simultaneous measurement of multiple longitudinal and transversal resistances. Moreover, the actual electron temperature is derived from the thermal broadening of Landau levels with increasing cryostat base temperature but also due to heating when a larger current is induced through the hall bar device.

5

Asymmetric sensing dot (ASD)

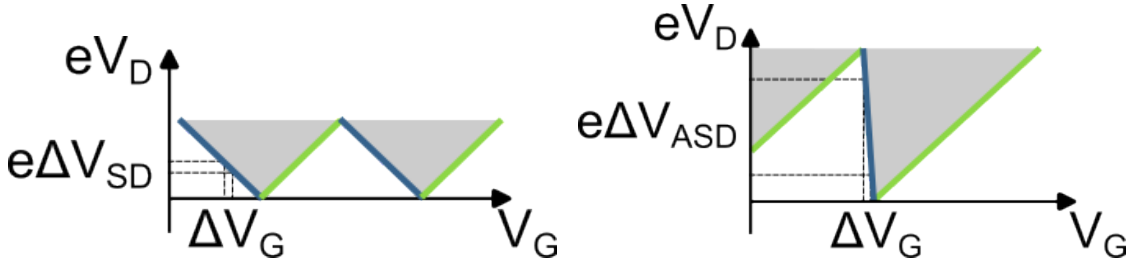
An important step for the development from the current NISQ era towards the turning of research-level quantum processors into an universal quantum computing technology is the scaling of the qubit number on a single processor chip. Certain aspects like the wiring and addressing of qubit sites need to be engineered. But also concepts for the readout of the qubit states have to be developed and implemented.
For gate-defined spin qubit systems, two different approaches of scaling the processor size were recently introduced. The concept of a dense qubit array [53] relies on multiplexing high-frequency signals and DRAM schemes for contacting a grid of qubits, but demands special homogeneity of all qubit sites. In the second concept of a sparse qubit array [68], physical records of qubit elements and classical electronics are proposed to alternate on a chip. Especially for this second scaling approach of using classical electronics on the same chip on which the spin qubit is implemented, also concepts for fast and high-fidelity readout of the qubit state need to be introduced, as a potential amplification of the measurement signal would be processed at the cold temperature at which the qubit is operated and the readout duration should be as fast as a single qubit gate duration.
Typically for semiconductor spin qubit systems, the single-shot spin readout is performed by spin-dependent tunneling. This dependence can either be implemented via Pauli blockade in a double qubit system [101] or by using the energy splitting given by the Zeeman energy and alignment to the Fermi energy of the reservoir [84]. In both methods conclusions about the spin state can be drawn by a readout of the amount of charge carriers in the qubit system, following the spin-dependent tunneling. We oftentimes refer to this concept as "spin-to-charge conversion".
The readout of the charging state in turn is commonly performed by recording the

conductance of a capacitively coupled SET [102] like introduced in section 2.3.2, or the so-called "RF-readout": The readout of an amplitude or phase change when a plunger gate or Ohmic contact of the sample is engineered into a LC circuit and driven at radio-frequency [103–107]. RF reflectrometry currently turns out to allow the fastest charge-state readout in less than 1 µs, which is roughly the timescale of qubit operations and clearly below the spin relaxation and dephasing constants. However, as microwave signals interfere up to a separation of a few centimeters, the need of installing bulky electrical components may hinder the scaling progress.
Transport readout measurements via a SET also has shown high-fidelity single-shot spin readout recently. But due to the comparatively large serial resistances of the SET in combination with shunt capacitances stemming from the wiring to room temperature amplifiers, the readout bandwidth is limited [104] and a single-shot readout typically takes about 100 µs.
For both readout schemes, the incorporation of some electrical components at cryogenic temperatures may turn out advantageous in terms of both noise and readout bandwidth. However, the thermal cooling power budget provided by commercially available cryostats as well as physical size demands of the classical electronics may limit such low temperature readout circuits. Especially for the baseband readout using a capacitively coupled SET, the signal amplification of small currents turns out very power-consuming and hence has so far required a large thermal budget, which scales with the amplification factor.

Here, we follow the baseband readout approach, measuring the current through a capacitively coupled SET, and present a new charge sensor concept intended to operate with a HEMT or HBT cryogenic pre-amplifier. As the thermal budget of the pre-amplifiers is related to their gain, an initial large sensor signal from the qubit device is favorable. Moreover, a large sensor response naturally provides significant improvement of the readout fidelity. We achieve a larger sensor signal by an asymmetric design of the capacitances from the Ohmic contacts onto the sensor dot. This chapter shows the from-scratch development of first a demonstrator device of such an asymmetrically coupled sensor dot, followed by a second, improved device version, including also adjacent quantum dots which may be used as qubits. We base the device development on simulations, performed by our collaboration partners at the RWTH Aachen University and show measurements in a Si/SiGe heterostructure system as well as complementary measurements in a GaAs based sample. The main results of this chapter have been reported in two publications [87, 108].

5.1 Concept

While charge sensing with constant sensor voltage bias is well established in the community and explained in section 2.3.2, our concept is based on a constant current readout of the sensor dot and thereby performing the charging state readout of a capacitively coupled qubit dot system.



(a) (b)

Figure 5.1: Sketch of the influence of the reservoir capacitances on a Coulomb diamond measurement. **(a)** Coulomb diamond measurement for a symmetric sensor dot. The graph shows the estimated current through a sensor quantum dot as a function of the voltage bias V_D and a plunger gate voltage V_G. Through the discrete qubit dot levels, blockade regions in diamond shape emerge, here illustrated in white, while the current-conducting regimes are colored in grey. The positive and negative slopes of the diamonds are highlighted in green and blue, respectively. The figure also illustrates the required bias change ΔV_{SD} to remain on the negative constant-current slope, following a change in the electrostatic configuration equal to ΔV_G. **(b)** Coulomb diamond measurement of a sensor dot with reduced drain capacitance. The negative slope is significantly steeper compared to the positive slope. The same electrostatic change ΔV_G results in a much larger bias compensation ΔV_{ASD}.

We show that the sensor voltage response ΔV_{ASD} increases by electrostatically decreasing the capacity between the drain contact and the sensor dot. This tuning of the capacity leads to strongly asymmetric and tilted Coulomb diamonds, significantly increasing the sensor signal. Figures 5.1a and 5.1b illustrate the resulting gain in the sensor response: Figure 5.1a shows a Coulomb diamond sketch of a symmetric sensor dot with equal capacitances to the source and drain leads. The two constant-current slopes of the diamond edges are highlighted. The negative slope m_- is colored in blue and the positive edge m_+ in green. The figure also indicates a small variation in the electrostatic configuration of the sensor dot ΔV_G which may arise due to an electron tunneling event in an adjacent qubit dot. When driven in constant current operation, a variation of $e\Delta V_{SD}$ of the sensor

bias is required to remain on the constant current edge m_-. This bias change constitutes our measurement signal.
Figure 5.1b shows a Coulomb diamond sketch of a sensor quantum dot for which the drain capacitance is much smaller than the source capacitance. This difference in the capacity reflects in the slopes m_- and m_+ which no longer equal and the diamonds appear tilted. Considering now the same small variation in the electrostatic configuration ΔV_G, the required bias change to remain on the m_- slope ΔV_{ASD} increases significantly.
To measure the gain in the sensor signal, we introduce the asymmetry factor (AS) which we define as

$$\mathrm{AS} = \frac{m_-}{m_+} = 1 + \alpha_D^{-1} . \tag{5.1}$$

This factor is inverse proportional to the drain capacity following the constant interaction model [83]. The figure now suggests that a large AS value is equivalent to a large voltage output swing.
The capacitances of the sensor dot to the reservoirs have typically not been designed frequently, neither in our working group nor in others. The gate layout of qubit dot devices normally is designed symmetrically to ensure tunability of the tunnel barriers separating sensor dot and Ohmic contacts.

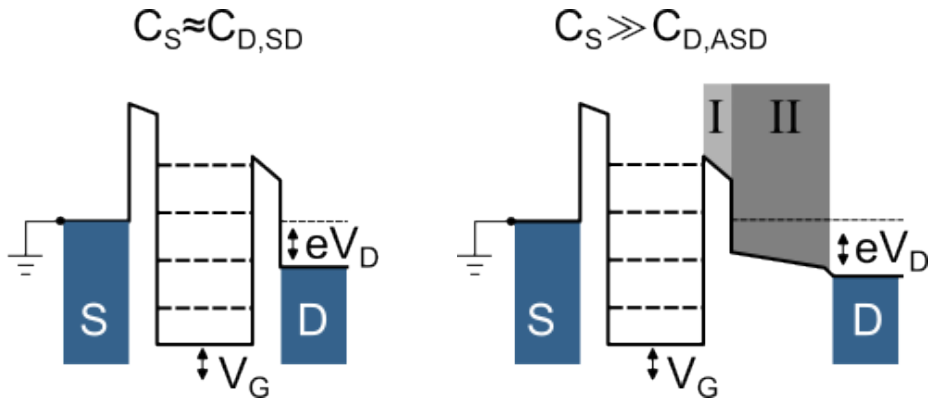


Figure 5.2: Sketch of the chemical potential of a symmetric and asymmetric quantum dot. (a) Symmetric sensor dot. **(b)** Asymmetric sensor dot (ASD). The decrease of the drain capacity is realized by two different regimes, a potential slide (II) and the tunnel barrier (I) to keep the quantum dot confinement similar to the symmetric dot.

We aim to implement the reduced drain capacitance by increasing the spatial separation from the sensor dot to the drain reservoir. The challenge by doing so is to keep the

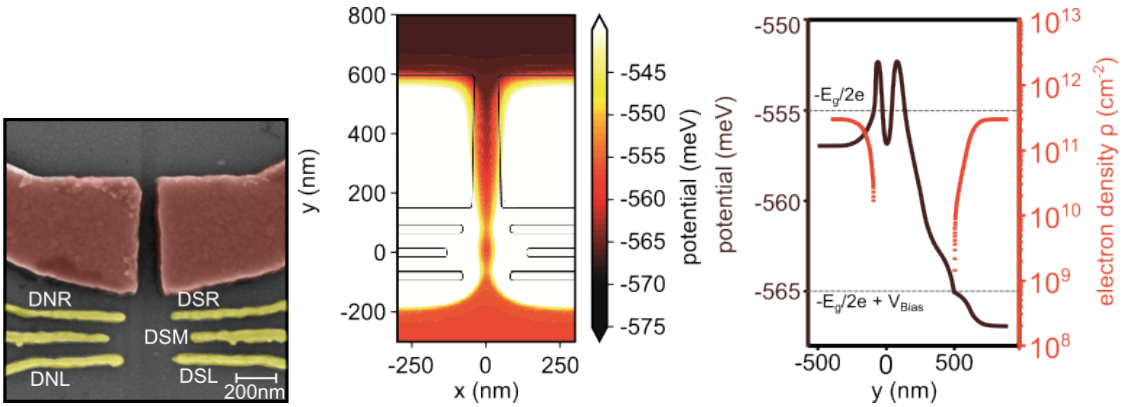
tunnel barrier separating sensor dot and drain reservoir unaffected in height and width. A sketch of an electrostatic potential of a symmetric sensor dot is shown in Figure 5.2a and a second sketch of an asymmetric sensor in 5.2b. For the symmetric sensor dot (SD), we expect the physical separation towards both reservoirs to equal and hence we expect the capacitances $C_S \simeq C_{D,SD}$ to resemble. In the asymmetric potential sketch we split the barrier to the drain reservoir into two sections, labeled by the Roman numbers. The section closer to the sensor dot (I) resembles the tunnel barrier of the symmetric sensor dot. As both barriers are intended to equal in width and height, we also expect a similar tunnel rate and hence current through the SET. Also, we expect to keep the quantum dot confinement upright, so that neither the sensor dot size nor its energy level structure change. The big difference to the symmetric sensor dot is the section II, which forms a potential slide towards the drain reservoir. By applying a larger bias voltage V_D to the drain reservoir, this potential slide causes a physical separation of sensor dot and reservoir and decreases the capacitance $C_{D,ASD}$.
The operation of the asymmetric sensor dot will require a larger bias voltage. This comes with two consequences. On the one hand, the larger bias may result in non-linear Coulomb diamond edges, but as for our intended usage we merely demand a large voltage swing, we will fit Coulomb diamond measurements as piece-wise constant for the calculation of AS factors. On the other hand, a larger back-action from the reservoir onto the qubit quantum dot may result from the increased bias. A study of such back-action effects is presented in the appendix of this thesis in A.2.2.

As typically the capacitances are not designed and as to our knowledge no such potential slide has been discussed in that detail in the community, we not only aim to demonstrate the working principle of charge sensing with constant current and improved sensor swing, but also to provide details of the from-scratch conception of a new gate design of a spin qubit device. One strategy for developing a new qubit device layout involves multiple fabrication and subsequent electrical transport measurements at cryogenic temperatures. From the transport measurements conclusions about the design can be drawn and an improved gate layout or device design can be fabricated in the next iteration. Such conclusions from measurements comprise e.g. the capacitive coupling of gates to a quantum dot, the sensitivity of the potential landscape to gate voltages, the risk of forming disruptive, additional quantum dots or insight regarding the challenge to deplete a quantum dot to the few-electron regime before the tunnel barriers become too opaque for electron exchange with the reservoirs. A fabrication and subsequent measurement cycle however is very time-consuming on the order of weeks or even longer. So here we take a different approach, presented also in our publication in [108]: We simulate the electrochemical potential and the electron density in the quantum well for a computer-modeled metal gate stack as a function of the applied gate voltages in a Comsol simulation using the Thomas

Fermi approximation for the Ohmic contacts. A big advantage of the simulations is a much shorter feedback cycle for design adjustments. Moreover, we can easily expand a working prototype model to more complex structures, for example featuring more than one single quantum dot. All simulations, that will be presented in this chapter, were performed by our collaboration partners Eugen Kammerloher, Inga Seidler and Malte Neul working at the RWTH Aachen University in the research group under guidance of Dr. Lars Schreiber.

5.2 Characterization of a 1st generation proof of concept gate layout

As a first step, we present the development of a simplified, prototype gate design intended to host a single quantum dot with reduced capacitive coupling to the drain reservoir while maintaining the tunnel coupling. For this prototype, we developed the gate layout shown in the SEM image in Figure 5.3a after multiple simulation feedback cycles. The device shown in the SEM image was fabricated at the University of Regensburg on an undoped $Si/Si_{0.7}Ge_{0.3}$ heterostructure featuring a 10 nm thick quantum well, buried 45 nm deep by a $Si_{0.7}Ge_{0.3}$ barrier and a 1.5 nm Si cap. The fabrication of this device was guided by Dr. Floyd Schauer. The device features two gate layers. The lower layer is separated by 10 nm ALD-grown aluminum-oxide from the heterostructure, features 8 gates and is shown in the SEM image: 6 tiny gates towards the bottom of the figure, false-colored in yellow and two large sliding gates towards the top of the image in red. The second layer is separated from the lower-lying one by 50 nm Al_2O_x and covers the whole active region of the device. We denote this second metal layer as topgate (TG). The TG is not shown in the SEM image.
The sample is designed to host a single quantum dot in between the yellow gates of the first gate layer. The middle gates are intended to serve as plunger gates and the four surrounding gates are intended to form potential barriers to confine the quantum dot and to control the tunnel barrier height to the reservoirs, which are accumulated on both ends by the global TG. The additional two large sliding gates now serve to form the potential slide.
A simulation of the chemical potential (Inga Seidler and Malte Neul, RWTH Aachen) of the device is shown in Figure 5.3b. For the simulation, a TG voltage of about 1 V and slide gate voltages of about 500 mV were applied, while the plunger and barrier gates were left at ground potential, equivalent to 0 V. The simulation reveals the formation of the sensor dot around x = y = 0 nm and a potential decline along an about 400 nm long channel around x = 0 through the sliding gates. At the top and the bottom of the figure



(a) **(b)** **(c)**

Figure 5.3: Proof-of-concept demonstrator device. **(a)** SEM image of the gate design resulting from multiple simulation cycles. **(b)** Simulation of the chemical potential after gate voltage tuning. A quantum dot around x = y = 0 nm and a sliding potential along x = 0 nm are formed. **(c)** Cut through the simulation along x = 0 nm. The line cut shows two tunnel barriers of approximately same height and width and the potential slide as intended. The figure also shows the simulated electron density in the device. (Simulation by Inga Seidler and Malte Neul, RWTH Aachen)

the electric field induced by the global TG is not screened by depletion gates and two reservoirs, which we will call source and drain, are formed. Directly underneath the dot and sliding gates the electric field from the TG is screened by the lower-lying metallic layer and we simulate no electron accumulation here.
A cut through the simulated potential along x = 0 nm is shown in Figure 5.3c. In the figure a 10 mV bias was applied to the drain reservoir, lowering its potential accordingly. The graph shows the simulated potential in brown, the electron density in red and as dashed black lines the Fermi energy in the source and drain reservoir. The brown potential forms a minimum in between two fairly symmetric tunnel barriers and declines monotonically towards the drain on the right-side of the figure. We also observe the intended spatial separation of sensor dot and drain reservoir. We simulate an electron density of multiple $10^{11}\ \frac{1}{\mathrm{cm}^2}$ in the reservoirs, a similar value as measured by typical Hall bar measurements in the previous chapter. The sensor dot potential minimum lies below the Fermi energy of the source reservoir and we expect the formation of a sensor dot with few electron occupation. The electron occupation is expected to be on the order of $\mathcal{O}(10^3\ \frac{1}{\mathrm{cm}^2})$ and hence does not appear in the simulated density here.

Robustness of the layout against fabricational defects

During the design development, we observed a crucial influence of the sliding gates on the course of the chemical potential. This observation is visualized in Figure 5.4a, which shows the chemical potential for 5 different sliding gate voltages. The main point of this simulation is, that the sliding gate voltages differ by only 10 mV, but the effect on the potential slide range from an almost complete lifting of the spatial drain separation for the green potential curve simulated for 530 mV to the formation of an opaque tunnel barrier in the simulation for 520 mV. We also observe, that reducing the sliding gate voltage entails the risk of lifting the monotonic sliding potential decrease, bringing the risk of the formation of additional electron dots in the sliding channel.

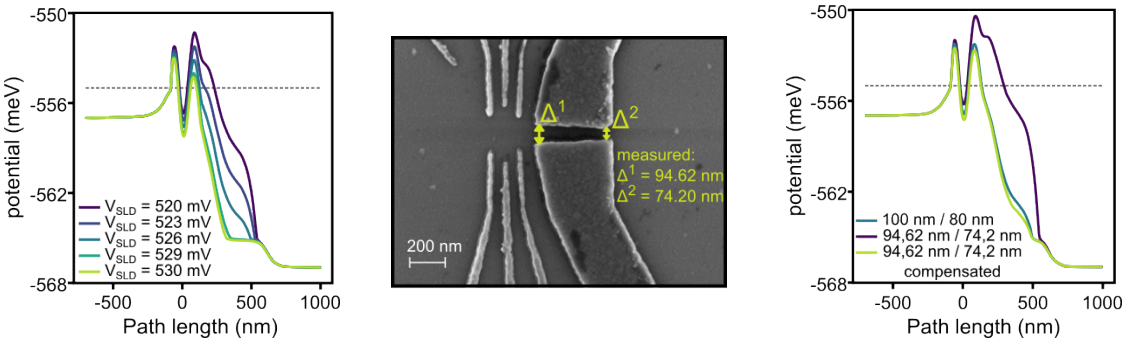


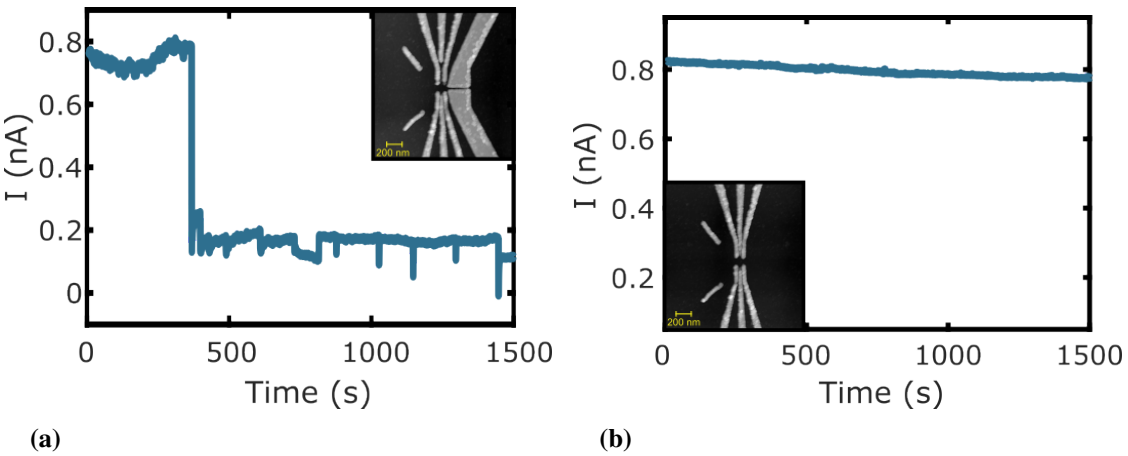
Figure 5.4: Sensitivity of the potential slide. **(a)** A slight variation of the sliding gate voltage by only ±5 mV alters the potential slide from a too opaque tunnel barrier to the lifting of the physical separation from sensor dot and reservoir. **(b)** SEM image of a fabricated device that has a slightly smaller gate separation than intended. **(c)** Adjusting slight fabricational imperfections by re-tuning of the electrostatic configuration. (Simulations in **(a)** and **(c)** by Malt Neul, RWTH Aachen)

Besides the applied voltage to the sliding gates, we also expect unavoidable fabricational defects to affect the sliding potential formation. Such imperfections may occur due to the lithography and lift-off processes during the metal structuring and differ from device to device. With the simulation we can test the robustness of the design against fabricational imperfections, without the need of many iterative fabrication and measurement cycles. To test to which degree such imperfections can be compensated by gate voltage tuning we consider the device shown in Figure 5.4b. For the shown device, the opening and closing width of the sliding gates are slightly shortened by about 5 nm compared to the desired values of 100/80 nm. Figure 5.4c shows the corresponding simulated potential for

the desired gate spacing of 100/80 nm in the blue curve and the potential for the same applied voltages but the slightly smaller slide gate separation of 94.62 nm and 74.2 nm in the purple graph. The purple potential clearly deviates from the desired blue potential as the tunnel barrier is significantly higher and thicker. We also observe, that the potential landscape can be re-tuned by respective gate voltage adjustments. We found that up to +-5 nm deviations can be compensated by gate voltage re-tuning, as shown by the light-green curve in Figure 5.4c, which matches the desired blue curve.
By simulating the ideas for the ASD prototype and feeding back first results from the fabrication process back into the simulation we now end up with a promising device layout. Only after these conception steps, we now perform transport measurements at cryogenic temperatures, presented in the following section.

5.2.1 Transport measurements at 360 mK

For the transport characterization of this device, we fabricated in total 6 samples and decided to fabricate the two larger sliding gates on four of these samples, while we omitted them for the remaining two. We could accumulate electrons and measure a current through all devices of this batch. However, we observed pivotal differences in the current stability, measured in our ^{3}He setup with base temperature of 360 mK. The fabrication was conducted by Dr. Floyd Schauer and details of the electron beam lithography are noted in his PhD thesis [81].
The current that we accumulated in the 4 devices featuring the sliding gate pair did not stabilize as expected after applying a positive voltage to the top gate. A typical course of the current through a prototype ASD device is shown in Figure 5.5a. The figure shows the current through the sensor in about the first half hour following the electron accumulation in the quantum well of the device. We observe multiple jumps in the current value and the current steadily decreased on that time scale. A further top gate voltage increase lead to a momentary higher current value, but the current did not stabilize in this manner and would vanishes eventually.
This time frame was too short for accurate tuning of Coulomb blockade and prevented the measurement of the AS factor, let alone its tuning. Leakage in between different gates or between Ohmic contacts and gates was experimentally excluded.
These current instabilities did not occur in the reference samples without large sliding gates, as shown as an example in Figure 5.5b. We conclude that the integration of the large metallic gates into the gate stack causes the instabilities. A possible explanation may be that in devices without sliding gates, a TG voltage of about 1 V suffices to accumulate a current through the device. In contrast, the sliding gates significantly screen any electric field of the TG and attenuate its electric field in the quantum well. Consequently, the samples with sliding gates required TG voltages exceeding 2.5 V for the electron



(a) **(b)**

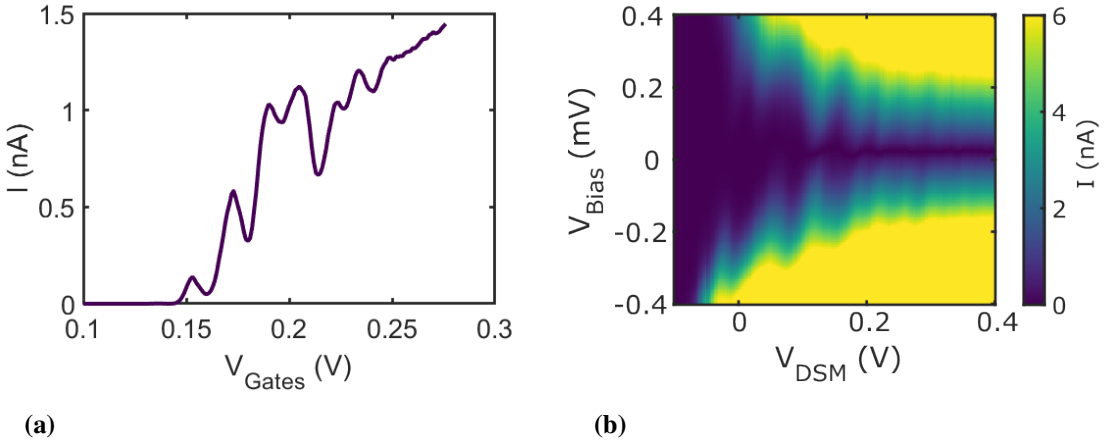
Figure 5.5: Instabilities of the current in transport measurements. **(a)** Devices featuring a sliding gate pair showed reproducibly current instabilities on a minute timescale, which could only be overcome by illumination of the samples. **(b)** Reference devices without sliding gates did not show current instabilities.

accumulation.
We can now draw a cross-reference to the Hall bar measurements in the previous chapter 4.1: In the Hall bar measurements we observed that increasing the gate voltage above a certain threshold would lead to trapping of charges at the semiconductor to oxide interface which would eventually lead to a continuous decline in the 2DEG electron density inside the quantum well. We now expect the same process in the ASD devices discussed here: The large gate voltage demand of devices containing the sliding gates also promotes trapping of charges in interface trap states, especially where not screened by the sliding gates.
We now utilized the strategy of illuminating the ASD devices that featured the sliding gates. Similar to Hall bar measurements, the 2DEG in the ASD samples following illumination with a red LED was tuned to just before the onset of electron accumulation in the quantum well. Slightly increasing the TG led to a measurable current through the devices. Most notably, we did not observe any abnormal current instabilities of the so-accumulated current.

5.2.2 Experimental proof of the ASD concept

For our ASD devices we observed that following illumination by a red LED, the current through the device remains stable for a complete cool-down cycle, allowing us to tune the ASD device. We put the device into operation by forming a single quantum dot,

shown in Figure 5.6a. The figure shows the measured current through the device as a function of the dot-defining gate voltages. We observe an oscillating behavior of the current, indicating the formation of a sensor dot with discrete energy levels according to its electron occupation. As we also sweep the gates controlling the tunnel barriers towards both reservoirs, the dot confinement is eventually lifted for gate voltages exceeding 200 mV and current through the device is no longer in Coulomb-blockade.



(a) **(b)**

Figure 5.6: Formation of a symmetric sensor quantum dot. **(a)** Coulomb oscillations indicating the formation of a single quantum dot. **(b)** Coulomb diamond measurement for a deactivated sliding gate configuration.

With the sensor dot formed, we focus on the potential slide. From the simulation results, we expect that the spatial separation of sensor dot and drain reservoir is deactivated by increasing the sliding gate voltages. So here we set the sliding gate voltages to a relatively large positive value of +50 mV and record a first Coulomb blockade measurement, shown in Figure 5.6b. The measurement shows the current through the device as a function of a single gate voltage (DSM) and the applied bias voltage. We observe rather symmetric and not-tilted diamonds in transport, indicating symmetric capacitances of the dot towards both reservoirs.
It is notable to recall at this point that the diamonds in the presented measurement are symmetric with respect to the bias axis. This observation is notable, as we applied the bias asymmetrically, like already sketched in Figure 5.2b: We only varied the potential at the drain reservoir while the source reservoir was held at ground potential, equivalent to 0 mV bias.

For the demonstration of the ASD working principle, we aim to activate the potential slide by reducing the sliding gate voltages and thereby spatially remove the drain from

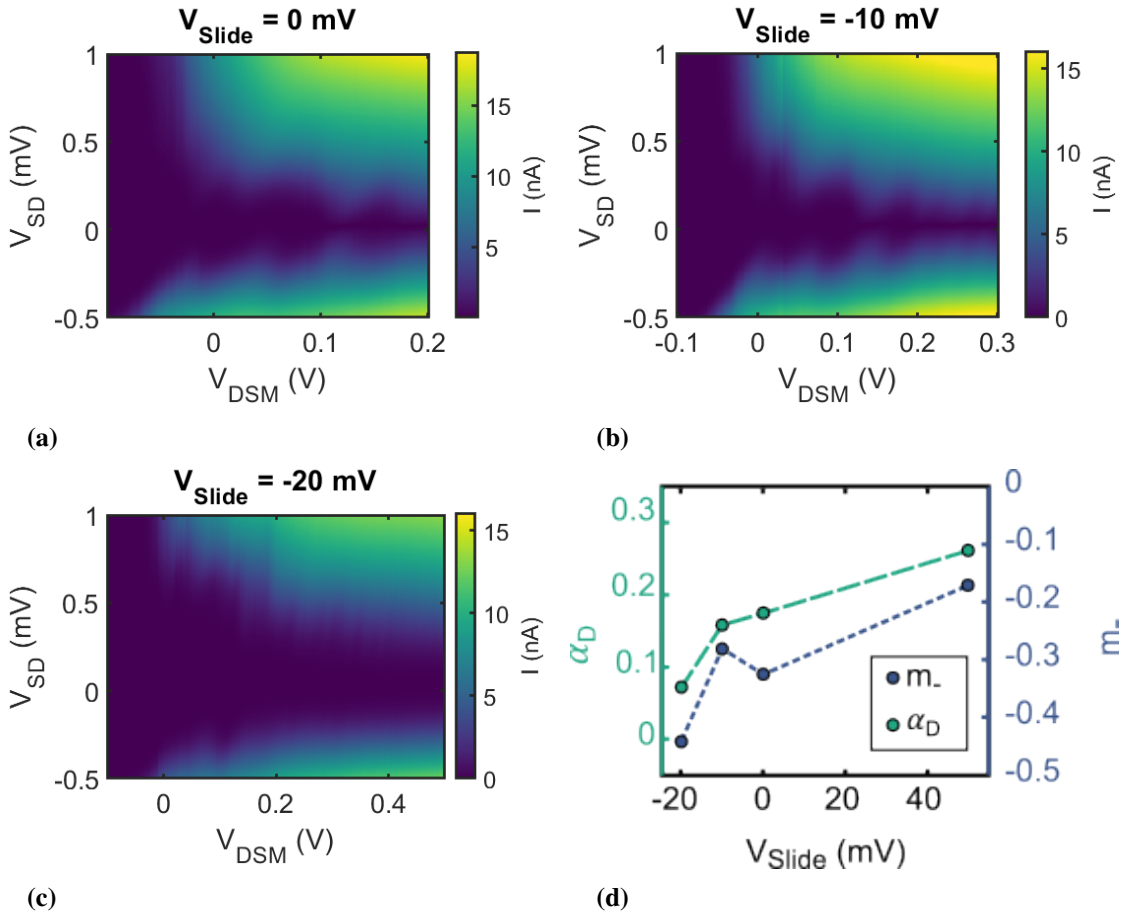


Figure 5.7: Activation of the potential slide. **(a)-(c)** Measurement series, varying the sliding gate voltage from +50 mV to -20 mV. For each gate voltage, a Coulomb diamond measurements is recorded and the slopes of the diamond edges are calculated. **(d)** Dependence of the drain lever arm α_D on the sliding gate voltage. The drain capacity can be reduced significantly by decreasing the sliding gate voltage.

the sensor dot. To maintain the tunnel barrier height and thickness, we compensate by adjusting the voltages on gates DNR and DNL where appropriate. Figures 5.7a-5.7c are Coulomb diamond measurements for which both sliding gate voltages are varied from V_{Slide} = +50 mV to -20 mV. The Coulomb diamonds in all three measurements differ from the reference measurement with deactivated sliding gates in Figure 5.6b. The diamonds tilt clockwise. The tilting becomes more pronounced the lower the sliding voltages are chosen. For the measurement with V_{Slide} = -20 mV diamonds are barely recognizable

and a non-conducting tube of close to 1 mV source-drain bias emerges.
To quantify changes in the drain lever arm α_D we extract the slopes m_+ and m_- from the graphs and calculate:

$$\alpha_D = \frac{|m_+|}{|m_+| + |m_-|} .$$

Figure 5.7d presents the extracted drain lever arms of this Coulomb diamond measurement series. We observe a clear decrease of the lever arm for decreasing the sliding gate voltages, which we interpret to be equivalent with a spatial separation of the sensor dot and drain reservoir. We observe a lever arm drop by a factor of 4.4. During the simulations a maximal tunability by a factor of 5.5 was predicted, which is set by device design, for example by the length of the sliding gates. For completeness, the graph also shows the variation of the slope m_-. The slope m_+ remained roughly constant during the tuning and is not shown here. We performed a complementary measurement series, which is not shown here, in which we held the potential of the drain reservoir, which we identify as the reservoir beyond the sliding gate pair, at a constant bias of 0 mV and varied the potential of the source Ohmic contact by applying a bias voltage. We did not observe any variation in the slopes of the diamond measurements within a sliding gate variation measurement series. Hence, we conclude that the tuning of the drain capacity that we measured in Figure 5.7d originates from a spatial separation of the reservoir from the sensor dot due to the presence of the potential slide, strengthening our concept of an asymmetric sensing protocol.

5.2.3 Interim conclusion

So far we have demonstrated the operational principle of the ASD concept and demonstrated that the capacity to the drain reservoir can be tuned as a function of the sliding gate voltages. We also observed a variation of the drain lever arm by a factor of 4.4, which is reasonably close to the simulated factor of 5.5.
During the measurement there have been some challenges that we will tackle in the upcoming section:

- The large metallic gates caused a collapse of the current through the device on a timescale of a few minutes, too short for a proper tuning of Coulomb blockade in the sample. We could overcome this instability by illuminating the sample what allowed stable measurements for days. We also assume that the large metallic sliding gates promote the formation of charge traps at the oxide to semiconductor interface. We expect these charge traps to cause the current collapse via screening of the electrical field from the topgate.
  For the upcoming devices we intend to improve the oxide and interface quality, but

also try to avoid large metallic gates whenever possible. This may also help in the device fabrication during which the pure size poses a challenge for the electron beam lithography due to the proximity effect.

- The presented device features only a single global topgate. This suffices for controlling the electron density in the device, but does not allow a proper tuning of it, for example allowing for different densities in different sections of the device or to properly compensate the screening of the lower lying metal gate layer. To improve the device tunability we strive to implement a larger degree of freedom in the device tuning by introducing more accumulation gates to the sample.

- The measured diamonds all appear very blurry and the edge detection becomes quite handy. We expect a large electron temperature to cause this blurring of the diamond edges. Though measured at a base temperature of about 320 mK, the electron temperature in the measurement may be higher, resulting from the electrical connection of the device to room temperature equipment. For this specific measurement series we used coaxial-type measurement lines from room temperature to the sample. These have the advantage of shielding the signal from disturbing electrical fields, but thermalization of the inner conductor is tricky and may have not been done properly for this measurement series. The electron temperature can be estimated from the width of the Coulomb diamonds. A thorough electron temperature analysis using this technique on a different sample in the dilution cryostat is given in A.3.1. For this ASD measurement series we expect an electron temperature exceeding 1 Kelvin. For the next measurements we will rebuild our measurement rod and implement a twisted-pair loom wire to replace the coaxial measurement lines.

- Obviously, the gate layout presented here, only allows for the formation of a single sensor dot. For the next device generation we intend to allow the formation of an adjacent, capacitively coupled double qubit dot system.

5.3 2nd generation ASD device

Following the successful demonstration of the ASD concept we now introduce a reworked device that tackles the disadvantages of the demonstrator prototype of the previous chapter. We aim for decreasing the drain capacity further while also enabling the formation of two qubit dots in the vicinity of the asymmetric sensor dot.

5.3.1 Layout considerations and simulations

A major change to the design we want to implement is to avoid large TG voltages for the electron accumulation in between the two larger sliding gates. As shown in blue false-color in the SEM image of the new device type in Figure 5.8a, we add a third gate in between the two large sliding gates. This third gate is positioned directly above the potential slide and hence its electric field is not screened by the two larger sliding gates. This additional gate allows better tunability of the electron density across the device and lifts the demand of large TG voltages. In this new design, we also extend the sliding region from about 400 nm to 1000 nm, inducing a larger asymmetry.
The figure also shows three green colored gates intended to confine the sensor quantum dot. The outer two form tunnel barriers towards source and drain reservoir while the middle one serves as a plunger gate. Additionally, the device features six yellow colored gates in vicinity of the eventual sensor quantum dot. These six gates can be used to electrostatically define a double quantum dot system. The SEM image does not show the global TG layer which is electrically isolated by a 50 nm thick Al_2O_x oxide layer.
In analogy to the first generation ASD prototype, we supported the device conception by iterative potential and electron density simulation cycles, performed at the RWTH Aachen University under guidance of Dr. Lars Schreiber. Line cuts for the simulated potential and electron density of the final gate geometry are plotted in Figure 5.8b and 5.8c, along a path through the potential slide and through the double dot area, respectively.
For the cut shown in Figure 5.8b a bias voltage of 10 mV is applied to the drain reservoir. Two tunneling barriers of equal height and width are formed to confine the sensor dot and the potential slide declines monotonically towards the drain reservoir, reducing the probability of disruptive quantum dot formation along this channel. We also observe a physical separation of sensor dot and drain reservoir of about 1000 nm as intended. In the simulations, a AS factor of 195 is predicted in this layout. The cut through the double dot section in Figure 5.8c shows two potential minima for the formation of (qubit) quantum dots.
From simulating the potential for different gate voltages, we observed that due to the elongated slide, the risk of forming serial quantum dots inside the potential slide increases. While gate width and pitch deviations can be compensated by the additional middle gate above the sliding channel, the simulation predicts the gate edge roughness along the 1 µm long channel to pose one of the biggest challenges in tuning the device while avoiding the trapping of electrons along the potential slide. The edge roughness cannot be totally suppressed within our lithography and metal lift-off process. To estimate the consequences and the limitations of this new gate design, we outline the gate shape of a sample fabricated at the RWTH Aachen University, shown in Figure 5.9a, and simulate the potential and electron density based on the gate outline in Figure 5.9b. The simulation

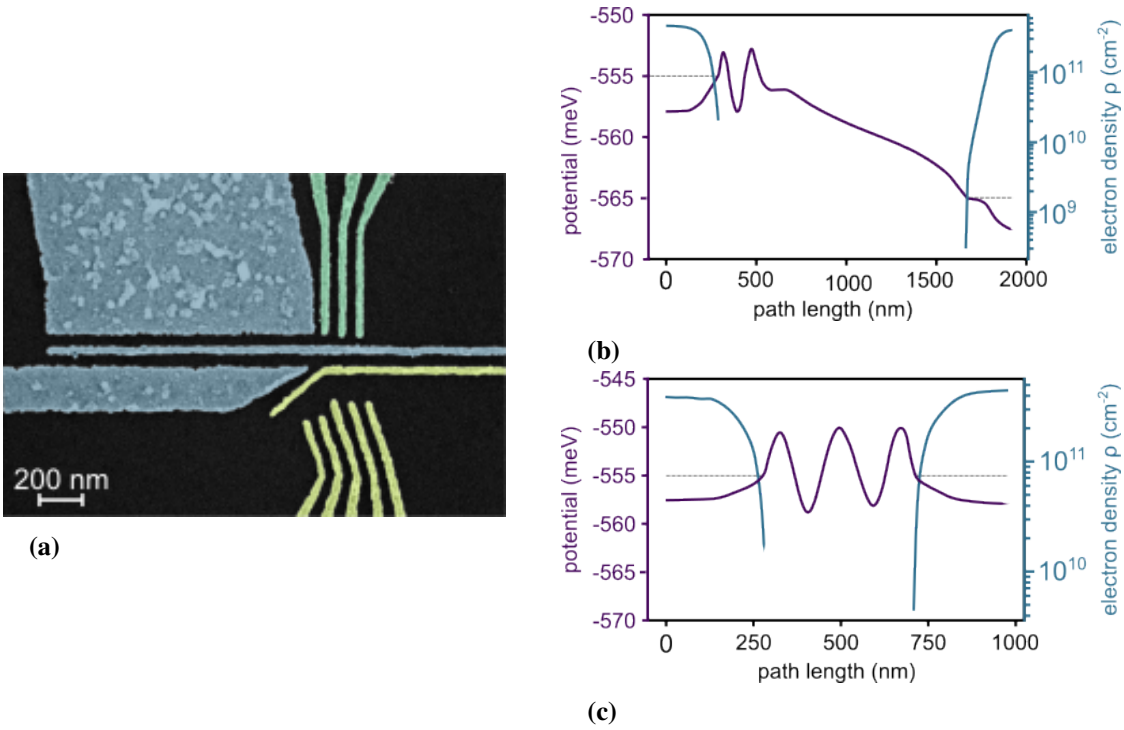


Figure 5.8: Reworked ASD gate layout. **(a)** False-colored SEM image. A second global TG layer is not shown here. **(b),(c)** Potential and density simulations along a path through the potential slide and the double dot (qubit) area of the device. (Simulations in **(b)** and **(c)** by Inga Seidler and Malte Neul, RWTH Aachen)

was conducted by Inga Seidler and Malte Neul. We observe the formation of multiple local potential minima along the potential slide. As a result from the simulation we observed that by appropriate re-tuning of the gate voltages, the potential slid can still be adjusted. We observed no fabricational improvement of the gate edge roughness following a vacuum anneal of the device at 400 °C.
We also analyzed interface defects, which had caused current instabilities in the prototype devices when charged through the quantum well and subsequently screened the gate voltage induced electric fields. By comparing room temperature CV measurements performed by Jan Klos at the RWTH Aachen University on oxide layers from four different ALD machines from four different clean room sites we observed roughly the same defect density of the order of $10^{11}\ \frac{1}{\mathrm{cm}^2}$ in all measurements. The effects of such interface defect states on the potential slide of the new device layout are shown in Figure 5.9c. A random distribution according to a density of $10^{11}\ \frac{1}{\mathrm{cm}^2}$ was integrated into the simulation, which was performed at the RWTH Aachen University. The effects on the functionality of

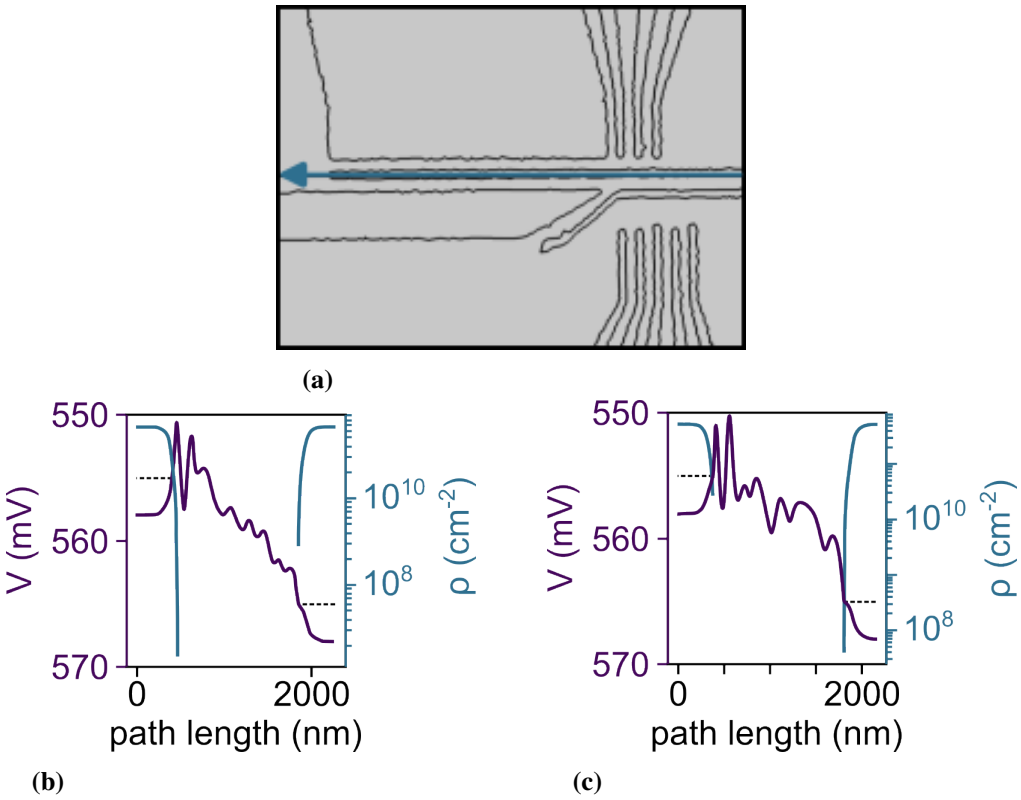


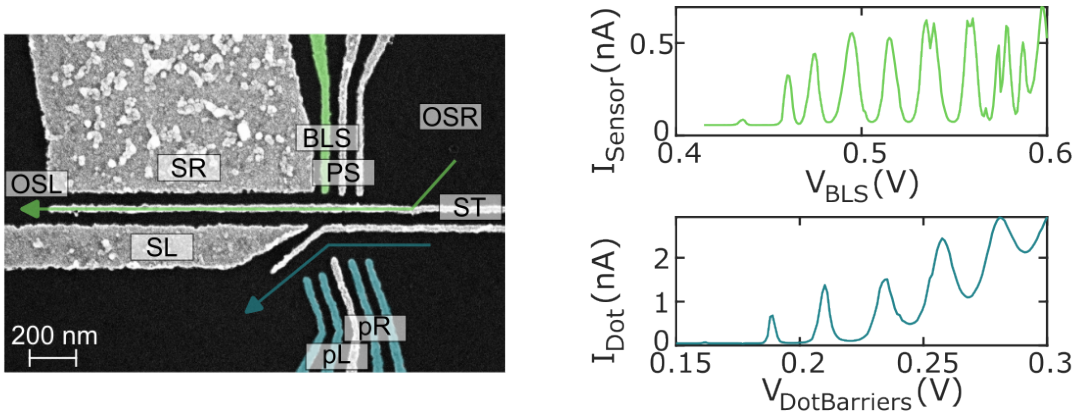
Figure 5.9: Disturbance of the potential slide through fabricational imperfections. **(a)** Outline of the metallic gates of a typical device. **(b)** Impact of the line-edge roughness on the potential slide. **(c)** Potential simulation considering interface trap states. (Simulations in **(b)** and **(c)** by Inga Seidler and Malte Neul, RWTH Aachen)

the ASD device can hardly be predicted due to the random distribution of defects. In any case, tuning of the potential slide will be more challenging compared to the shorter prototype ASD. A suppression of the defect density may be achieved by reducing the oxide thickness, especially of the lowest lying layer [109].

5.3.2 Device tuning and constant voltage bias charge sensing

First transport measurements of 2nd generation ASD devices at the University of Regensburg turned out challenging because leakage current emerged in 3/3 measured devices from TG voltages of about 800 mV on, right after the onset of charge carrier accumulation

inside the quantum well. We cannot exclude a bad ALD oxide quality for this fabrication run. Also we may have limited ourselves by too thin isolation layers with a thickness of 10+50 nm for this gate layout. We nevertheless were able to conduct transport measurements at a base temperature of 360 mK by biased cool-down of the devices, as introduced on Hall bar devices in section 4.2.2. By means of the biased cooling we could shift the turn-on of the electron accumulation to lower gate voltages, most importantly lower than the leakage current breakthrough voltage.

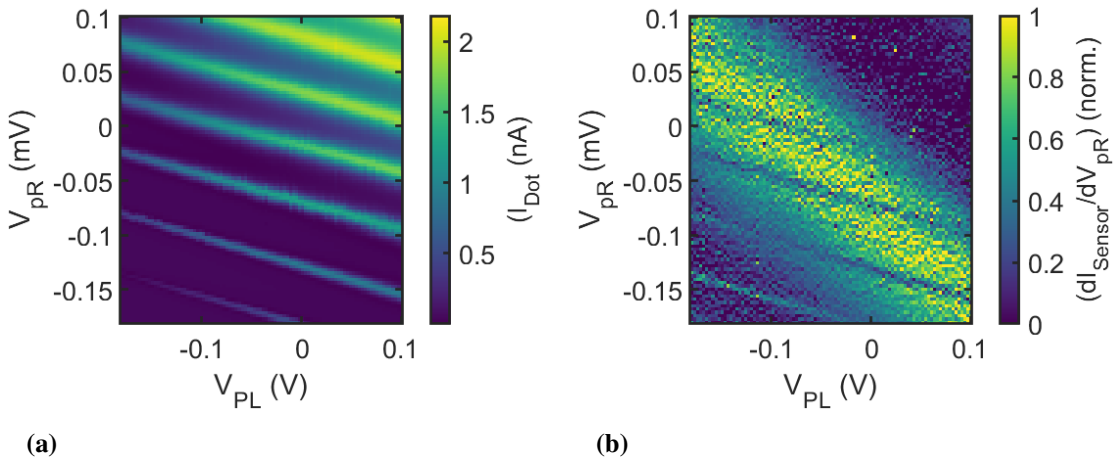


(a) **(b)**

Figure 5.10: Current accumulation and quantum dot formation. **(a)** False-colored SEM image of the measured device. **(b,Top)** Current measurement along the path through the sensor dot. The graph shows the formation of a single sensor dot for voltages below 500 mV. For higher voltages, a second dot forms in parallel to the first dot. **(b,Bottom)** Current through the double-dot area of the device. A single dot forms as indicated by the Coulomb blockade oscillations.

Following the biased cool-down, all tested devices appeared extremely stable, without slow or sudden recharging events for weeks. Also no illumination of the samples was required. We demonstrate electron accumulation as well as the formation of quantum dots in Figure 5.10. Subfigure 5.10a shows the SEM image of the device, highlighting the two current paths through the device: The green arrow indicates the sensor current, while the blue arrow marks the current path through the qubit dot section of the device. The top graph in Figure 5.10b shows the sensor current as a function of the left sensor barrier gate BLS for deactivated sliding gates, which is a configuration for which we do not expect spatial separation of sensor dot and drain reservoir. The current oscillates, indicating the formation of discrete energy levels inside a quantum dot. For voltages exceeding 500 mV we observe a beating pattern in the current hinting at the formation of

a second, parallel quantum dot, which we will deplete for all following measurements. From complementary measurements we can conclude that the remaining single sensor dot is located under the long ST gate, right in between BLS and PS, slightly shifted towards the sliding gates compared to the ideal simulation. The second faulty quantum dot may form right under the BLS gate.



(a) **(b)**

Figure 5.11: Constant voltage bias charge sensing. **(a)** Current measurement through the (qubit) quantum dot. **(b)** Derivative of the current measurement through the sensor quantum dot. A single Coulomb oscillation of the sensor dot is visible on the diagonal through the graph. We also observe the same charging lines as in subfigure **(a)**.

The lower panel of Figure 5.10b shows the current through the qubit-dot section of the device. We observe an oscillating behavior of a single quantum dot. By sweeping all outer gates, we intend to form a single large quantum dot in between pL and pR, right where the blue arrow bends in the corresponding SEM image. As we sweep all outer gates, we open the tunnel barrier for voltages above 250 mV and the Coulomb blockade does not pinch off the current completely any longer.
Next, we test the general charge sensing capability of the device by recording the charge stability diagram of the qubit-like quantum dot by gates pL and pR, shown in Figure 5.11a. We observe the same Coulomb blockade peaks as measured in the single-gate sweep from the previous measurement 5.10b. These peaks appear as lines in this measurement as a function of two gate voltages.
For testing the charge sensing capability of the layout, we tune the sensor in the conventional constant voltage bias method to a sensitive configuration and simultaneously record the current through the sensor dot. The resulting derivative of the sensor current is shown

in Figure 5.11b. The measurement shows a prominent thick line from the top left to the bottom right corner of the graph. This is a Coulomb blockade peak in the sensor dot. Additionally, the graph shows identical lines of the qubit-like dot charging, measured here via constant voltage bias charge sensing. So we can conclude that in general the device allows charge sensing of a qubit-like dot with the sensor.

5.3.3 Tuning of the sensor asymmetry

Having demonstrated constant voltage bias charge sensing we next characterize the tuning capability of the drain capacitance with the aim of demonstrating a large asymmetry factor. Therefore, we activate the potential slide by decreasing the voltage on the sliding gate SR. We avoid changing the second sliding gate voltage on gate SL as we observed that SL does quickly pinch off the sensor current completely such that no operational window remains for tuning the potential slide. This behavior may result for example from device-specific fabricational imperfections.
We measure the potential slide activation by recording a series of Coulomb diamonds as a function of the drain bias and the sensor dot plunger gate PS. In between consecutive measurements we step-wise decrease the slide potential V_{SR} and compensate effects on the tunneling barrier that separates sensor dot and drain reservoir by increasing V_{BSL}. The measurement series is shown in Figure 5.12. The figure shows three Coulomb diamond measurements as well as a graph of the AS factor as a function of the sliding gate voltage. The Coulomb diamonds in Figure 5.12a for the largest V_{SR} = 0.34 V appear very symmetric. The figure shows two and one half diamonds. In this configuration we call the sliding gates deactivated. For PS voltages larger than 0.4 V, the tunnel barriers are strongly affected by the sensor plunger gate and no clear Coulomb blockade is formed any longer. Contrary, for voltages lower than 0.3 V the barriers become very opaque and a large bias voltage is required to overcome the tunnel barrier at all.
Decreasing the voltage applied to the sliding gate SR totally changes the Coulomb diamond shapes in Figures 5.12b and 5.12c, for V_{SR} = 0.24 V and V_{SR} = 0.215 V, respectively. The diamonds appear no longer symmetric but largely asymmetric with respect to the source-drain bias. Also a non-conducting tube appears for low bias voltage which will be discussed in section 5.3.5.
The figure of merit for our concept is the steepness of the negative Coulomb diamond edges. This slope is proportional to the voltage swing ΔV_{bias} required to compensate a given potential change after the (un-)loading of a proximal qubit quantum dot when operated at a constant current. This voltage swing constitutes our measurement signal.
To compare the different voltage configurations, we now calculate the asymmetry factor by linearly fitting the constant current edges of the Coulomb diamonds in both positive and negative direction. We observe, that the positive slope m_+ barely changes as a function

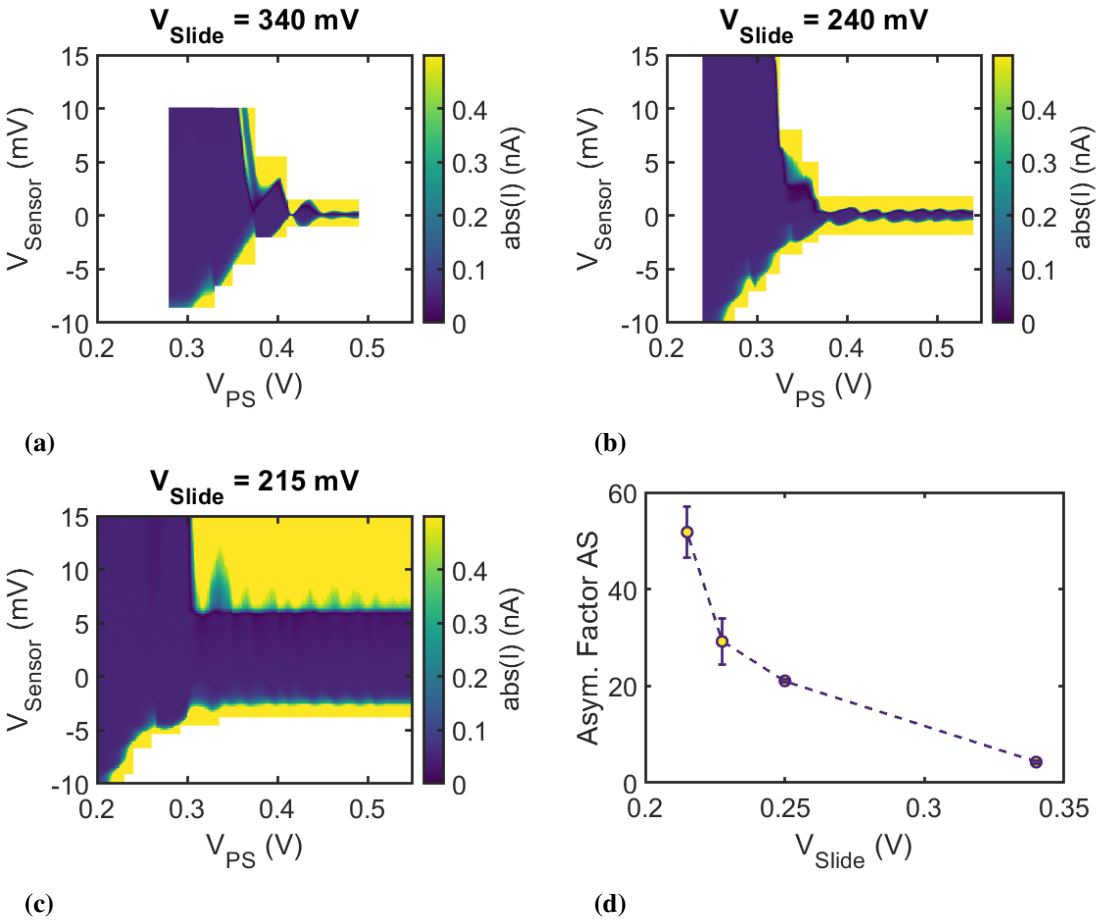


Figure 5.12: Slide gate variation. **(a)-(c)** Coulomb diamond measurements for different sliding gate voltages SR. **(d)** Extracted asymmetry factor AS from the slopes of the Coulomb diamond measurements.

of V_{SR} while m_- significantly increases with decreasing V_{SR}. The evaluation of $AS(V_{SR})$ is shown in Figure 5.12d using the same m_+ slope for all AS calculations. We observe that the variation of the Coulomb diamond shape also reflects in a strong increase of the AS factor. While for the deactivated slide the ratio amounts to $AS = \frac{m_-}{m_+} = 4.3\ (\pm\ 0.23)$ it increases to 51.8 ($\pm$ 5.3) for the lowest SR voltage measured here. The extracted AS value of this second proof-of-concept measurement exceeds the value of the first demonstrator device by more than an order of magnitude, presumably due to the elongated slide.
We also observe that the error bar increases for lower SR voltages. The large error bar stems from a limited voltage resolution in the PS gate voltage of $\Delta V_{PS} = 1$ mV, while for the bias we have a resolution as low as $\Delta V_{Bias} = 0.3$ µV. Consequently, we can fit

along only very few PS gate voltages for the steepest diamonds, leading to the significant increase of the error bar.

5.3.4 Makima fit

To demonstrate this evaluation challenge, Figure 5.13 shows three graphs, each extracting the PS voltage whenever the current exceeds a chosen threshold of 50 pA along the negative slope of the respective Coulomb diamond edge from measurements 5.12a and 5.12c.
Figure 5.13a shows the slope extraction for the most symmetric measurement of V_{SR} = 340 mV. Fitting with a least-squares routine can map the data set with low error bar and results in m_- = -0.645 (± 0.013).
This changes drastically for the most asymmetric Coulomb diamond measurement (V_{SR} = 215 mV) in Figures 5.13b and 5.13c. In Figure 5.13b we again extracted the PS voltage for the first exceeding of the current threshold of 50 pA. We observe a clustering to only two PS voltages due to the extreme steepness of the diamonds and the limited resolution of the gate voltage. The least squares fit gives a value of m_- = -2.5 (± 2.1) with extremely large error bar. This could be a significant underestimation when fitting only through two data points.
As we are not limited in the bias voltage resolution, we can significantly reduce the error bar in the AS value evaluation by an interpolation of the data: For each V_{Bias} value we interpolate the data by a modified Akima algorithm [110, 111] along the V_{PS} axis.
The resulting threshold crossing analysis of the interpolated data set for the lowest SR gate voltage is shown in Figure 5.13c. The linear least squares fit gives a value of m_- = 7.82 (± 0.53) with much reduced error bar and indeed exceeds the simplest fit by a factor of almost 3. We did not observe a significant variation in the AS calculation for the symmetric diamond or to m_+ by interpolating the data.

In analogy to the first slide gate variation measurement series on the prototype devices, we also need to exclude effects of the asymmetric bias application on the tilting of the Coulomb diamonds. A complementary measurement series of Coulomb diamonds for different SR gate voltages but varying the source and not the drain bias voltage to exclude such effects is shown in the appendix of this thesis in A.2.1. The presented data confirm that the variation in the AS value stems from the activation of the potential slide and the separation of sensor dot and drain reservoir.

Second slide gate variation with improved gate resolution

To conclude the slide gate study, we present a second slide gate variation measurement, recorded with a modified measurement setup, adding the passive voltage adder described

in section 3.3.3. This component improves the voltage resolution on the PS gate to $\Delta V_{PS} = 6\ \mu V$. This improved sliding gate variation is shown in Figure 5.14. The figure shows Coulomb diamond measurements recorded for three different sliding gate voltages. The measurement series starts with a deactivated potential slide in 5.14a for a SR voltage of 470 mV and the most asymmetric diamonds are recorded for a SR voltage of 382 mV in 5.14c. In this last measurement for the lowest sliding gate voltage the Coulomb diamond shape has changed to that extent that the diamond form is barely visible any

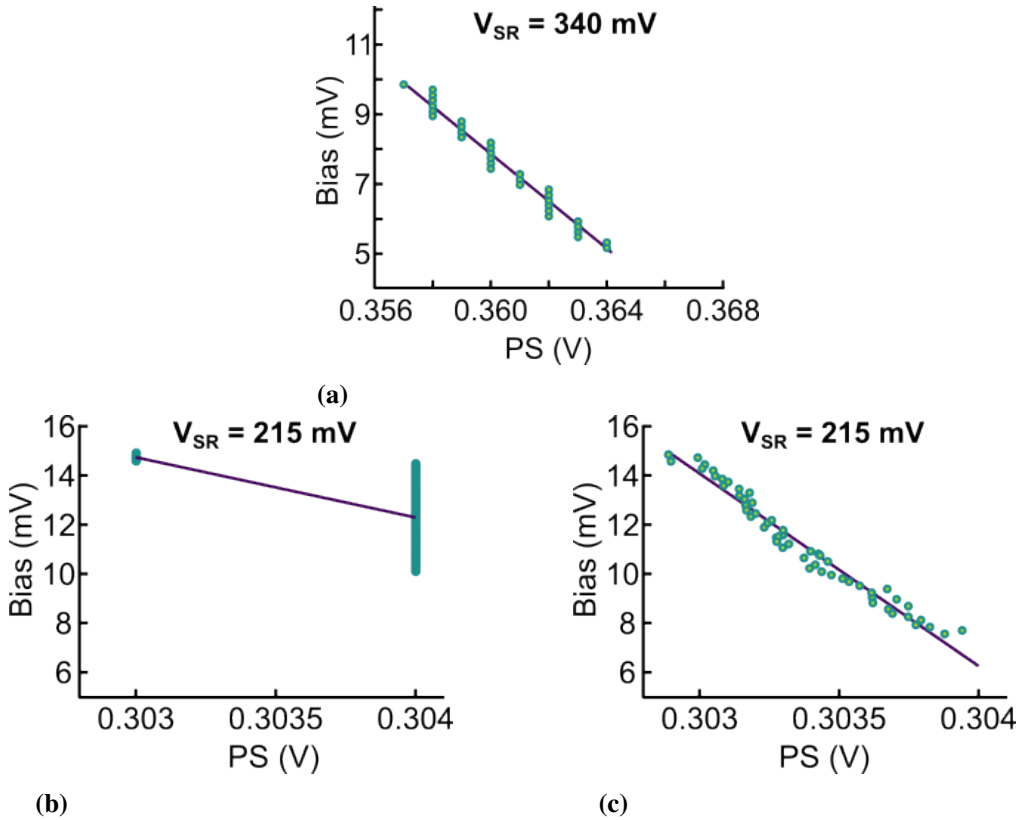


Figure 5.13: Extraction of the PS voltage along the m_ slope when crossing a threshold of 50 pA. **(a)** For the most-symmetric diamond measurement a least squared fit is reasonably accurate. **(b)** For the steepest diamond measurement the slope is as large and the PS gate voltage resolution so low such that the threshold crossing occurs at only two different voltage values, leaving a least squared fit with an enormous error bar. **(c)** Performing an interpolation of the data following a MAKIMA approach artificially increases the gate resolution, thereby very much reducing the error bar of the slope extraction.

longer. This does not pose a problem for the readout, which requires only a steep slope. For the slope evaluation and the extraction of the AS value, a MAKIMA interpolation was

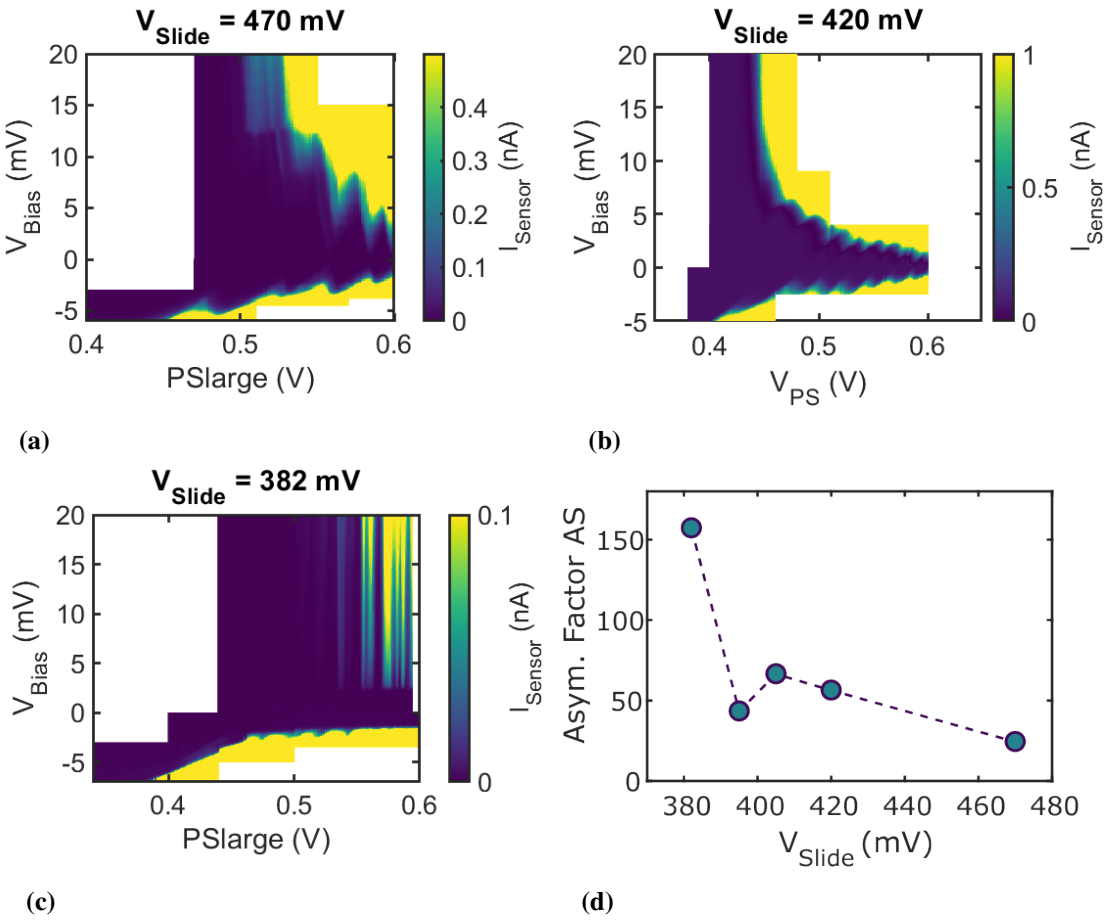


Figure 5.14: Second sliding gate variation with improved gate voltage resolution. (a)-(c) Coulomb diamond measurements for different sliding gate voltages. **(d)** Extraction of the AS value as a function of the sliding gate voltage.

no longer required due to the physically improved resolution on the PS gate. The result of the AS evaluation is shown in Figure 5.14d. We observe an increase of the AS value as before, however here the highest AS value is as large as 175, close to the predicted value of 195 from the simulations.

5.3.5 Current gap at positive bias

Notably, all three presented sliding gate variation measurement series in this chapter have in common that a blockade gap forms for a positive voltage bias after activating the sliding gates. This non-conducting gap becomes as large as 5 mV. No similar observation has been reported in symmetric sensor dots in the community where typical sensor bias voltages do not exceed 1 mV.
We explain this feature by two effects: On the one hand, potential disorder along the potential slide might add to the intended potential barrier under the BLS gate. On the other hand, we have observed that the sensor drain bias also enhances the steepness of the potential slide. Only for a large enough drain bias in turn this disorder potential can be overcome, leaving only the intended tunnel barrier underneath gate BLS.

5.4 Constant current charge sensing

Finally, we want to discuss the constant current charge sensing according to our concept. We also aim to make use of the increased steepness of the Coulomb diamonds. Our silicon-based sample suffered an electrostatic discharge (ESD) damage during the attempt to unplug the current amplifier and to replace it by a constant current source device.
Therefore, for the demonstration of constant current charge sensing with an ASD sensor we refer to complementary measurements performed during the same time span at the RWTH Aachen University by Eugen Kammerloher on a GaAs-based qubit device. All measurements that will be discussed here are also pre-published in our research paper [87]. Figure 5.15a shows the gate layout of the GaAs sample, details on the heterostructure and on the fabrication can be found in the above reference. Similar to our silicon-based samples, the device features a sensor part towards the bottom right of the image which is highlighted by the yellow and orange colored gates and a qubit dot section in the top left corner, defined by the purple colored gates. The sample shows many similarities with the device fabricated on the silicon heterostructure: Along the sensor current path (dashed line), the three orange colored gates are intended to form the potential slide towards the drain reservoir while the three yellow colored gates form tunnel barriers for the sensor dot towards both reservoirs and serve as plunger gates for tuning the chemical potential of the sensor dot levels.
The sensor dot can be tuned symmetrically by deactivating the potential slide. The corresponding Coulomb diamond measurement is shown in Figure 5.15b. By decreasing the sliding gate voltages we can activate the potential slide as demonstrated by the Coulomb diamond measurement in 5.15c. Figure 5.15c appears remarkably similar to the activated Coulomb diamond measurement in Figure 5.14c in the silicon sample of the

previous section.

In the GaAs sample we observe a decrease in the drain capacity by a factor of 13 when activating the potential slide.
We tune the adjacent double dot system to form two quantum dots, highlighted as white circles at the tips of gates RFA and RFB. Figure 5.15d shows a charge stability diagram of this double dot system recorded in the constant current measurement mode by the asymmetric sensor dot. Four different electron occupations of the upper and lower quantum dot can clearly be distinguished. The corresponding occupation is indicated by the numbers in brackets. A line cut through the (n-1,m) to (n,m-1) transition, across the inter-dot transition, is shown in Figure 5.15e, showing a voltage swing of 3 mV, an order of magnitude larger than expected for a symmetric sensor dot.

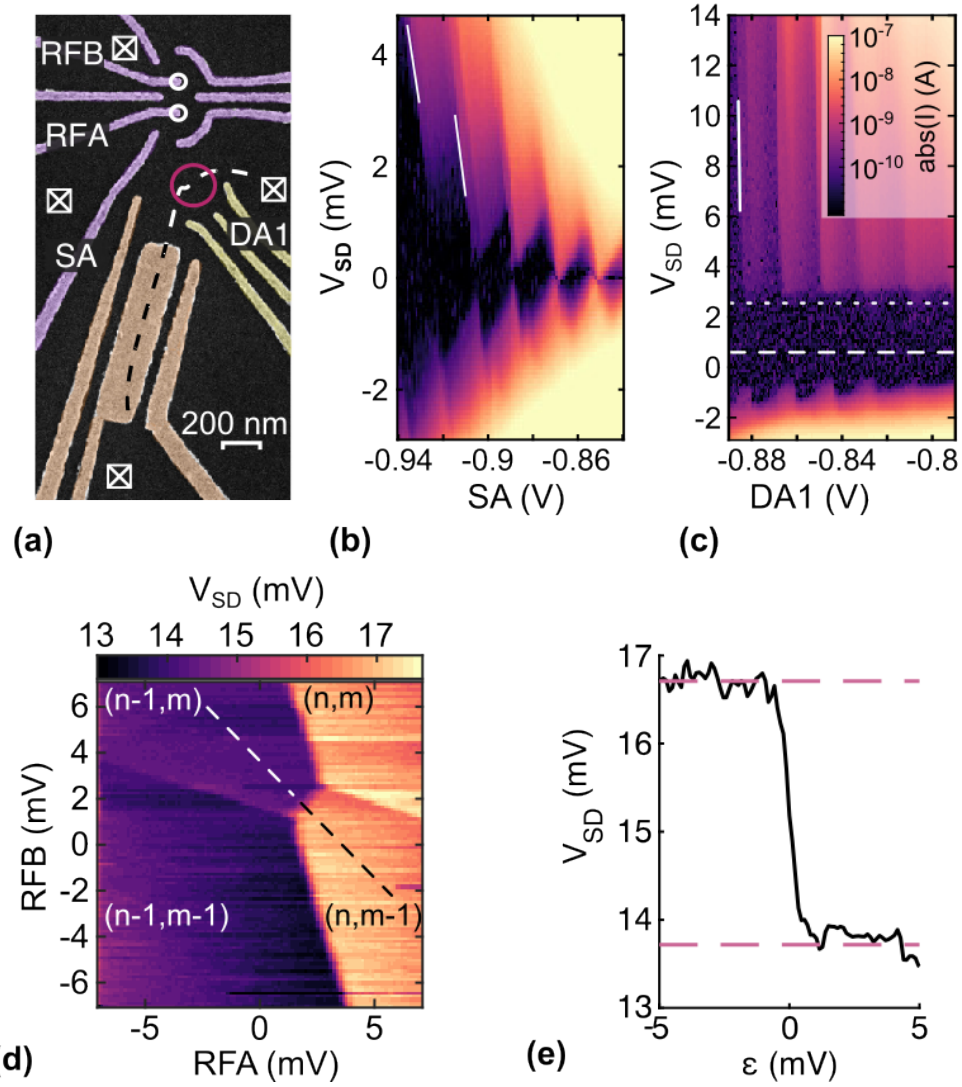


Figure 5.15: Charge readout by an ASD sensor. **(a)** False-colored SEM image of the GaAs-based device. **(b)-(c)** Symmetrically and asymmetrically tuned Coulomb diamond measurements. The drain capacity is tuned by the sliding gates by a factor of 13. **(d)** Charge stability diagram of the capacitively coupled double-dot system. **(e)** Line-cut across the interdot transition showing a voltage swing of 3 mV. The measurement was conducted by Eugen Kammerloher.

5.5 Conclusion

We introduced a new concept of reading out the charging state of a qubit system by a constant-current driven SET for which we developed a metal gate layout allowing us to capacitively tune the dot's capacity to the drain reservoir. We achieved this reduction of the drain capacity by spatially separating the drain reservoir from the sensor dot while keeping the tunnel barriers and the dot confinement unchanged. We derived an inverse proportionality of this capacity on the sensor's output swing. This increase in the output swing renders the use of low-power-consuming pre-amplifiers at cryogenic temperatures possible.
By simulation we could design a sample layout and calculate the expected electron density and chemical potential with much reduced turnaround time compared to full fabrication and measurement cycle times. We designed and fabricated an ASD device on a Si/SiGe heterostructure for which we could demonstrate constant voltage bias charge sensing of a proximal quantum dot and for which we could electrostatically tune the asymmetry factor AS by almost an order of magnitude to a value of AS = 175, close to the simulated value of 195. In a complementary measurement by our collaboration partner during the same period on a GaAs based ASD device, constant-current charge sensing for an activated sliding potential configuration was demonstrated, measuring an increase in the sensor output swing also by an order of magnitude. These results make the ASD a promising readout candidate for scaling of semiconductor-based spin qubit architectures by using low power-consuming pre-amplifiers like a HEMT or HBT at cryogenic temperatures in proximity to the qubit device.
For the next steps we have to improve our oxide quality to avoid both leakage currents and sudden recharges at the oxide to semiconductor interface to prevent possible collapses of the current through the device. This may also avoid the necessity of biased cool-down or illuminating the sample.
The discussion of the back-action of the sensor, which is now operated with a bias voltage of up to 10 mV is still pending. We mentioned this detail already in the concept section of this chapter. We also performed complementary measurements in a working device at the RWTH Aachen University, as the test requires a working qubit for which the spin can be manipulated and read out. First measurements of the back-action effect are very promising up to a bias voltage of 1.5 mV, for which we did not observe any back-action on the qubit. These results are presented in the appendix in A.2.2.

6

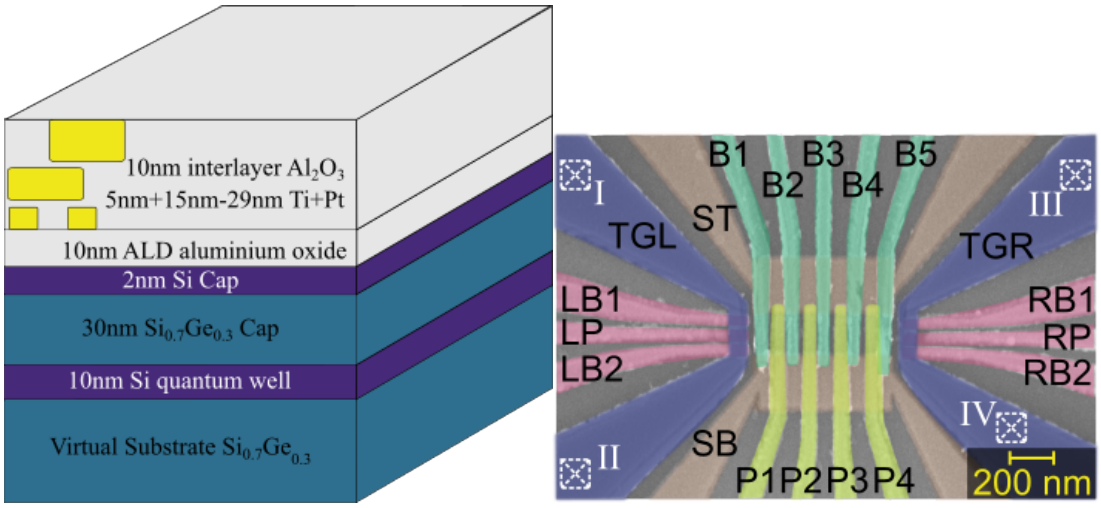
Spin qubit device (Qubus)

At the time of the beginning of this PhD project very promising results for one [5] and two-qubit gates [4] in silicon-germanium spin qubit devices were published. Both of these exemplary referenced state-of-the-art studies presented measurements of spin qubit devices, fabricated on a silicon/silicon-germanium quantum well heterostructure and used a depletion architecture metal gate stack. The qubit dots in both these devices were tunnel coupled directly to the 2DEG, that was accumulated within the quantum well and which allowed loading and unloading the qubits, but also the readout of the qubit state via spin dependent tunneling.
At the same time a device with similar design hosting a single qubit dot that was also tunnel coupled directly to the 2DEG as electron reservoir was measured in the cooperation of the University of Regensburg and the RWTH Aachen University. In these measurements, which were conducted at the RWTH Aachen, we demonstrated spin manipulation with state-of-the-art T_2^* time [59]. The device heterostructure was MBE grown and showed the largest valley splitting to date [58]. Simultaneously, Coulomb blockade measurements performed solely at the University of Regensburg also demonstrated pioneering experiments like the control of the last electron in a ^{28}Si/SiGe heterostructure device for spin qubit application, but so far without single-shot electron control [88, 112, 113].
All of the referenced devices here have in common that the qubit dot(s) were defined via the depletion-type architecture (see concepts section 3.1.3), were loaded via a two-dimensional electron reservoir and the spin readout was performed via spin-dependent tunneling to this 2DEG reservoir [84].
Recently, a second gate architecture started to become more popular: The accumulation-

type [114, 115], which may allow a better electrostatic control as well as a more compact device design. Some of such new generation devices are now designed to use a sensor dot as electron reservoir for the qubit dots instead of directly the 2DEG [115, 116].
In this section, we present measurements on an accumulation-type device that was fabricated at the RWTH Aachen University by Ran Xue from the group of Dr. Schreiber at the chair of Prof. Dr. Bluhm. This device is also designed to use a sensor dot as electron reservoir for four serial qubit dots. While the device was designed with the intention of electron shuttling along the linear qubit chain [116], we want to perform single-shot spin readout of that device. While such single-shot spin readout has been demonstrated in devices with the sensor dot acting as electron reservoir using Pauli spin blockade (PSB) for the spin-to-charge conversion [114], we perform such spin readout measurements with the aim of analyzing the readout fidelity of an Elzerman-type spin-to-charge conversion by electron tunneling to the sensor dot instead of tunneling to a 2DEG reservoir [84]. We want to investigate whether a spin relaxation constant T_1 can be determined and whether a valley splitting can be measured. A second aim of the intended study is the setup of a new dilution cryostat at our university for which single-shot spin readout would be one of the validation aims, as no single-shot spin readout has been performed before at our university.

6.1 Device initialization and tuning

We perform this study in a device built upon a commercial Si/SiGe heterostructure from Lawrence semiconductors custom-produced for the group of Dr. Schreiber at the RWTH Aachen (S4840R/S39). A sketch of the heterostructure is shown in Figure 6.1a. The undoped Si/SiGe heterostructure features a $Si_{0.7}Ge_{0.3}$ virtual substrate which is followed by a 10 nm thick strained natural Si quantum well 30 nm below a 2 nm thick Si cap to prevent oxidation. Electrons are accumulated in the quantum well by Ti/Pt metallic gates, fabricated by electron beam lithography. The gate stack consists of three layers of metallic gates separated from the Si cap and from each other by consecutive 10 nm ALD deposited Al_2O_x. Each metallic gate has 5 nm Ti as adhesive material, followed by an increasing Pt thickness ranging from 15 to 22 to 29 nm thickness. The increase prevents tearing of metallic gates during the wet-chemical liftoff when climbing the previous layer. A zoom-in of the gate stack is shown in the false-colored SEM image in Figure 6.1b.
Ohmic contacts to the quantum well are fabricated via ion implantation of phosphorus atoms and a rapid thermal annealing step as described in 3.1.2. The Ohmic contacts are labeled by Roman numbers in the SEM image in the four corners of the device.
The device is symmetric to the x-axis and features the possibility to tune two sensor dots



(a) **(b)**

Figure 6.1: Heterostructure and gate layout. **(a)** Undoped Si/SiGe heterostructure. **(b)** False-colored SEM image of the device layout.

on both left and right end for charge sensing. Electrons are accumulated by the two large gates TGL and TGR (blue in Figure 6.1b) and on both ends three plunger gates (pink) enable the formation of tunnel barriers and a potential minimum in between, confining the sensor quantum dot.
In between both sensors a channel is defined by the larger rectangular gates ST and SB (light brown), providing the possibility to form 4 serial quantum dots under the plunger gates P_1-P_4, separated from each other and the sensor dots by the barrier gates B_1-B_5. The sensor dots may serve as reservoirs for the serial (qubit) quantum dots.
In the following section we discuss the tuning of the device via charge sensing readout and control the electron number on the qubit quantum dots.

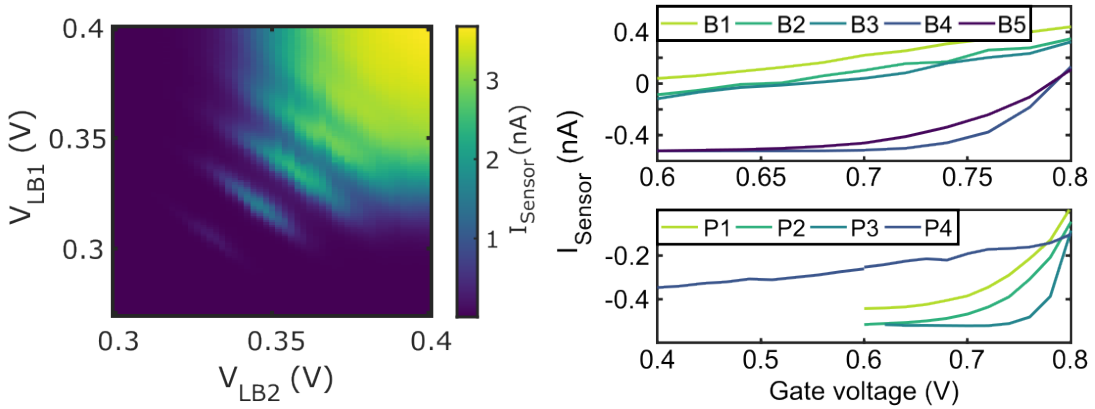
6.1.1 Tuning the sensor, a single and a double qubit system

To put the device into operation we accumulate electrons in the quantum well and tune the electrostatic potential configuration such that a sensor dot as well as a single or double qubit quantum dot configuration is formed.

Sensor tuning

We want to operate the device with one or more consecutive qubit quantum dots under plunger gates P1-P4 and we intend to read out the qubit quantum dot occupation via

charge sensing by a sensor dot at an end of the device. We started by focusing on the tuning and readout of the left sensor, but experimentally observed that both sensor dots were tuned very similarly. Therefore, we only present data of the left sensor dot tuning here.



(a) **(b)**

Figure 6.2: Accumulation of electrons in the Device (a) Coulomb blockade in the left SET can be tuned by the two gates LB1 and LB2 which predominantly control the tunnel barriers of the dot. **(b)** Pinch-off curves of the current through the device channel from Ohmic contacts I/II towards contacts III/IV.

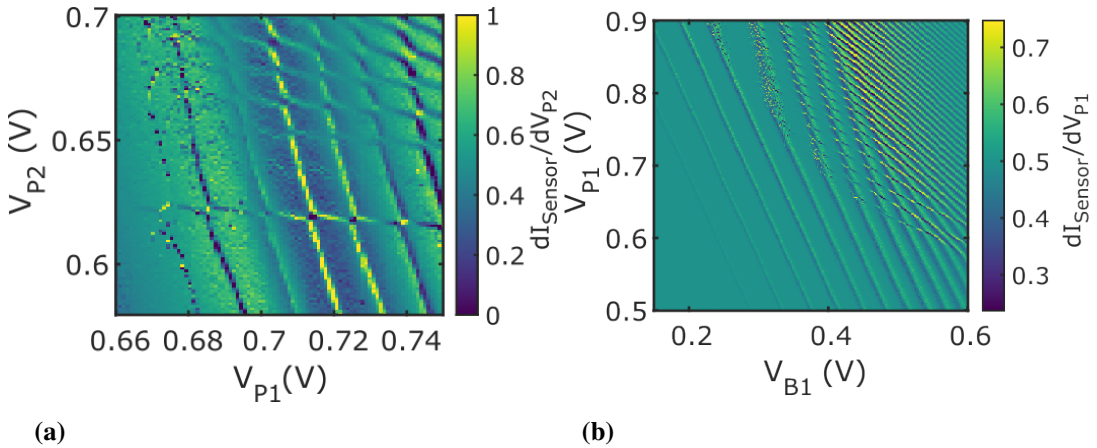
We accumulate electrons in the sensor predominantly by the gate TGL. Electrons start to accumulate at a voltage of close to 1000 mV applied to TGL, when all surrounding screening, plunger and barrier gates are also set to a positive value of a few hundred mV (about +400 mV). A measurement of the current between Ohmic contacts I and II as a function of the two gates LB1 and LB2 is shown in Figure 6.2a.
We observe a non-interrupted current flow underneath gate TGL for 400 mV applied to LB1 and LB2. For lower voltages we observe a modulation of the current: Current is only conducted along parallel lines and blocked in between, indicating the formation of a quantum dot. As these Coulomb-blockade lines lie almost diagonal in the figure, we conclude that the sensor dot is formed symmetrically in between both barrier gates LB1 and LB2.
Each of the Coulomb peaks can be used for charge sensing of the adjacent qubit quantum dots under P_x (see Concepts 2.3.2). For a large signal in a charge sensing measurement and hence a lower error rate in the charge sensing detection, we aim for steep edges of the Coulomb peaks. In the tuning of the sensor dot we observed a strong dependence of the sensor blockade on both the barrier gate B1 and the gate TGL, as the peaks became flatter

for larger TGL voltage values as well as for larger B1 gate voltages.
The measurement in Figure 6.2a presents the formation of a sensor dot with steep Coulomb peaks, from which the second visible peak at around 340 mV applied to both gates is the steepest. We will use this peak for the following charge sensing measurements.

Current pinch-off and formation of a single and a double dot system

With the sensor in place, we next check the functionality of all remaining gates and also accumulate electrons inside the channel connecting the sensor dots, which eventually hosts the qubit quantum dots. Increasing the voltages on all plunger and barrier gates P_x and B_x to 800 mV induces a current along this channel. We record a current measurement in the drain of the left sensor (Ohmic II), shown in Figure 6.2b. For this measurement we lift the sensor Coulomb blockade by also increasing the gate voltages on LB1, LB2 and LP to 600 mV and similarly on the gates on the right end of the device. As four Ohmic contacts are connected during the current measurement in Figure 6.2b, the current measurement is not straightforward. We applied a positive bias voltage to the Ohmic contacts III and IV and kept the potential of contacts I and II at ground. Due to the four involved Ohmic contacts, a value of about -0.5 nA corresponds to a pinched-off channel, while a positive current indicates current along the channel underneath P_x and B_x.
The upper panel of Figure 6.2b shows a measurement in which we alternately lower the gate voltage applied to one of the gates B_x while keeping the other 4 gates at a voltage of 800 mV. By increasing the potential directly underneath one of these gates through the lower gate voltage, we intend to form a barrier along the current channel and pinch-off the current flow. We observe, that all B_x gates can pinch-off the current, but we also observe that the pinch-off occurs at a much steeper rate and already at a higher gate voltage for gates B4 and B5, while gates B1-B3 resemble each other and show a much flatter pinch-off.
The lower panel shows the same measurement using the gates P_x. Again we observe that all gates pinch-off the current. We observe that gates P1-P3 pinch-off already at a gate voltage of 700 mV, while the current has not yet been interrupted for a gate voltage of 400 mV applied to P4. We interpret from both measurements that gate P4 might be broken at some point along the metallic gate and that the gate allows only a reduced control of the underlying electrochemical potential in the quantum well. Note, that the gates P_x have 10 nm less oxide between gates and quantum well compared to the gates B_x. Therefore, the steeper pinch-off of gates P1-P3 compared to gates B1-B3 is expected.
As we assume that gate P4 is broken, we focus on the left-hand side of the device and attempt to form a double qubit dot system under gates P1 and P2 and load the qubits from the SET sensor on the left-hand side, while simultaneously using this SET for the charge sensing readout. The idea behind this tuning is that in such a configuration we do not

necessarily use the right-most barrier and plunger gates and are not limited by the broken P4 gate.
For the tuning of the double dot system under gates P1 and P2, we tune our SET to the sensitive configuration shown in Figure 6.2a. We pinch-off the current through the device channel by decreasing the voltage at gate B3. By also slightly decreasing B1 and B2 we form two tunnel barriers underneath the respective gates. Figure 6.3a shows a stability measurement of the double dot system varying gates P1 and P2. The measurement shows the derivative of the left SET sensor current. In the measurement we make two observations: First, we observe a slow modulation of the background, mainly varied by the P1 gate voltage. For voltages below 700 mV we measure a positive current derivative, in the interval between 700 mV and 720 mV we detect a negative derivative of the current and for voltages larger than 720 mV we again measure a positive derivative. We identify this slow background modulation of the current as coupling of the P1 gate onto the sensor dot and link one full oscillation (positive slope, subsequent negative slope) as traversing of one sensor Coulomb blockade peak. Hence in this experiment we measure one and a half sensor Coulomb blockade peaks. The second observation is the grid-like modulation of the sensor current derivative on top of the SET Coulomb blockade peak. We observe two sets of parallel lines. One set of the lines couples much stronger to the P1 gate voltage, the second set couples much stronger to the voltage applied to gate P2. As these two sets of lines do show the exact opposite algebraic sign in the current derivative (See section 2.3.2), we identify these lines as charge sensing lines of two quantum dots, one located underneath gate P1 and the second underneath gate P2. We conclude the estimated position of the quantum dots by the respective gate coupling strength. As we strongly reduced gate voltage B3 ahead of the measurement, we conclude that the quantum dot underneath gate P2 is loaded from the quantum dot underneath gate P1.
We observe in the measurement, that the last visible transition for the first quantum dot under gate P1 becomes fragmented for voltages of P1 < 690 mV. We explain this fragmentation by the fact, that the tunnel barrier between the quantum dot under gate P1 and the SET sensor dot, which here serves as its electron reservoir, becomes opaque due to the reduced P1 gate voltage.
From complementary tuning measurements, which are not shown here, we observed that the double dot system is completely emptied for the lowest gate voltage configuration in the bottom left corner of the measurement; the system here is in the (m,n) = (0,0) state. In fact the m=1 line that corresponds to a loading of the right quantum dot by the first electron, which we measure here around a gate voltage of P2 = 625 mV, does not continue on the left side of the n=1 transition of the left quantum dot underneath gate P1, as the right quantum dot can no longer be loaded from the left quantum dot.
This double dot system can easily be tuned towards a single dot system by depleting the right quantum dot under gate P2 completely. Figure 6.3b shows a charge stability



(a) **(b)**

Figure 6.3: Tuning of qubit dots in the device. (a) Double Dot. Two sets of parallel charging lines of which one set couples strongly on the P1 gate voltage, while the second couples much stronger on the voltage applied to gate P2. **(b) Single Dot.** We can control the charging of the first electron onto the quantum dot. The measurement shows that for B1 gate voltages larger than 550 mV sensor dot Coulomb blockade lines and charging lines start to merge, while for voltages below 400 mV the tunnel coupling becomes weak.

measurement recorded with gates P1 and B1 after the right quantum dot was fully depleted. The figure shows two sets of lines, one set in the background which couples stronger to the voltage of B1 and a second set of lines which in comparison does couple stronger onto the P1 gate voltage. Again we identify the background oscillations as Coulomb blockade oscillations of the sensor dot. As the sensor dot is located on the left-hand side of the B1 gate it is further physically separated from the P1 gate than from the B1 gate. This larger separation explains the stronger coupling of the Coulomb oscillations to the B1 gate voltage. In turn, we identify the second set of lines in the measurement, which do show again the inverse algebraic sign in the current derivative, as charging transitions of the qubit dot under plunger gate P1.

For B1 voltages below 400 mV the charging lines start to fizzle. As B1 predominantly controls the tunnel barrier, we interpret this fizzling as a decrease in the strength of the tunnel coupling between qubit and sensor dot.

Notably, we do not observe any more charging transitions below the last visible one here around a voltage of P1 = 650 mV. As also for increasing B1 voltage no further transition appears in the measurement, we identify this last visible line as the charging line corresponding to the first electron being loaded onto the qubit quantum dot.

In the measurement we can make a further interesting observation. For the largest B1

gate voltages here, the charging lines and the Coulomb blockade oscillations of the sensor dot start to merge. We interpret this observation as the beginning of the formation of one single quantum dot, merging SET and qubit quantum dot when the tunnel barrier separating both becomes quite low for these large B1 gate voltages. We do not intend to operate the qubit in this regime, but wanted to note this observation here.
As a short intermediate summary we can state, that the device allows the formation of quantum dots underneath the plunger gates P1 and P2. Notably, especially in comparison to the depletion-type architecture device measured during my Master's thesis [75], the location of the quantum dot formation is much better controlled already by the device design in the accumulation-type architecture. We also do not measure a single unintended quantum dot formation or measure charging of single defect states in the device, which both have occurred in the depletion-type device [75].

6.1.2 Tunnel rate tuning by barrier and plunger gates

We continue the device characterization with the aim of using the single quantum dot underneath gate P1 as qubit. Single-shot loading and readout of this qubit demands precise and quantitative control of the tunnel rate of the last electron between reservoir and quantum dot. The tunnel rate sets the timescale for all single-shot measurements and has to be adjusted on the one hand to the spin relaxation rate and on the other hand to the bandwidth provided by the measurement equipment.
Here, we also aim for a better understanding of the accumulation-type gate architecture, especially in terms of lever arms, gate cross-couplings and pinch-off behavior and compare such results to results of depletion-architecture qubit devices and devices with qubit tunnel coupling to a 2DEG reservoir.

By design we expect the height of the tunneling barrier potential and hence the tunnel rate to be dominantly controlled by the gate directly above the barrier, here B1. We also expect all other surrounding gates to impact the tunnel barrier via capacitive cross-coupling, as already introduced in the concepts section (2.3.2).
The additional capacitive coupling of the qubit plunger gate P1 on the tunnel barrier for example is already apparent in Figure 6.3b. For the N=1 charging transition we observed that the charging line starts to fizzle at a B1 gate voltage larger than 400 mV. Looking now for example at the N=5 transition, which appears at a larger P1 gate voltage, the same fizzling starts at a B1 gate voltage only well below 400 mV. The difference can be explained by the increased P1 gate voltage and its cross coupling onto the tunnel barrier.
For a quantitative tunnel rate analysis we first focus on the impact of the B1 gate voltage, which we assume to have a larger impact by the device design and subsequently characterize the impact of the P1 qubit plunger gate voltage separately.

Barrier gate voltage

To investigate the impact of B1 on the tunnel coupling, we tune the electrostatic configuration to four different configurations along the N=1 transition line of the first electron loading, as shown in Figure 6.4a.

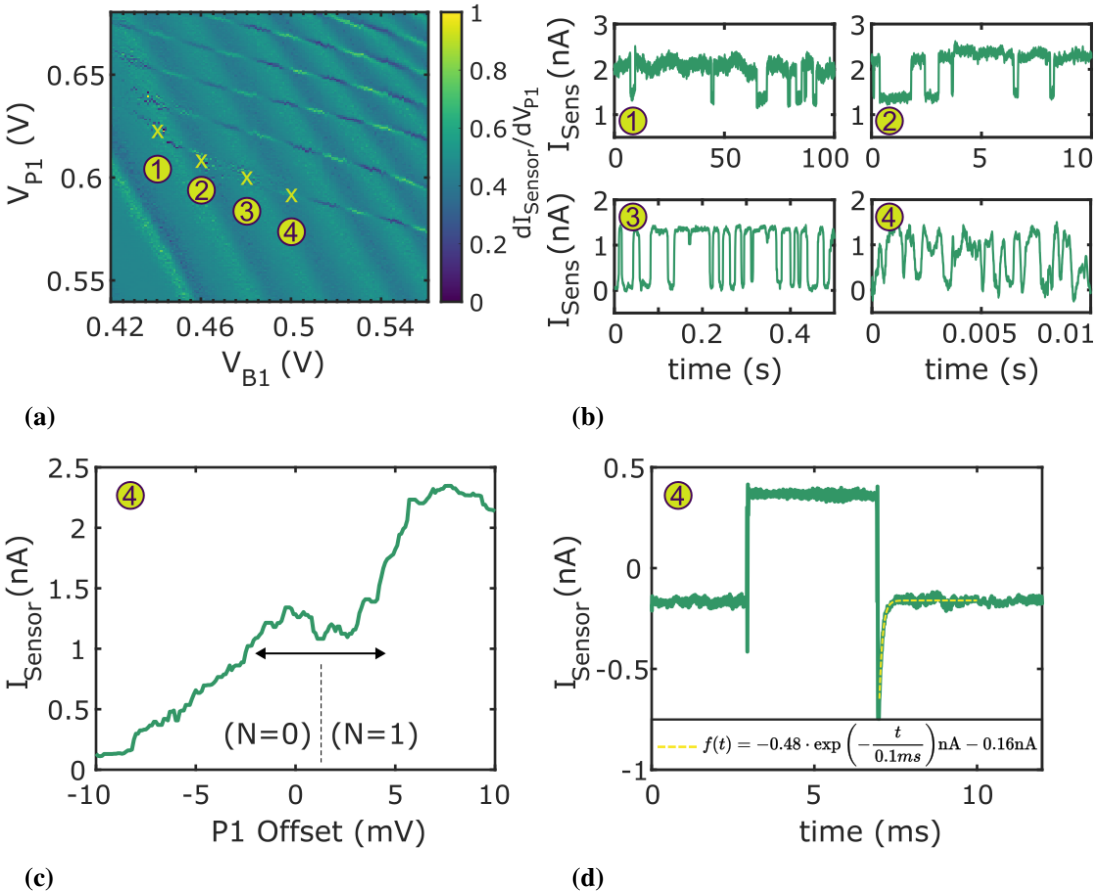


Figure 6.4: Tunnel barrier tuning. **(a),(b)** Telegraphic noise measured at four different configurations along the N=1 transition. **(c)** Line-scan across the N=1 transition. **(d)** Single-shot two-phase pulse loading and unloading the qubit. A fit to the exponential current increase of the averaged single-shot measurements at the beginning of the loading phase is colored yellow.

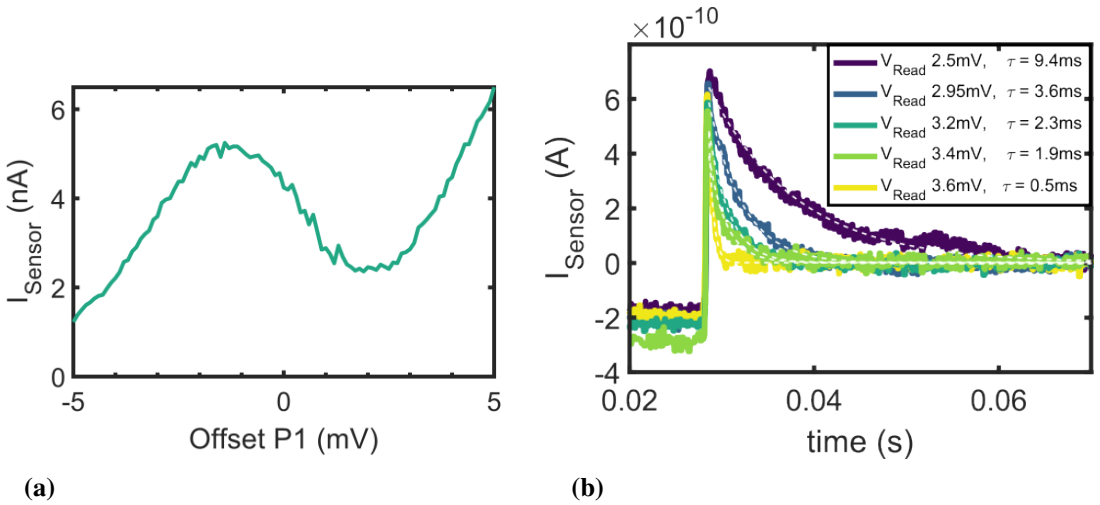
For each of those four configurations we record the current over time, shown in Figure 6.4b. For all four measurements the current signal tends to oscillate between two values. The two current values of this so-called telegraphic noise correspond to the two states of the

qubit dot being uncharged or charged and the two measured current values reflect the corresponding shift along the sensor Coulomb peak following the electron tunneling to or off the qubit (Figure 6.4c). The duration of the individual segments (uncharged/charged) is relatively long for configuration ① with the lowest B1 gate voltage of 440 mV (here 10-15 seconds) while it becomes ever shorter the higher the gate voltage of B1 is set. For configuration ④ with a B1 gate voltage of 500 mV we measure a fluctuation faster than 1 ms, which is more than 3 orders of magnitude shorter compared to configuration ①. Note, that the tunnel rate decreases from ④ to ①, despite the P1 voltage increase. We interpret again the tunnel rate to be dominated by B1.
To quantitatively evaluate the tunneling rate, we apply a simple pulsing scheme: A rectangular voltage pulse on P1, periodically tuning the qubit potential from the (N=0) state across the charging transition into the (N=1) state and vice-versa. This pulsing scheme already allows for a single-electron control, as in each measurement cycle exactly one electron is loaded onto the qubit dot when the configuration is tuned into the N=1 regime. During the second phase, the unloading phase when tuned into the N=0 regime, this single electron will tunnel off the qubit again. The two-phase pulse measurement is also indicated in Figure 6.4c by the black arrow. Coming from the N=1 configuration and tuning to N=0 at a voltage offset at P1 of about -3 mV, we first expect a current of about 0 nA which then abruptly increases to about 1 nA when the qubit dot is unloaded. Vice-versa, coming from the N=0 state and pulsing to a P1 gate offset of about +5 mV, we do not expect such a large sensor response following the loading of the qubit, as the configuration is at the peak of the sensor Coulomb oscillation. Here, the sensor is not very sensitive.
We apply the pulse to a configuration with yet higher B1 and hence faster tunnel rate compared to ④ in Figure 6.4a. The averaged sensor signal of about 1000 single-shot measurements is shown in Figure 6.4d. The median value of each trace was subtracted before the averaging. We observe two different current values reflecting the two phases of the rectangular pulse. The higher current value corresponds to tuning the qubit into the N=1 regime, the lower into the N=0 state. We observe an exponential increase at beginning of the pulse phase bringing dot into (N=0) state after about 7 ms of pulse duration. The exponential increase results from the summation of the individual abrupt current increases in each single-shot measurement and hence allows to extract the tunneling rate from an exponential fit. This fit reveals a tunneling rate of about 1/100 µs.
We conclude this section of tuning the tunneling barrier by noting that we could tune the tunneling rate by many orders of magnitude using gate B1. Here, we measured tunneling durations ranging from many seconds to 100 µs, allowing us flexibility in driving of the qubit dot.
We also want to note, that the tunneling rate of 1/100 µs is about as fast as we can resolve with our measurement setup. We cannot resolve faster tunneling rates in single-shot

measurements as we get limited by both, the experimental setup bandwidth limit given by the DC connection and the lowpass filtering along these DC lines as well as by our averaging and filtering procedure of the single-shot measurements, shown in the appendix A.3.6.

Plunger gate voltage

In the configuration in which the device is tuned to host a qubit dot underneath gate P1 and is loaded from the SET on the left-hand side of the device underneath gate TGL, we form the tunnel barrier directly underneath gate B1. In the last section we also already observed, that we can tune the tunnel rate by the B1 gate voltage over more than 6 orders of magnitude. But from tuning measurements shown before we observed that there is some gate cross-coupling present in the device, which is unavoidable. By the term gate cross-coupling we mean that for example the B1 gate does not only control the tunnel barrier separating the SET and the qubit dot, but that the B1 gate voltage also affects the sensor tuning or the qubit dot energy tuning via capacitive coupling. Vice-versa we also expect a cross-coupling of the P1 gate onto the tunnel barrier underneath gate B1. Here we demonstrate how to tackle this challenge of P1 gate cross-coupling.
To do so we fix the B1 gate voltage to a value in between configuration ④ and ③ in Figure 6.4a. We record a measurement of the sensor Coulomb peak featuring the N=0 to N=1 qubit transition as shown in Figure 6.5a. We now tune the transition such, that the sensor is sensitive when the qubit is tuned into the N=1 regime, unlike the linescan in Figure 6.4c, where the sensor was tuned sensitive in the qubit N=0 regime. We continue by applying the same rectangular pulse across the N=1 transition as before with gate P1. We also give the two phases of the rectangular pulse names: unloading and readout of the qubit dot. During the unloading phase we bring the quantum dot potential electrostatically into the unoccupied (N=0) voltage regime at a P1 offset voltage of about -5 mV. For the readout we pulse the qubit into the N=1 regime, at +2-3 mV.
In the measurement series in Figure 6.5b we intend to vary the voltage of the readout pulse in the N=1 regime. We apply the two level rectangular pulse 1000 times and average the sensor signal. We vary the readout voltage (offset) for the consecutive measurements from 2.5 mV to 3.6 mV, meaning we pulse deeper into the N=1 regime by increasing the P1 voltage offset. Note, the actual P1 voltage is at about +600 mV, here we merely apply an additional voltage for fine tuning along the charging transition.
In Figure 6.5b we observe an exponential decrease of the measurement signal at the beginning of the readout phase for all five readout voltages. By fitting the data, we observe a clear increase in the tunnel rate, by a larger P1 voltage during the readout. The tunneling constants change from 10 ms to less than 1 ms. This increase is considerable and potentially caused by gate cross-coupling. The effect must be considered when



(a) **(b)**

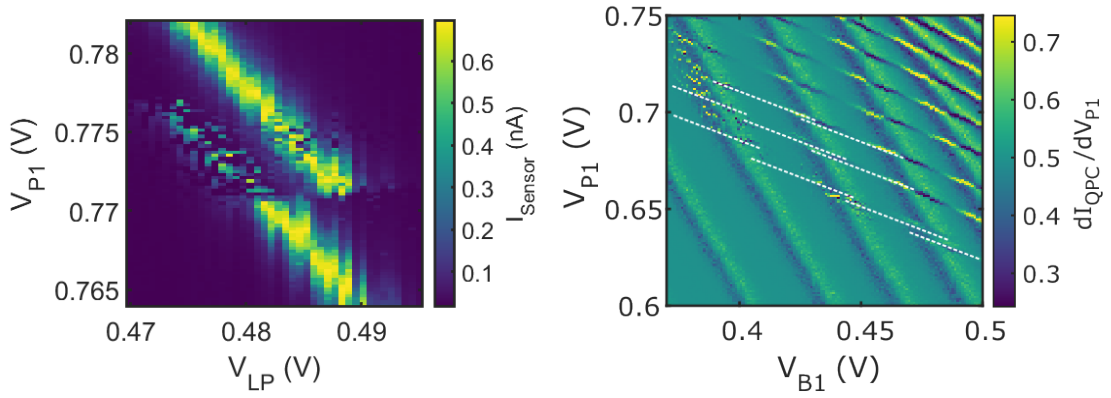
Figure 6.5: Analysis of the P1 gate cross-coupling on the tunnel barrier underneath B1. **(a)** Line scan of the sensor tuning. The sensor is tuned sensitive in the N=1 qubit regime. **(b)** Exponential fit following a two-level pulse sequence for different qubit readout voltages.

performing any readout and if necessary be corrected by tuning the B1 gate voltage.

To summarize the tuning of the tunneling barrier we did observe a very good tunability over a wide time scale. We did not observe significant differences in tuning of the tunnel barrier compared to a depletion-type architecture device [58], although the gate cross coupling may still be slightly lower here for the accumulation-type device.

6.1.3 Simultaneous use of the sensor dot as electron reservoir

The tuning of the qubit formation as well as of the tunnel barrier is similar to the tuning of a depletion-type architecture device [58], in which the tunnel barrier also was tunable over a wide range. The accumulation-type device used here however, does have a peculiarity by design in comparison to many of the devices used at the time of the beginning of this thesis. The qubit dot underneath gate P1 is loaded from a second quantum dot, which we use simultaneously as sensor for the charge-state readout. A challenge of using the sensor dot as reservoir might be, that the density of states (DOS) of the sensor dot is discrete and not continuous as expected for 2DEG reservoirs used in comparable depletion-type architecture devices [4, 5, 58].
In the following section, we now focus on the impacts of loading from a quantum dot instead of a reservoir with a continuous DOS. The measurement in Figure 6.6a shows the



(a) **(b)**

Figure 6.6: Analysis of the charge sensing signatures when loading the qubit from a quantum dot with a discrete DOS. (a) Zoom-in of the N=0 to N=1 charging line of the qubit dot. **(b)** Observation of discrete steps in the charging lines, whenever a line crosses the Coulomb blockade of the sensor dot.

N=0 to N=1 transition of the qubit quantum dot.
The figure shows a Coulomb blocked sensor peak with low source-drain bias, that is interrupted and shifted at a plunger gate voltage of about P1 = 771 mV. We identify this shift in the voltage of the sensor blockade as signature of the charging of the N=1 electron onto the qubit dot at the qubit plunger voltage of P1 = 771 mV. Below that voltage the qubit quantum dot is empty (N=0), for higher voltages we expect it to be in the N=1 configuration. The now added electron above P1 = 771 mV shifts the sensor peak to larger LP voltages to compensate the electric field of the additional loaded electron. This is the typical signature of charge sensing, already explained in section 2.3.2. For the measurement here we apply a very low bias voltage of only 50 µV, hence, the sensor Coulomb peak is very slim in the presented measurement and we do not end on the flank of the Coulomb peak following the qubit charging, but rather shift the complete peak in the gate voltage space.
However, in contrast to the typical signature of charge sensing, in the measurement in Figure 6.6a we observe additional tunneling events following the left coulomb blockade branch in a voltage window as large as 5 mV above the charging transition of 771 mV. Contrary, on the right sensor peak branch, we barely observe such events above or below the qubit charging transition. A potential explanation could be the discrete DOS of the sensor dot. A detailed analysis will be given in the following. Here we want to note that the tunnel rate for this measurement was set to about 1/300 µs, much faster compared to the measurement speed of 5 mV/s. Also the gate sweep direction of the P1 gate

voltage was from higher to lower voltages, to exclude the measurement error discussed in the Appendix in section A.3.3. This fizzling in the charge sensing signal was observed independent of the used gates. In the measurement in Figure 6.6a we used gates P1 and the sensor plunger LP, but it also appeared when using P1 and B1 to map the charging transition of the qubit.
Having a wider view on the individual transitions in a charge scanning measurement, steps in the transition lines become apparent whenever a charging line crosses a sensor Coulomb peak, indicated by white dashed lines in 6.6b. Both of these two effects have been observed independent of sensor bias, magnetic field or sweep rate of the used gates. Hence, we expect the origin in the discrete nature of the sensor DOS which was used as reservoir.

A possible explanation for both previous observations is given in Figure 6.7. The figure shows the same measurement as before in the center, surrounded by a false colored SEM image on the left-hand side to illustrate the location of the source and the drain Ohmic contacts of the SET as well as the estimated position of the sensor and the qubit dot. The figure also shows 6 sketches of the electrochemical potential for different voltage configurations, labeled with numbers ① - ⑥. Sketches ① - ④ mark the extreme cases of the voltage regime that features the unexpected additional electron tunneling events which we suspect to arise from the discrete nature of the sensor dot's DOS which serves as reservoir for the qubit dot. In the potential sketches, the individual levels of reservoir, sensor and qubit dot are purposely drawn with a certain thermal broadening. The occupation of the qubit dot is labeled with a capital N, the one of the sensor dot with a small n.
For the first two potential sketches ① and ② the qubit-dot level N=1 is exactly aligned with a sensor dot level. The imaginary line connecting the configurations ① and ② we typically identify as the charging transition of the qubit by the first electron N=1. The two configurations also mark the edges of the sensor Coulomb blockade: In configuration ①, the (n+1) sensor dot level is aligned with the Fermi energy of the source Ohmic contact, while in configuration ② the (n+1) sensor dot level is aligned with the drain Ohmic contact. Due to the capacitive coupling of the qubit dot onto the sensor dot, the sensor dot level depends on the electron occupation of both quantum dots. Hence in the following we will use two labels for the sensor dot level description, here $(n_{Sensor},N_{qubit}) = (n+1,1)$. Increasing now the P1 gate voltage to a value larger than 771 mV, the qubit N=1 level is energetically pushed below the (n+1,0) level of the sensor dot. Hence an electron can tunnel onto the qubit and remains confined there. Note, that in this configuration, the (n+1,0) state of the sensor can no longer contribute to electron transport through sensor. Also the (n+1,1) state of the sensor is energetically above the source-drain sensor bias window and current through the SET should be blocked. The LP gate voltage has to

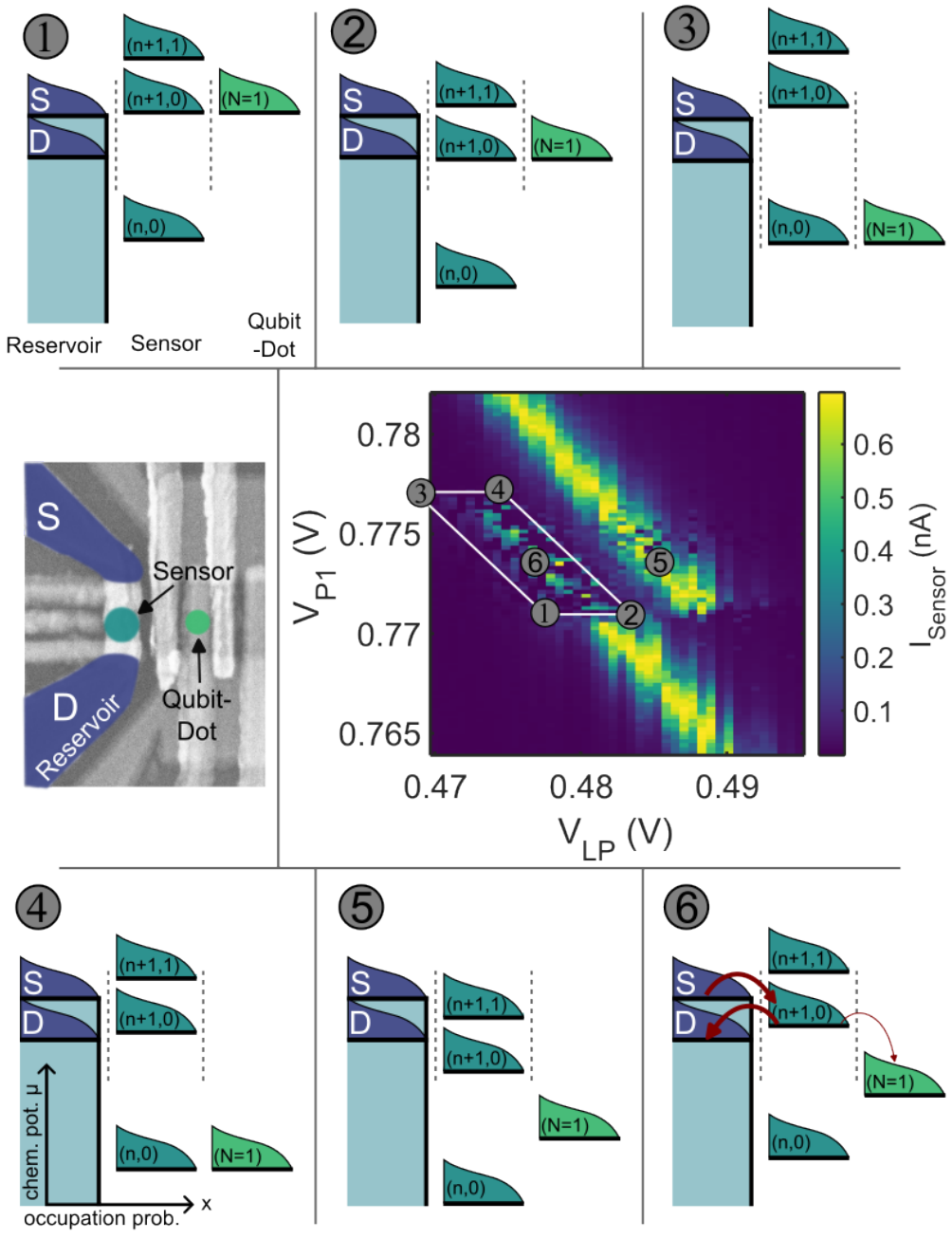


Figure 6.7: Explanation of the appearance of additional current transport due to the discrete nature of the SET's DOS serving as the qubit reservoir. Measurement of the N=1 qubit charging transition, surrounded by a false-colored SEM image of the device and 6 sketches of the electrochemical potential at 6 configurations within the measurement.

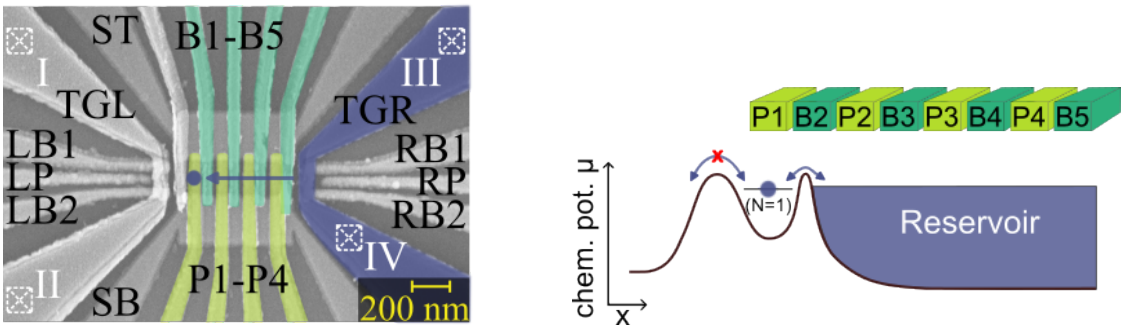
be increased as shown for example in configuration ⑤, bringing the (n+1,1) state of the sensor into the source-drain bias window and enabling current transport through the sensor again.
Nevertheless, we observe this additional temporary current transport in the white square, framed by ① through ④. These events terminate first, when the qubit level (N=1) is aligned with the next lower sensor state (n,0) in ③ and ④.
We explain the emergence of transport through the sensor in the white square by the assumption that the qubit quantum dot may temporarily be unloaded as the electron eventually tunnels back onto the sensor dot for example through thermal excitation. Subsequent re-loading of the qubit dot via the sensor level (n+1,0) does now not take place instantaneously, because the tunnel coupling of the sensor to the drain Ohmic contact is so much stronger (sketched by the arrow thickness in ⑥) and hence for a certain amount of time transport through the sensor becomes visible again. We expect the tunnel coupling of the sensor dot to its drain Ohmic contact to be much larger than to the qubit dot. From a previous estimation of tunnel rate we determine about $O(10^2)$ sensor-qubit dot tunnel events per second. This is many orders of magnitude lower compared to about $O(10^9)$ tunnel events per second we expect for a source-drain current of 1 nA.
In configurations ③ and ④, when the qubit quantum dot can energetically now be loaded via the lower lying (n,0) sensor state, re-loading of the qubit dot occurs instantaneously and no transport is observed in the measurement beyond configurations ③ and ④.
This assumption is supported by the fact, that the faster the tunneling rate between sensor and qubit quantum dot, the shorter and the lower current is measured in the just discussed white rectangular in Fig. 6.7. For tunnel rates faster than about 1/100 µs we do not observe this effect any more in our measurements.
This effect clearly can be reduced to the 0D reservoir in this sample here. In devices with a continuous density of states in the reservoir such effects have not been observed.
We also do not only see this effect for the transition of the last electron N=1, but for all qubit transitions. These considerations do also explain the discrete steps in Figure 6.6b: When the qubit transition crosses a sensor transition, the qubit is loaded from a different sensor dot level. In the detailed explanation before, that would be loading from (n,0) instead of (n+1,0).

In this section we observed that the loading of the qubit dot via a SET sensor seems challenging, because of the sensor dot's discrete density of states (DOS). Moreover, the Fermi energy of the sensor dot, which we identify as the highest occupied discrete SET state, depends on the qubit occupation due to its capacitive coupling to the SET.
In our measurement, the discrete nature of the SET DOS manifested in a lack of a set qubit plunger gate voltage, above which the N=1 electron is loaded onto the qubit dot and below which the qubit dot is empty. We rather observed a wide plunger gate voltage

range in which electron tunneling between qubit dot and SET was energetically possible - a feature we have not observed in devices, in which the qubit is loaded via a 2D reservoir instead of a quantum dot. The lack of a set voltage for the energetic alignment of the N=1 qubit level and the Fermi energy of the SET poses a challenge for the qubit spin readout which critically relies on the exact alignment of the N=1 spin up and spin down levels with the reservoir.
Moreover, also for the qubit initialization we expect an imbalance in the average spin orientation due to the discrete DOS of the SET.

6.1.4 Using the Qubus channel as elongated electron reservoir

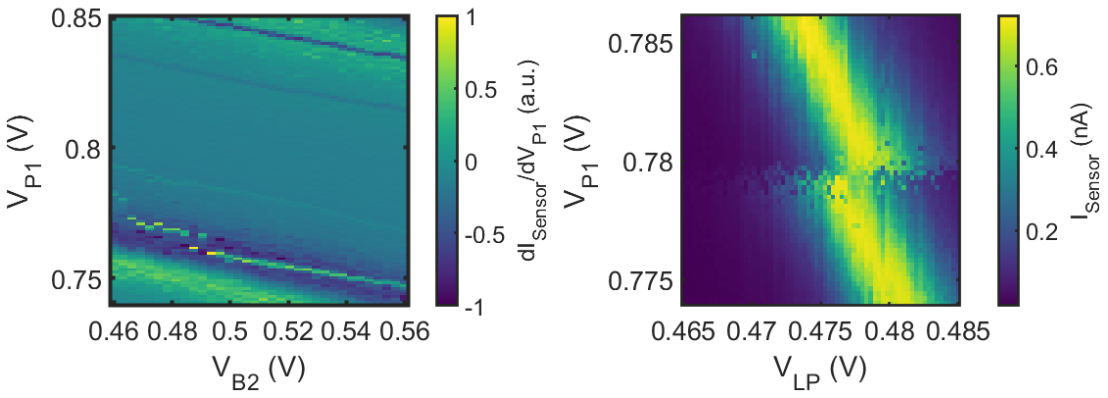
We continue the analysis in the next section by averting from the sensor dot as electron reservoir for the qubit. As the electron exchange between qubit and the SET on the left-hand side of the device seems challenging due to the SET's discrete DOS, we completely block the tunnel coupling of the qubit dot and the SET by increasing the tunnel barrier height and width through a lower B1 gate voltage of about +300 mV, which is significantly lower than in all previously introduced measurements. By this tuning, the capacitive coupling of qubit and sensor dot is maintained, preserving the qubit charge state readout capability.
We now aim to form a reservoir that is not restricted by discrete energy states due to a 0D confinement by using the Ohmic contacts III and IV on the right-hand side of the device (Figure 6.8a) and extend the electron reservoir also under gates P2-B5, like shown in Figure 6.8b. By tuning the gate voltages of P2-B5 above 1 V, a comparatively large value, we explicitly intend to not form quantum dots in the channel, but to homogeneously accumulate electrons. This channel is confined sideways by the screening gates ST and SB. We also increase the voltages on RB1, RP and RB2 to not form potential barriers or a second quantum dot on the right-hand side of the device.
An experimental analysis of this reservoir is to check, whether it is suitable for spin readout of the qubit dot by spin dependent tunneling, which is the main task of this chapter. We expect distinct differences to the zero-dimensional character of the SET reservoir, as we avoid the formation of separated electron islands by the gate voltage increase on the right-hand side of the device (6.8a). A 2D reservoir, which was studied extensively in the literature in recent years, provides a continuous DOS, like sketched in Figure 6.8b, allowing precise spin-to-charge conversion readout. The device geometry here however suggests an one-dimensional character, which DOS would follow the power law $\frac{1}{\sqrt{E}}$, so would not be continuous but may behave comparable to the 0D reservoir posed by the SET. The DOS characteristics will experimentally be evaluated in the following.



(a) (b)

Figure 6.8: Reservoir through the device channel. **(a)** False-colored SEM image of the device, highlighting the reservoir accumulation using Ohmic contacts III and IV. All yellow, green and blue colored gates, except P1 and B1, are raised to a voltage above 1 V. **(b)** Illustration of the reservoir accumulation on the right-hand side of the qubit. The tunnel coupling of the qubit to the SET on the left-hand side is blocked by increasing the tunnel barrier width.

For this new configuration, B2 is now the barrier gate separating qubit quantum dot from the reservoir, while P1 remains the plunger gate of the qubit. We again record a charge stability diagram of the qubit dot, which is presented in Figure 6.9a. The figure shows the derivative of the SET current, which is still on the left-hand side of the device, but electrons are exchanged between qubit and reservoir from the right-hand side. The figure shows two Coulomb blockade peaks of the SET sensor as broad lines, centered around 765 mV and 850 mV gate voltage applied to P1. On top of these sensor peaks, we observe the charging of the qubit by the first 5 electrons, which emerge in the measurement as the 5 fine charge sensing lines. The N=3 transition is barely visible at a plunger gate voltage of about P1 = 800 mV, because the sensor does not conduct current in that voltage configuration. We estimate its existence from the voltage spacing of the remaining 4 charging transitions. We ensured from complementary measurements, which are not shown here, that the lowest visible transition in the figure corresponds to the loading of the first electron N=1 onto the qubit. We observe a fizzling of the N=1 transition for B2 voltages below 500 mV. We correlate this effect in the measurement to a reduction of the tunnel coupling for lower B2 gate voltages: The tunnel rate becomes lower than the measurement speed (see Appendix A.3.3). We want to distinguish this observation from the formation of discrete steps in the charging line due to loading from different discrete states in the reservoir, which was introduced in Figure 6.6b. A thorough tuning of the tunnel rate for this new configuration will be presented in section 6.1.4.



(a) **(b)** . .

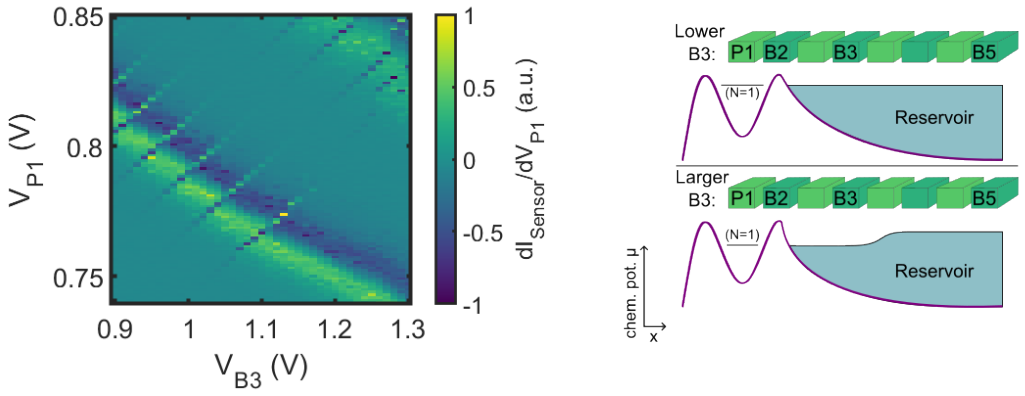
Figure 6.9: Stability measurement of the qubit when loaded from the right-hand side. **(a)** Derivative of the SET current. The measurement shows the charging of the first 5 electrons onto the qubit. For the N=3 transition, the sensor is in an insensitive configuration, making the transition barely visible. **(b)** High-resolution of the N=1 charging of the qubit.

Before we tune the tunnel rate with the reservoir on the right side of the qubit and eventually prepare single-shot operation of the qubit, we now focus on an investigation of the DOS of the reservoir through the device channel. Figure 6.9b shows a high-resolution measurement of the charging of the first electron onto the qubit. Similar to the measurement in Figure 6.7, the measurement here is also recorded using the sensor plunger gate LP and the qubit plunger P1. In contrast to the measurements using the SET as reservoir in the previous chapter, here we do not observe additional tunneling events. In this exemplary measurement here, we can assign a gate voltage of P1 = 779 mV to the charging of the first electron. The absence of electron tunneling events, once the qubit dot is tuned in the N=1 configuration, constitutes a big advantage of this new reservoir from the right side. The transition in the measurement seems only broadened to an equivalent of about 1 mV in gate voltage on gate P1 which corresponds to the thermal broadening still present at cryogenic temperatures. A detailed analysis of the electron temperature can be found in the appendix in A.3.1.

Positive charge sensing slope

The absence of additional tunnel events beyond the N=1 loading voltage threshold is a promising indication that the newly formed reservoir on the right half of the device does not exhibit a dominant discrete level structure of the DOS. During the accumulation and

tuning of the right reservoir however, we observed a second characteristic of this newly tuned, elongated reservoir.
A stability measurement of the qubit loading transitions, recorded as a function of the qubit plunger and the remote gate B3 is shown in Figure 6.10a. The figure shows the derivative of the SET current. We observe two sensor Coulomb peaks which form two broad diagonal lines trending from the bottom right corner of the graph towards the top left corner.



(a) **(b)**

Figure 6.10: Positive charge sensing slope in the stability measurement. (a) Derivative of the SET sensor current. We observe an expected dependence of the SET Coulomb blockade on the two varied gate voltages, but a counter intuitive positive slope of the charging lines. **(b)** Sketch of the chemical potential and the Fermi energy of the reservoir on the right-hand side of the device for two different voltage configurations along the N=1 charging line.

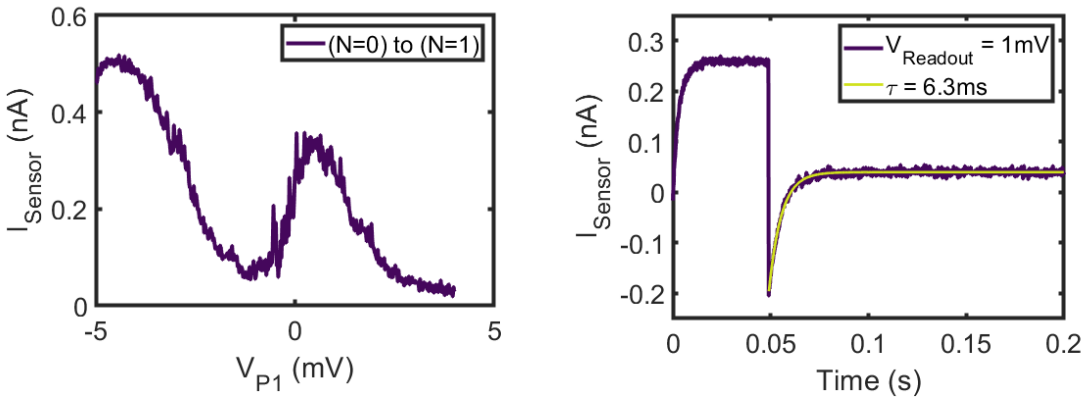
We also observe 6 charge sensing lines in the measurement for the loading of the N=1st to N=6th electron onto the qubit dot. There is now a distinct difference compared to the stability measurement shown in Figure 6.9a: While in both measurements the two Coulomb-blockade lines of the SET sensor trend from the bottom right towards the top left in the stability measurement recorded using gate B2, the slope of the charge sensing lines has the same slope as the Coulomb blockade lines of the sensor. This dependence is well understood and already explained by gate cross-coupling in the concepts section of this thesis in 2.3.2. Counter intuitively, we observe a slope of the charge sensing lines with opposite algebraic sign compared to the sensor lines in the measurement shown here, recorded using the remote gate B3. The difference in the sign of the slopes cannot be explained by gate cross-coupling and will be discussed in the following.

We start with a quick repetition, why a line in the measurement - independent whether it is a Coulomb blockade of the sensor or a charging line of a qubit transition - has a slope in such a 2-gate stability measurement.
A sensor Coulomb blockade line indicates a current flow through the sensor, which is allowed when a discrete sensor dot state is tuned into the source-drain bias window. Increasing V_{B3} in Figure 6.10a will now slightly lower the respective discrete sensor dot level via its cross-coupling on the sensor dot. To keep the level in the bias window requires a reduction in a second gate voltage, for example V_{P1} which also couples capacitively on the sensor dot energy level via cross-coupling. Therefore the sensor lines appear with a formally negative slope in the stability measurement.
A charging line typically emerges, when the next higher electron level N of the qubit dot is aligned with the Fermi energy of the reservoir. To keep the alignment despite the gate cross-coupling, an increase in one gate voltage demands a reduction in a second gate voltage, typically also leading to a negative slope of the charging line in a stability measurement of the qubit charging state.
The measurement in Figure 6.10a now reveals charging lines with positive slope: We observe that, when increasing gate B3, also the second gate P1 has to be increased to have the respective quantum dot level aligned with the reservoir Fermi energy.
Figure 6.10b sketches two potential and Fermi energy configurations along the N=1 charge sensing line for a lower and a higher value of the B3 gate voltage. Independent of the slope of the charging line, the transition forms when the qubit level is aligned with the reservoir Fermi energy. When increasing both gate voltages, the N=1 dot level is lowered in chemical potential as indicated in the figure. The potential lowering is dominated by the P1 increase, but also supported via cross-coupling by the B3 gate voltage increase. To maintain alignment with the Fermi energy of the reservoir would require that the Fermi energy is lowered as a consequence of the gate voltage increases. However, if the reservoir along the channel right of the qubit dot was a real 2DEG, lowering the chemical potential by increasing V_{B3} would not lead to reduction of the Fermi energy, as the Fermi energy of the 2DEG would be set by the potential of the Ohmic contacts. Consequently, we interpret the observation that there is no real 2DEG inside the channel. This interpretation does not provide a final answer, whether the reservoir has a zero-dimensional and discrete DOS or an one-dimensional DOS, with subsequent levels with a $\frac{1}{\sqrt{E}}$ dependence.
The interpretation that no real 2DEG is formed within the reservoir is further verified, when investigating the top right corner in Figure 6.10a for B3 voltages above 1.2 V. In this voltage configuration, the charging lines start to fizzle and moreover, the separation of the N=2 and the N=1 charging line decreases. We interpret both these observations as a result of a lowering of the tunnel rate between qubit and reservoir. This interpretation again is

at first glance counter intuitive, as increasing voltages typically leads to a lowering of the surrounding chemical potential and thereby also a lowering of the tunnel barrier via cross-coupling of P1 and B3 on the tunnel barrier underneath B2. A decrease in the tunnel rate can however again be explained by the sketch in the lower panel of Figure 6.10b, but only, if indeed the Fermi energy of the reservoir is lowered following the gate voltage increase and hence is not continuous: Then reservoir Fermi energy and the qubit dot level are pushed lower in energy and as the tunnel barrier is only slightly lowered via cross coupling, the tunnel barrier effectively becomes wider and higher.
The observation that the reservoir from the right side does not have a continuous DOS, is further supported by a complementary measurement, recording a stability diagram of the qubit dot with gate B5 in which the charging lines also show a positive slope. The measurement is not shown in this thesis.

Tunnel rate tuning

As a last characterization of the reservoir on the right-hand side of the qubit dot we analyze the tunability of the tunnel rate between qubit and reservoir.



(a) **(b)**

Figure 6.11: Tuning of the Tunnel rate. **(a)** Charge sensing of the N=1 transition in the sensor current Coulomb blockade. **(b)** Averaged current measurement of a two-phase single-shot pulse sequence of unloading and subsequently loading the qubit dot.

The charge sensing of the N=1 transition is shown in Figure 6.11a, which shows the sensor current as function of the qubit dot plunger gate voltage offset at gate P1. The figure shows the right half of a Coulomb peak of the sensor for P1 voltages between [-5,0] mV. Around 0 mV we observe a sudden increase of the sensor current and from [0,5] mV we again

measure the right half of the same Coulomb sensor peak. We interpret the measurement, that around 0 mV P1 plunger gate offset the N=1 charging of the qubit occurs.
To determine and tune the tunneling rate, we apply the 2-phase pulse in Figure 6.11b: We apply an unloading pulse of about -5 mV for 50 ms which tunes the qubit into the N=0 configuration. Subsequently we apply a +0.2 mV offset pulse for 150 ms, which brings the N=1 qubit level just below the reservoir Fermi energy. The figure shows the averaged and median subtracted current of 1000 repetitions of this pulse sequence. In the measurement we identify the two different voltage pulses, but we also observe an exponential increase of the current at the beginning of the unloading and the beginning of the second phase. At the beginning of the unloading phase the qubit is occupied and the electron leaves the qubit, while at the beginning of the second phase, the qubit is unloaded and an electron will occupy the qubit dot leading to a current increase. Although this measurement cycle is a single-shot measurement, so one single step occurs in the current for the unloading or the qubit loading, in the averaged signal here, the individual peaks sum up to the exponential curve. For the tunnel rate at the beginning of the second phase, we fit about 6 ms. We do not observe big differences in tuning the tunnel rate, when using the reservoir from the right-half of the device to loading the qubit using the SET as reservoir. We can control the tunnel rate from below 100 µs up to multiple seconds.

To summarize the device tuning, we observed that loading from the right reservoir turns out more promising for single-shot qubit operation, although no pure 2DEG could be accumulated. Nevertheless, we did not observe discrete reservoir states like for using the sensor dot as reservoir. The right reservoir provides at least a certain transition voltage, which we can employ for qubit initialization and readout measurements instead of a voltage window as given by the SET reservoir.
A slightly different result has been observed in the Master's thesis of Mats Volmer [117] in a device with similar gate layout. The author observed discrete steps in the charging line when the reservoir was brought through the channel under the Px and Bx gates, similar to the results presented here for the 0D SET reservoir. A possible explanation for the qualitative difference may be lower accumulation voltages on P2-B5 along the channel and hence a formation of unintentional quantum dots along it. There is a third study by Dr. B. Klemt [118], which also demonstrated additional tunneling events beyond the N=1 qubit transition.

6.2 Single-shot spin readout via spin-dependent tunneling to low-dimensional reservoirs

We now turn towards single-shot control of the qubit. In the last section we already observed from the qubit tuning that using the SET sensor dot as reservoir to load and unload the qubit seems challenging due to the discrete DOS of the SET. In fact, we tried to implement single-shot readout and control of the N=1 electron of the qubit when the SET was still used as a reservoir. In that attempt we could not separate spin signal in the spin-to-charge conversion readout from additional tunneling events that we already observed in the stability diagram in Figure 6.7. Nevertheless, tunnel-based readout using a dot as reservoir in general is not impossible as demonstrated for example by Pla [73], however using a different qubit implementation based on a single donor atom in a semiconductor environment.
In this chapter we now test the capability of single-shot spin-to-charge conversion of the device (as introduced in section 2.3.3), while using the reservoir from the right side. For the spin readout we tune the two Zeeman split qubit dot levels such, that the spin down level is below the Fermi energy of the reservoir during the readout, while the spin up level is energetically above. Hence, we expect a spin down electron to reside on the qubit quantum dot during readout, while we expect a spin up electron to tunnel off the quantum dot and to be subsequently replaced by a spin down electron from the reservoir.

For the implementation, we start by applying a magnetic field of 2 T and tune the qubit again to the last electron. We tune the tunneling rate to a value between 3-10 ms to not be limited by spin relaxation during our readout. We expect the relaxation constant to be an order of magnitude longer [58] than this adjusted tunnel rate. Faster tunneling rates eventually become hard to measure, as the signal during the readout becomes shorter accordingly and eventually we end up being limited by our ADC in combination with post-processing procedures like averaging and filtering of the data (see Appendix A.3.6). For the tuning of the tunneling rate, we only focus on the rate during the qubit readout, as we know that for both, loading and unloading the qubit, the level alignment is detuned by several meV. For both these configurations tunneling turns out much faster compared to the configuration of the readout in which we energetically align reservoir and dot [75].
From previous efforts we have already observed, that the readout fidelity of the spin-to-charge conversion is prone to the exact alignment of qubit energy and reservoir, which might be the most delicate parameter for the readout procedure. Therefore, we introduce two measurements in the following, that allow the precise adjustment of the level alignment between reservoir and qubit during the readout.

6.2.1 Adjusting the readout position and first spin to charge conversion

For both these measurements we build our single-shot spin readout sequence out of three consecutive phases, as already introduced in section 2.3.3. We first unload the N=1 electron from the qubit and apply a loading pulse, during which an electron of arbitrary spin orientation is loaded onto the qubit dot. At the start of the third phase, which constitutes the readout measurement, the qubit hence is occupied. If a spin down electron was loaded before, no tunneling occurs during the readout, while if a spin up electron was loaded, it eventually will tunnel off the qubit and is replaced by a spin down electron from the reservoir.

Time-line measurement

A rough but fast measurement to determine the readout voltage is, to repeatedly apply this three phase pulse (unloading-loading-readout) and vary the qubit plunger gate voltage during the readout phase step-wise in between consecutive pulse sequences. The amplitudes for the unloading and the loading pulse have not been optimized here. We choose for an amplitude of ±5 mV, centered around the varied value for the readout voltage. The pulse signal, which is defined by the AWG, is added to the DC voltage at gate P1 as explained in section 3.3.3. Optimizing the loading amplitude is possible and introduced in the next section. By using ±5 mV we ensure loading and unloading of the qubit.
For determining the best alignment of spin states and reservoir, we repeat this 100 ms long pulse sequence and vary the offset voltage in between two consecutive pulse sequences. The first 19 ms of each measurement constitute the unloading phase, followed by 2 ms of qubit loading and a 79 ms readout phase. The differences in duration arise because tunneling during the unloading and the loading is much faster than during the readout. For the loading phase we moreover try to be as fast as possible to not be spin-relaxation limited in the detection. A detailed series varying the loading time is given in section 6.2.3.
The sensor current during the single-shot measurements is plotted in Figure 6.12. For each single shot measurement the median current is subtracted. Along the time axis of the figure we can distinguish the three phases of the single-shot sequence. In the unloading section the sensor is not very sensitive for the detection of electron tunneling events and the unloading is barely visible at the beginning of this first phase: A dark blue color (no current) corresponds to a loaded qubit and a lighter blue color (very few current) is measured when the electron has tunneled off the qubit dot. Notably, there are no tunneling events in the second half of the unloading phase and the sensor current remains in light blue, assuring that the qubit dot is empty at the beginning of the loading phase. In the

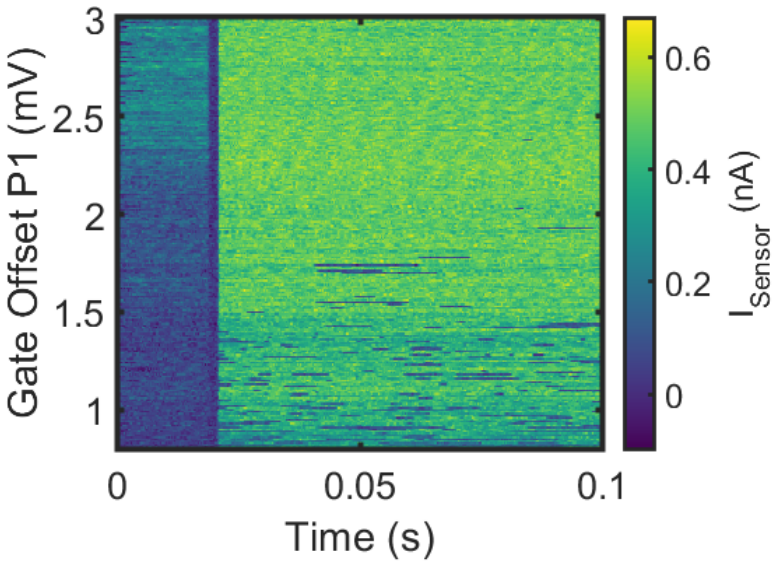


Figure 6.12: Time-line measurement. Repetition of the three-phase pulse sequence while varying the readout voltage between consecutive measurements. The voltage applied during the readout is equivalent to the "gate offset" axis.

loading phase the sensor indeed is completely insensitive, so we do not measure any current here. The readout section in the figure is the right green fraction of the graph. During the readout, we expect a current of about 0.4 nA when the qubit quantum dot is occupied by an electron and a lower value around 0 nA when it is empty.
We now look at the different gate offset voltages during the pulse application, which we varied to perform the spin-to-charge conversion at different readout voltages. We observe three different sections of the graph: For gate offset voltages above 2 mV, the qubit dot stays occupied during the whole readout phase. Reducing the gate offset to a value in between 1.5-2 mV, we eventually observe a single electron tunneling event during the readout phase. Not every single shot measurement does feature such a single tunneling event. Below 1.5 mV offset, there are multiple tunneling events within one single-shot measurement.
We interpret the absence of electron tunneling events during the readout for the largest offset voltages here as tuning both Zeeman split levels below the Fermi energy of the reservoir during the readout. Hence, independent of the single electron's spin orientation, no tunneling is energetically allowed during the readout phase. The ideal range in this experiment is found at a gate voltage of about 1.5-2 mV. In this interval, single tunneling events during the readout indicate, that only a spin up electron can leave the qubit during

the readout and is subsequently replaced by a spin down electron, which then can no longer leave the qubit again. We interpret the single-shot traces within this gate interval, in which no tunneling is detected, as spin down electrons being loaded during the loading phase. In the third section for gate offset lower than 1 mV, multiple tunneling events during a single measurement trace can be detected. Here we interpret that the readout offset voltage is too low, such that both, the spin up and the spin down level are tuned either above or even approximately aligned with the reservoir Fermi energy. Hence, independent of the spin orientation, an electron can tunnel off the qubit at the beginning of the readout. Once it eventually gets replaced by an electron from the reservoir, this electron again can tunnel off the qubit.

Fidelity measurements

This time-line measurement is quite fast (few minutes) and does not require refined post processing of the data. Hence the measurement is quite simple to implement, but the result gives only a qualitative estimation of a gate voltage interval, in which single-shot readout is in general possible. It does not provide further insight for example about the fidelity of the single-shot readout.
We now introduce a second method that allows on the one hand a more precise adjustment of the readout voltage and on the other hand also a quantitative measure of the error rate of the single-shot readout. This measurement is more time consuming and does require post-processing of data in comparison to the time-line measurement. A technique to digitize and automatically detect tunneling events from the readout sensor signal is given in the appendix A.3.6 and in [119]. We call this second measurement the fidelity measurement which looks as follows: We apply the normal three-phase pulse sequence of unloading-loading-readout of the qubit. The readout phase for this measurement is now set twice as long however. The idea of the measurement is that we perform two qubit spin readouts during the twice as long readout phase. In the first half, we expect a mixed spin signal due to the preceding unloading and random initialization of the qubit. We also know that after spin to charge conversion the qubit ends up with a spin down electron loaded. Therefore, during the second half of the readout phase, when we perform a second spin readout, we expect no electron tunneling. Any signal we measure during the second half of the readout phase hence is faulty.
Figure 6.13 shows the result of such a fidelity measurement. The figure shows two graphs, the purple curve illustrating the single-shot spin up detection rate during the first half of the readout phase when a mixed spin signal of spin up and spin down orientation was loaded onto the qubit, while the blue circles show the percentage of spin up detection during the second half of the readout phase. The two data points for each readout voltage are the average detection rate of 1000 single-shot measurement sequences.

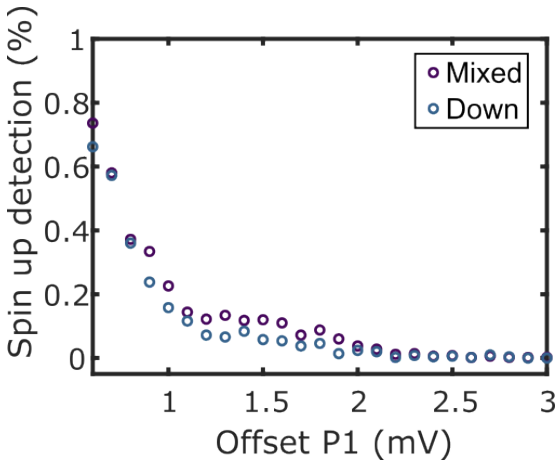


Figure 6.13: Fidelity measurement. The two data points for each readout offset voltage illustrate the rate of detecting a spin up signal in a single-shot measurement sequence during the first half of the readout phase, when a mixed spin signal is expected on the qubit dot (purple) and during the second half, when only a spin down orientation is expected on the qubit dot (blue).

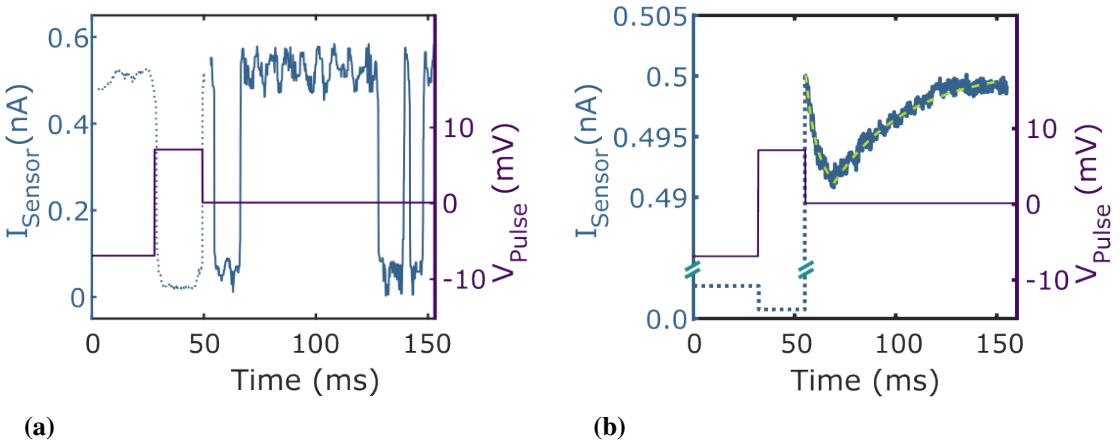
Similar to the time-line measurement, we can divide the fidelity measurement in Figure 6.13 into three sections. For gate voltages below 1 mV we do not observe a significant difference in the single-shot spin up detection rate for the mixed and the pure spin down measurement. Note, that the blue curve detecting spin up signal, when only the spin down orientation is expected on the qubit dot, gives directly a measure for the false spin up detection rate. So we interpret that for a readout voltage below 1 mV at the qubit plunger P1, there is a very high false counting of spin down traces as spin up, up to more than 70%. We also observe that here we cannot distinguish real spin up single-shot measurements from the large amount of false counted spin down traces for this readout voltage interval. In the second section, extending from about 1 mV readout offset voltage to about 2 mV, we observe a true difference in the spin up detection rate between both curves. We identify a spin up detection rate above 15 % while the false counted spin rate is below 10%. This difference allows us to distinguish real spin related electron tunnel events from false-identified ones.
In the last section above 2 mV readout voltage, both curves match again and reach a value of a few percent. In this last regime, we again cannot detect real spin-related tunneling events and we identify every count in the single-shot measurements as a false count. So for operating the qubit dot and performing single-shot spin readout we recommend to use a readout voltage offset of about +1.5 mV here. We also note, that the fidelity is comparatively small. In a similar single-shot measurement sequence performed on the depletion type sample in

my Master's thesis, we observe a difference of both curves as large as 20%. A discussion on the worse measurement fidelity is given in the ensuing section. We note, that we adapt similar tuning and measurement concepts compared to the readout of the spin during my Master's thesis. Therefore, we suspect the origin of the large fidelity difference either in the device tuning or the device geometry with the lack of a continuous DOS in the reservoir.

Besides the quantitative classification of the single-shot spin readout here, we can now use this measurement technique to optimize the load and unload depth. Once the optimal readout voltage offset is set, the difference of the detection rate measured for the "mixed" and the "only spin down" traces can be monitored and the three-phase pulse sequence can be modulated until the difference is maximized. Here, we do not find a significant variation for the load and unload amplitudes in the interval of V_{load}-V_{unload} = 10 mV to 18 mV. We performed a detailed study of this readout fidelity as function of the loading voltage depth in my Master's thesis [75]. At the used voltage here of typically 18 mV peak-to-peak we expect to load into all spin up states during the loading phase.

6.2.2 Fidelity evaluation of the spin readout via reservoir tunneling

In the fidelity measurement of the previous section we observed two differences in comparison to data from my Master's thesis: A low spin up detection but also a large false-counting rate. Here, we will look at both, the low spin up detection rate of about 15% and the high error rate, which was as large as 10% of the spin down traces identified as spin up. These two values compare to a value of 25% spin up detection rate and a considerably lower error detection rate of only 1-2% measured in the mentioned sample with depletion gate architecture during my Master's thesis. We want to note, that the low spin up detection rate itself may not pose a challenge. A low spin up rate may stem from the random qubit initialization which is not desired for the long-term qubit operation anyway. However, the large false-counting of spin down traces does indeed pose a challenge. We identify the large error detection rate to be mainly caused by the appearance of multiple tunneling events within a single single-shot readout. An exemplary trace featuring three electron tunneling events within a single readout phase is shown in Figure 6.14a.
The figure shows the sensor signal during a single-shot spin measurement cycle. Within the first 50 ms of the measurement the first two phases can be observed: A 25 ms unloading pulse and a 25 ms loading pulse. As the sensor was not sensitive for these two phases, the current measurement is only sketched with dashed dots here. In between



(a) **(b)**

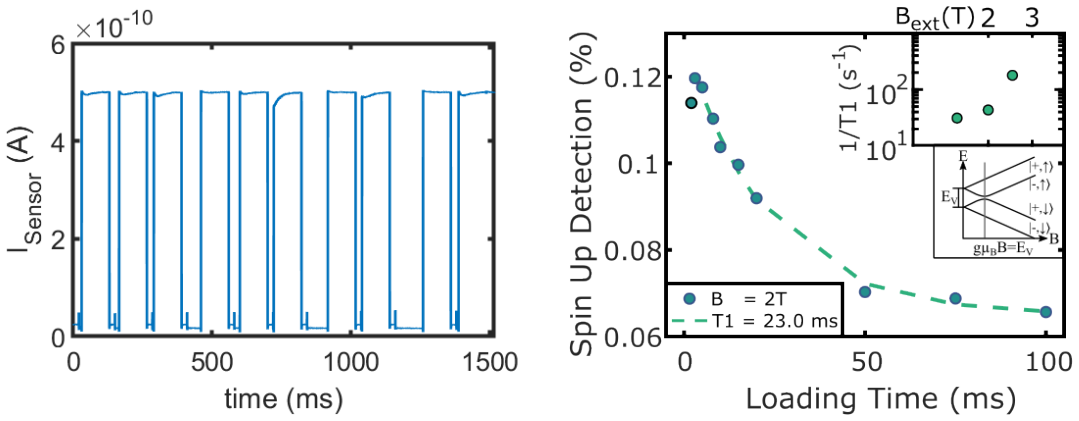
Figure 6.14: Appearance of multiple tunneling events during a single readout phase. **(a)** Exemplary readout trace of a single-shot measurement sequence. **(b)** The averaged signal of 20.000 single-shot measurements allows to identify spin-related signal.

50-150 ms of the measurement cycle, the spin readout is performed. In the exemplary trace presented here, we observe one isolated spike of the sensor signal at the beginning of the readout window for which the sensor current drops by 0.5 nA and increases after about 10 ms. We interpret this spike as stemming from the tunneling of a spin up electron, which was loaded during the loading phase. After 10 further milliseconds, it is replaced by a spin down electron from the reservoir. The measurement however shows two further tunneling events towards the end of the readout phase. This is not expected as tunneling should be prohibited energetically for the now loaded spin down electron. Thermal excitation of the spin orientation alone is not likely as the Zeeman splitting at two Tesla is much larger than the electron temperature in the device (see A.3.1).
We assume that such additional blips appear with a random distribution along the readout window while spin-related electron tunneling preferably occurs at the beginning of the readout. To analyze this occurrence, we repeat the readout sequence 20.000 times. The averaged sensor signal is shown in 6.14b. The truly spin up related tunneling leads to a double-exponential blip at the beginning of the readout phase: The averaged current decrease due to the spin up electron tunneling off the qubit dot and the ensuing exponential increase is caused by electron replacement with a spin down electron from the reservoir. We can fit both edges of the averaged blip with exponential functions and deduce the two tunnel rates of $\tau_{\Uparrow} = 5.6$ ms and $\tau_{\Downarrow} = 36.2$ ms. A similar difference in the tunneling rates of spin up and spin down has already been observed in a sample with a 2D reservoir [75, 119]. Interestingly, the random distribution of additional blips averages over the whole

readout and only appears in the form that the equilibrium current towards the end of the readout window is slightly lower compared to the starting value, immediately after we ensured single electron occupation in every single-shot measurement after the loading phase. But this separation of true spin up signals and additional blips presented in Figure 6.14b does only work for averaging of the single-shot measurements. Within a single single-shot experiment, the emergence of additional blips lowers the readout fidelity, giving a false-counting rate as large as 10%.
Tracking the origin of the emergence of so many additional tunneling events turns out challenging. When loading the qubit from the SET, we derived an explanation for additional tunneling events which was given in Figure 6.7. Using the reservoir on the right-hand side of the qubit now, we concluded from the stability diagram and the tuning procedure, that the DOS not necessarily showed a pure discrete zero-dimensional character, but we already identified that it was not continuous like expected for a perfect 2DEG.
Similar observations have been measured in the study of Klemt [118], in which a high false-counting of spin down traces with an error rate of 9% was reported. The author explained the large error rate by discontinuities in the density of states of the reservoir, but did not specify his interpretation further. Here we want to note once more, that there is another study by Pla [73] in which he demonstrated single-shot readout via spin-dependent tunneling to a reservoir with discrete DOS, however measured in a different system and by using a single donor atom and its electron as qubit implementation.
To end this fidelity discussion we want to look at the comparatively low spin up detection rate measured here. A possible explanation may be the finite switching time between the unloading and the loading phase in our setup in combination with the earlier accessibility of the spin down state during the loading phase. If the tunneling rate is on the same order of magnitude as the finite pulse ramp, the spin down state may be significantly longer available before the spin up state during the loading, leading to this spin down and spin up imbalance. We do not have a good means to characterize the loading rate yet, as it is much faster than the tunneling rate during the readout and typically the sensor is not tuned sensitively for the loading phase. A discussion on the pulse ramp is also given in the appendix of this thesis in A.3.4. Moreover, we know from [120] that the spin-dependent tunneling rate depends on the level alignment during the loading phase, which we however could not optimize here, once the fidelity measurement was implemented.

6.2.3 T_1 measurement

The single-shot spin up detection rate also depends on the length of the loading pulse: The longer we maintain the loading pulse amplitude, the more likely a potential spin up electron relaxes to a spin down electron once it has tunneled onto the qubit.



(a) **(b)**

Figure 6.15: Measurement sequence to determine the spin relaxation constant T_1. (a) A three-phase pulse sequence featuring 10 intermixed loading pulse duration lengths. **(b)** Extraction of the spin up detection rate for the different loading pulse durations. A fit to the data results in a relaxation constant of 23 ms. The measurement point for 2 ms is excluded from the fit.

In this section we now use that relation to determine a value of the spin relaxation constant T_1. We keep the three phase pulse sequence (unloading, loading, readout), but now we vary the time of the loading phase. We apply a magnetic field of 2 T and form a sequence of intermixed loading times which we repeat 20.000 times. The loading pulse durations are (10, 15, 5, 50, 20, 2, 75, 3, 100, 8) ms. The averaged sensor signal is shown in Figure 6.15a. For all but the longest two load times we observe the previously discussed double exponential blip during the readout sequence indicating significant spin up signal in the measurement. For the shortest two loading times, the qubit dot appears badly initialized as at the beginning of the readout phase the current increases, indicating that the dot was not loaded in every single-shot measurement due to the too short loading phase. For the analysis of the spin relaxation, we digitize the individual single-shot measurements and determine the fraction of measurements in which we detect electron tunneling during readout. This curve of the detection rate for different loading durations is shown in Figure 6.15b. Indeed, we observe the expected decrease in the detection rate with the increase in the loading pulse duration. By fitting the curve by an exponential function, we observe a relaxation constant of T_1 = 23 ms. Due to the bad initialization we excluded the data point at 2 ms loading time from the fit.
Similar to the fidelity measurement presented in the previous section, we observe that the fitted rate converges to a value between 7-8% spin up detection rate for long loading times. Again we do not expect any spin up signal to be measured for loading durations exceeding

100 ms ($\exp(-100\,\text{ms}/23\,\text{ms}) < 1.3\%$), so we again face a significant false counting rate of spin down traces, potentially caused by additional tunneling events during the readout phase.

A single value of T_1, here measured at 2 T, is not very meaningful as the relaxation rate critically depends on the size of the magnetic field [58] and the relaxation can become very fast, when the Zeeman splitting matches the intrinsic valley splitting. A sketch of the energy level diagram as a function of the magnetic field is shown in the lower insert in Figure 6.15b. Typical values of the valley splitting range from 10-200 µeV, hence we assume that for the value of 2 T we are above the relaxation hotspot, while typically a qubit operation below the hotspot is desired.
We implement the measurement of the relaxation constant for different magnetic fields. The data of three measurements are plotted in the upper insert of Figure 6.15b. A measurement of lower magnetic fields than 1.5 T was not possible in our experiments. We assume, that due to the smaller Zeeman splitting in combination with the non-continuous DOS in the reservoir, no spin dependent tunneling could be resolved in the single-shot spin readout and the already low readout fidelity becomes overlaid by the appearance of too many non-spin-related tunneling events.
In our sample we expect a valley splitting of $10 \leq E_V \leq 70$ µeV, measured in the Master's thesis of Mats Volmer [117] on a sample from the same heterostructure. The author used a spectroscopy technique called "magneto-spectroscopy" that does not rely on single-shot measurements and is described in his thesis in detail. From this estimation of the valley splitting we expect to be in the phonon dominated branch of $1/T_1(B)$ above the valley mixing hotspot, which may explain why the spin relaxation is faster compared to the values at the same magnetic field in the depletion type architecture in [58, 75].
We also tried to implement a third spectroscopy measurement, called "pulsed-gate-spectroscopy", but were not able to resolve the valley splitting. The measurement is shown in the appendix of this thesis in A.3.5.

6.2.4 Summary and outlook

In this chapter we put a qubit device into operation, electrostatically tuned an electron reservoir, a sensor dot as well as a qubit quantum dot. We adjusted the tunnel coupling of qubit dot and reservoir, depleted the qubit dot to the last electron and performed the first single-shot spin to charge conversion at the University of Regensburg.
We conducted the study, given the fact that in recent years the design of qubit devices trended from a so-called depletion architecture towards accumulation-type devices. During that change, large 2D reservoirs for electron exchange with the qubit dot were replaced by either a 1D channel or even a 0D sensor dot to load and unload the qubit dot. Many

of such new prototypes worked excellently, showing high single- and two-qubit gate fidelities. However, an in-depth study of many consequences of this change regarding for example the Fermi level alignment or single-shot readout fidelities for the Elzerman-type spin-to-charge conversion [84] was lacking.

Here, we performed such a study, revealing coincidental tunneling events between qubit dot and 0D or 1D reservoir, caused by a discrete or at least not-continuous density of states in the electron reservoir. Such stochastic tunneling events during the single-shot spin readout in combination with a rather low valley splitting of 10-70 µeV and low spin-up initialization of the qubit dot led to a low spin-up detection rate at a maximum of about 15%. By tuning the device to host a 1D like electron reservoir, we demonstrated single-shot spin readout by spin-dependent tunneling to a electron reservoir for three magnetic fields. We measured a spin relaxation constant T_1 up to 35 ms, potentially limited by phonon-mediated spin-orbit mixing. We only performed T_1 measurements for magnetic fields above the valley splitting hotspot. A relaxation constant measurement for magnetic fields below 1.5 T was not possible due to the limited readout fidelity.
As the readout via spin-dependent tunneling to the reservoir turned out quite challenging, we recommend tuning the device to feature a double qubit dot system and performing Pauli spin blockade for the spin readout. The low spin-up initialization can be compensated by spin driving for example in a magnetic field gradient via EDSR. Finally, magnetospectroscopy may turn out as superior measurement of the valley splitting, as its implementation is comparatively straightforward and the technique does not rely on single-shot experiments.

7

Charge noise power spectral density

Extending the discussion of improving the single-shot spin readout detection visibility and accordingly the measurement fidelity, the question about potential limitations of single and two-qubit gate operation fidelities may be raised. The debate of improving these gate fidelities is a currently much discussed topic, for example in the context of quantum error correction.
According to the current state of research [5, 59, 121] gate operation fidelities are limited by charge noise which is a term that covers temporal electrical field or potential fluctuations.

In this chapter, we use measurements of the current through a SET sensor dot to characterize the footprint of this charge noise. After tuning the SET on a sensitive edge of a Coulomb blockade peak, a slight variation in the electrostatic potential (charge noise) results in a measurable variation of the conducted current. Complementary, when the SET is tuned into blockade and no current is transported, all fluctuations in the measurement signal can be attributed to the measurement equipment subsequent to the non-conducting sensor dot. Hence, such a measurement of a blocked sensor dot constitutes a characterization of the noise floor of the setup.
As the origin of charge noise and strategies of its mitigation in quantum processor devices are not fully identified up to date, in this chapter we aim to extend the existing charge noise studies with measurements in our accumulation-mode devices that we introduced in the preceding chapter.

7.1 Calculation of the power spectral density

We record noise spectra by measuring the current through the sensor of the quantum processor device. We set the sampling rate to $f_S = 2{\cdot}10^4$ samples/sec and typically record for 1000 seconds. For the calculation of the power spectral density (PSD), we perform a fast Fourier transformation of the current signal I(t) and normalize the squared result by dividing by the sampling frequency and the total number of measurement points N. To account for having only a single sided spectrum we multiply by factor of 2:

$$S(f) = \frac{2 \cdot |\, \mathrm{FFT}(I(t))(f)\, |^2}{f_S \cdot N} \tag{7.1}$$

This definition follows [121]. The calculation provides a PSD in units of A^2/Hz. Conversion into gate equivalent noise is given by normalizing the spectrum by the slope of the Coulomb peak $\frac{\delta I}{\delta V}$ and further conversion into chemical potential noise is given by multiplication with the respective gate lever arm, which can be calculated from a Coulomb diamond measurement with the two slopes $m_- = m_D$ and $m_+ = m_S$ following [83, 122, 123] with the formula:

$$\alpha = \left| \frac{m_S \cdot m_D}{m_S - m_D} \right| \tag{7.2}$$

So the final PSD conversion follows:

$$S_\mu = \frac{S(f) \cdot \alpha^2}{\left(\frac{\delta I}{\delta V}\right)^2} \tag{7.3}$$

This noise amplitude is more universal as it does not depend on the potential tuning of the device. As the conversion is linear it does not change the spectral course of the noise amplitude as a function of the frequency.
We typically record a spectrum 10 times and average the spectra. No peaks as well as no background are subtracted and we also do not make use of a windowing function.

7.2 Analyzing the noise floor

We begin the noise characterization by analyzing the noise floor of the dilution cryostat setup that was set up during this PhD project. Here, we focus on the current readout measurement equipment. The appendix of this thesis (see A.4.1) shows the impact of

the cryostat filter installation by comparing two PSD spectra before and after the filter installation.
In the analysis of the I/V-converter pre-amplifier in section 3.4 we concluded that the noise amplitude is decreased by increasing the amplification factor. We also made a consideration about the maximum amplification stage due to limited input voltages of digitizer and differential amplifier.

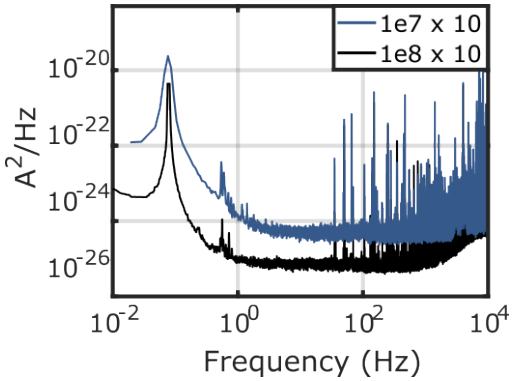


Figure 7.1: Noise floor measurement for different total amplification settings.

In section 3.4 no sample was connected to the readout line. Here, the same device as presented in the measurements throughout the previous chapter 6 is cooled in the dilution cryostat setup. We tune the sensor into current blockade and consequently attribute any fluctuation in a current measurement to be picked up from the measurement environment. We refer to such a measurement of the Coulomb-blocked sensor as insensitive measurement and term the noise amplitude the noise floor or PSD baseline. Figure 7.1 shows two spectra recorded in such a blocked transport regime. The blue curve was recorded using our normal amplifier configuration with a total current amplification of $10^7 \cdot 10$. The black graph is a measurement of the noise floor with an increased amplification of $10^8 \cdot 10$, which limits us to a maximum current of 10 nA through the sensor, which is of course not reached for the current measurement presented here. We now make three observations: First, in both graphs there is prominent peak around 70 mHz, which was not present in the noise spectra of solely the amplifier in section 3.4. From systematic tests, we assign the origin of this peak to the cold head as part of the cryostat pulse tube pre-cooling. Note, that the cold head was off in the discussion in section 3.4. We are currently in communication with the cryostat manufacturer to suppress this unwanted source of slow noise. Secondly, we observe that for frequencies above 1 Hz the noise amplitude terminates in a minimum value that we identify as the noise floor baseline. We attribute the deviation from the noise floor towards 10 kHz to the bandwidth limit of our DC lines and the lowpass filter of the current amplifier. A third observation we make in

the measurements is that the courses of both graphs resemble and that the black curve, that was recorded using a 10-fold higher amplification factor, has an about one order of magnitude lower noise amplitude. While the noise baseline for our regular amplifier setting (blue curve) amounts to a value slightly lower than 10^{-24} A^2/Hz, the black curve falls as low as 10^{-25} A^2/Hz. Also the peak amplitude at about 70 mHz is lowered by that one order of magnitude.

Since both spectra were recorded for a current-blocked sensor tuning, we conclude that the difference in the noise amplitude between both graphs is caused solely by the different amplification setting on the I/V-converter. As the maximum current that can possible be detected depends in the amplification factor (see section 3.4), we were restricted to apply the slightly worse setting of $10^7 \cdot 10$ in the remainder of this section, unless noted differently. We are currently investigating technical improvements in that regard.

7.3 Quantification of device-related noise: S_0(1 Hz)

As a next step, we tune the sensor to a sensitive configuration along the Coulomb blockade, in which current transport through the SET is allowed. The device as well as the Coulomb blockade transport peak is shown in the insets in Figure 7.2. The two PSDs in the figure are already converted by equation 7.3. The black graph (insensitive measurement) is the same measurement as in the previous figure. It was recorded when the sensor was not conducting, indicated by the black dot in the Coulomb blockade inset. The blue-colored PSD was recorded when the sensor was tuned to the most-sensitive configuration along the transport peak, indicated by a blue dot in the corresponding inset. We observe that this sensitive PSD equals the noise floor baseline for frequencies above around 1 kHz. In contrast to the insensitive measurement, the sensitive PSD additionally features a section for frequencies between 10 mHz to 1 kHz, in which the noise amplitude appears as linear course in the double-logarithmic scale, clearly differing from the insensitive graph. We conclude that the difference between sensitive and insensitive measurement in that frequency interval originates from the current fluctuations, measured by the sensor, and not due to for example differences in the setup like different load resistances which go into the pre-amplifier [124].
To classify and compare the noise amplitude of this measurement to other experiments, the y-scale has been converted by equation 7.3. For the comparison, oftentimes the noise amplitude measured at 1 Hz, which is denoted as S_0(1 Hz), is used. In our device and

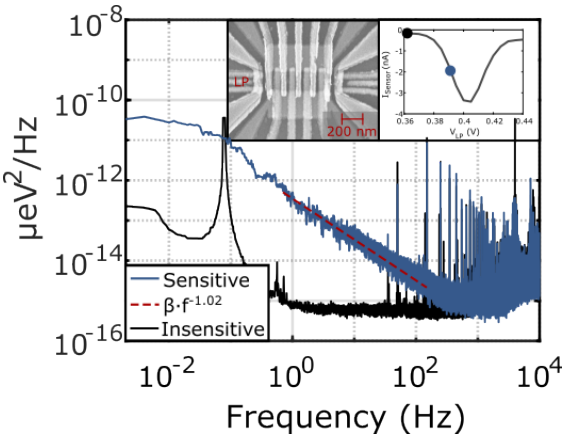


Figure 7.2: Power spectral density of current fluctuations measured in transport through the SET. The sensitive measurement (blue) was recorded with the SET tuned to the most-sensitive position along the flank of a transport peak with increased amplification $10^8 \cdot 10$. The insensitive measurement (black) was recorded with the same amplification setting, but with the sensor tuned into Coulomb blockade.

with the best possible measurement settings we determine a $S_0(1\ \mathrm{Hz})$ value of

$$S_0 = 0.64\ \mu\mathrm{eV}/\sqrt{\mathrm{Hz}}\ . \tag{7.4}$$

This marks a state-of-the-art charge noise amplitude. In comparable devices S_0 values in the range between 0.3-2 $\mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$ have been reported during the elaboration of this thesis [125]. According to the reported values, no significant differences in the charge noise PSDs have been observed in accumulation- and depletion-architecture spin qubit devices.

7.4 Discussion of sensor charge noise: $f^{-\alpha}$

7.4.1 A f^{-1} spectral dependence of the noise

For the further analysis of the sensor noise, we now focus on the sensitive PSD measurement in the frequency interval between [10 mHz - 1 kHz]. We fit the spectrum and extract a polynomial dependence $A \cdot f^{-\alpha}$ with a coefficient of $\alpha = 1.02\ (\pm 0.03)$. This fit is plotted as red dashed line in the graph. The course of the sensitive noise spectrum measurement, showing a polynomial dependence and eventually terminating in the noise

floor baseline, is characteristic for charge noise in the qubit device and has been observed in many different semiconductor quantum computing processor devices, independent of the design and flavor of the qubit implementation [5, 59, 121, 122, 125, 126].
The charge noise spectrum in any electronic semiconductor device may scale with the dependence $f^{-\alpha}$, for which the coefficient α may take a value between $1 \leq \alpha \leq 2$ [125]. A model for this dependence was first set up by A. McWhorter et al. [127] more than half a century ago. The model is applicable to many semiconductor qubit devices, like nicely exemplified in the publication by E. Connors et al. [122]. We will adapt the outline of the model in the following from this latter citation.
This model by McWhorter et al. assumes a homogeneous distribution of two-level fluctuators (TLFs) with a certain thermal activation energy E, not specifying the nature of the TLFs, which may be dangling bonds, crystal defects or dopant atoms to just name a few examples. According to the model, each fluctuator contributes a Lorentzian component to the noise spectrum at its corresponding fluctuation frequency. Integrating over all Lorentzian terms results in a f^{-1} dependence of the common noise spectrum.
This basic model is then extended by P. Dutta, P. Horn et al. [128], who ended up with the formula for the spectral dependence of the charge noise following [122]

$$S_E(f,T) = \frac{k_B T}{2\pi f} D(E) \, . \tag{7.5}$$

The complement by Dutta/Horn et al. now links the spectral dependence of the noise amplitude to the energy distribution of the TLFs D(E). A f^{-1} dependence is consequently only measured for a homogeneous distribution, both in energy and space. For a nonuniform distribution, other exponents α for the frequency dependence in between $1 \leq \alpha \leq 2$ [125] are possible.

As we fitted a clear f^{-1} dependence in Figure 7.2, that described the noise spectrum in the interval of [10 mHz - 1 kHz], we assume an uniform distribution of TLFs to be present in the device. The resulting electrical field and potential fluctuations (charge noise) may shift the SET working point along the Coulomb blockade peak resulting in the measurement of current noise. Note, that the data below 10 mHz are hardly interpretable, as the spectrum only features two more data points here.
We measured a comparable f^{-1} course of the charge noise spectrum in a second accumulation-type qubit device, that was fabricated at the University of Regensburg on a MBE grown heterostructure. The measurements of this second device are presented in the appendix of this thesis in section A.4.2. Tuning methods of the electrostatic potential were conducted by Michaela Zoth in her Master's thesis [129].
Both, our device and the one measured by Michaela Zoth used the accumulation gate

architecture, that was described in the concepts section of this thesis in 3.1.3. But also in depletion-type qubit devices a f^{-1} spectral dependence of the noise for a comparable frequency range has been reported [5, 59, 126]. It is an important observation that across many different state-of-the-art qubit devices a f^{-1} dependence of the sensor current noise has been measured recently. Two of these studies [5, 59] extended the noise analysis of the sensor current by also recording a noise spectral density of a single-electron qubit quantum dot in the respective device. Both studies reported that the qubit noise equals the sensor noise PSD and follows a f^{-1} dependence and hence identically is dominated by charge noise, caused by a homogeneous distribution of TLFs. Moreover, both studies suggest, that the PSD measured by the sensor current fluctuation also describes the qubit noise PSD.
The current question however where in the device stack such TLFs may reside and how to suppress or even mitigate their detrimental influence on a qubit device remains unclear up to date. Much discussed candidates for fluctuating two-level defect states are either assumed in the heterostructure crystal or the oxide dielectric, but also at interfaces, for example the quantum well interfaces or the oxide interface to the semiconductor. No unanimous microscopic picture has been established so far, raising the question if there are quantitative measures or parameters to benchmark the charge noise in current generation spin qubit devices.
In the literature oftentimes the $S_0(1\ \mathrm{Hz})$ value is used to compare charge noise across different qubit devices, leaving scope for the discussion whether this value can accurately characterize the charge noise. Kranz et al. [125] reported the lowest noise amplitude value of $S_0 = 0.0088\ \mu\mathrm{eV}^2/\mathrm{Hz}$ in a silicon-based qubit device. The peculiarity of the used device was that gates, qubit dot and electron reservoirs were defined by STM placement of phosphorus atoms (Si:P) in a single layer, avoiding semiconductor interfaces and allowing to bury this active layer deeply from oxide layers on top of the device. The significantly lower noise amplitude compared to other multi-gate-layer qubit devices, for which $0.1\ \mu\mathrm{eV}^2/\mathrm{Hz} \leq S_0 \leq 4\ \mu\mathrm{eV}^2/\mathrm{Hz}$ values have been reported [125], may be a first experimental hint that semiconductor/(ALD-)oxide interfaces or the oftentimes poly-crystalline oxide are especially prone to forming TLFs. Another experimental hint pointing towards the oxide hosting TLFs was demonstrated in the study by Connors et al. [122], in which an increase of the noise amplitude with increasing oxide thickness was observed.

Besides $S_0(1\ \mathrm{Hz})$ as a potential parameter to benchmark the charge noise in qubit devices, also the question arises whether the polynomial coefficient α may provide useful physical insight. The by Dutta/Horn refined model of McWhorter does not provide a clear microscopic picture in that regard and a further development of the theory in the future is very much desirable. Experimentally, values between $1 \leq \alpha \leq 2$ have

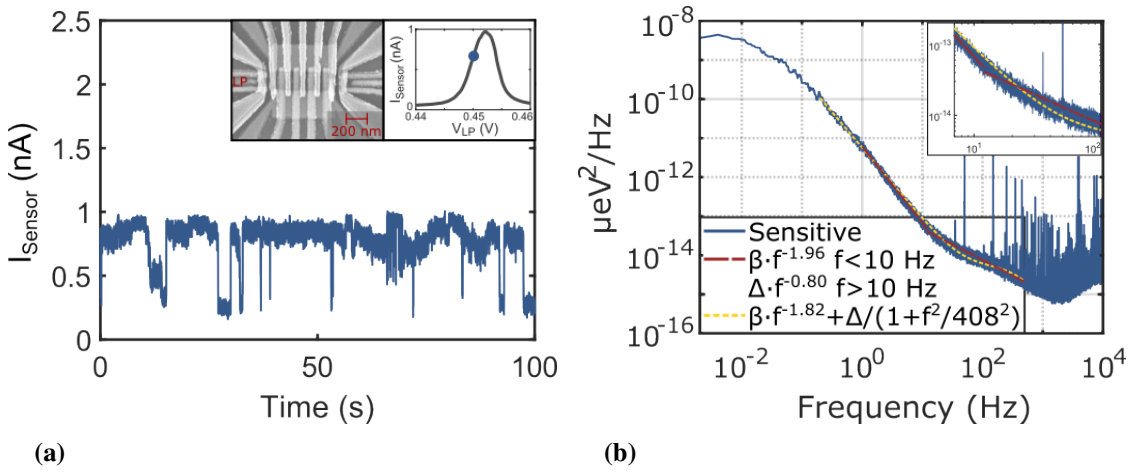
been reported [125]. Notably the Si:P device by Kranz et al., that demonstrated the lowest S_0(1 Hz) value, showed an exponent of $\alpha = 1.63$ of the noise spectrum in the frequency interval of [10 mHz - 0.3 Hz]. So despite the low noise amplitude value, the spectral exponent suggests an inhomogeneous distribution of TLFs (either in space or frequency).
In our publication (T. Struck et al. [59]), in which we presented spectra recorded by transport through a sensor dot as well as complementary noise measurements, recorded by tracking the qubit resonance frequency, we measured a f^{-1} over a very broad interval of [1 mHz - 10 kHz]. Below 1 mHz, the course deviated from f^{-1} and the exponent was fitted as $\alpha = 2$. A possible microscopic explanation is the presence of slow TLFs with inhomogeneous distribution, dominating the homogeneous TLFs for low frequencies.
Also E. Connors et al [121] used a combination of qubit and sensor noise measurements to record the charge noise over a large interval between [1 µHz - 1 MHz]. The general trend of this large noise spectrum also followed a f^{-1} dependence, but for some frequencies (∼1 Hz, ∼1 kHz), the exponent α clearly deviated from 1, as the PSD became steeper, suggesting for these smaller frequency intervals an exponent $\alpha > 1$. This observation raises the question if a deviation from $\alpha = 1$ in some frequency interval as well as a regression to $\alpha = 1$ above a certain frequency also contains valuable information. An example may be the superposition of a homogeneous TLF distribution by an inhomogeneous one, that causes the deviation within a certain bandwidth.
In out data, we do not observe such deviations from f^{-1}. Our data rather resembles our previously published data in [59]. However, we may only exclude a deviation from $\alpha = 1$ in the interval between [10 mHz - 1 kHz]. We cannot exclude a transition of the PSD to f^{-2} for lower frequencies, like observed in [59].
Generally we conclude from these observations, that the S_0(1 Hz) as well as the exponent α can provide a first categorization of the charge noise in a qubit device, but neither parameter alone fully characterizes the charge noise yet. An extension of the microscopic model would be very much desirable in that regard.

7.4.2 Gate voltage induced deviation from f^{-1}

In an earlier experimental study from our research group by Wild et al. [112] a noise spectrum of a modulation doped silicon spin qubit device was discussed. The authors determined a spectral exponent of $\alpha = 2$ and explained this observation, supported by simulations, by the presence of a non-uniform distribution of not-fully ionized donor atoms. Moreover, the authors also showed that by varying the voltage of a global TG, the degree of ionization of the donor atoms could be modulated and observed a spectral exponent of $\alpha = 1$ after full ionization. This result raises the question to what extent the applied gate voltages in a qubit device (global but also local gates, which are typically

incorporated in current-generation qubit devices) can impact the exponent α.

In Hall bar measurements, shown in section 4.1, the linear and capacitor-like dependence of the electron density in the quantum well n_{2DEG} on the gate voltage terminated for a critical voltage above which the density no longer increased. We explained this observation by tunneling of electrons towards the semiconductor to oxide interface and subsequent trapping of electrons there.
For qubit devices the impact of large gate voltages has so far mostly not been investigated. So in the following, we measure how the sensor-detected noise amplitude reacts to variations of the gate voltages.
In our experiment, the sensor current became unstable and fluctuated on a few second timescale, following a large voltage increase on all relevant sensor plunger gates. An exemplary noise trace of the sensor current at a nominally sensitive voltage configuration is plotted in Figure 7.3a. The figure shows frequent current jumps between two values on a timescale of a few seconds. The figure also shows the Coulomb blockade peak as well as a SEM image of the device as insets. Figure 7.3b shows the corresponding



(a) **(b)**

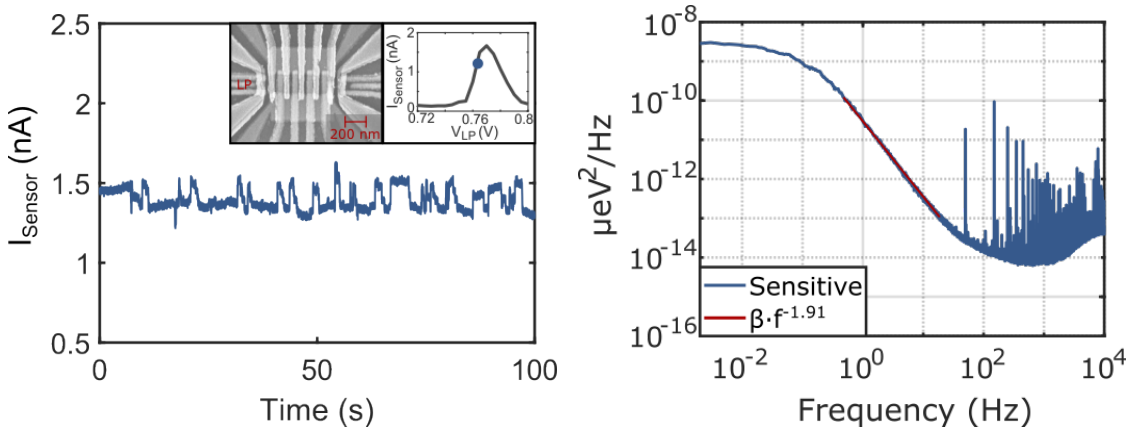
Figure 7.3: Increase of the gate voltages. (a) Measurement of the current stability for 100 s. **(b)** PSD after the gate voltage increase, showing a kink around 10 Hz.

PSD after the gate voltage increase. Indeed, the PSD differs from the measurement shown in Figure 7.2. The noise floor remains unaffected for frequencies above 1 kHz. However, the lower-frequency branch of the spectrum is no longer linear, but features a kink around 10 Hz, corresponding approximately to the current fluctuation frequency of Figure 7.3a. Moreover, below the kink the spectrum no longer follows a f^{-1} dependence.

This deviation, induced merely by a significant gate voltage increase, is a surprising observation.
According to the model by McWhorter et al., a Lorentzian spectral component is predicted for a single or a few TLFs at the switching frequency [122]. Therefore, we implement a fitting routing adding a single Lorentzian dependence at around 10 Hz, overlapping the $f^{-\alpha}$ dependence. This fit, shown as yellow dotted line in the figure, is calculated by the sum of a polynomial and this Lorentzian function. The polynomial coefficient is extracted at a value of $\alpha = 1.82$.
As this fit routine does not describe the PSD perfectly, we apply a second fit routine, following [59], as piece-wise polynomial fit below and above 10 Hz. This fit routine accounts for the observation of two different slopes in the PSD without an underlying microscopic picture. For this piece-wise fit (red dotted line in Figure 7.3b), we extract values of $\alpha = 1.96$ and $\alpha = 0.8$.
Both fit routines describe the PSD not perfectly, but we conclude that the spectrum for frequencies lower than 10 Hz clearly deviates from a $\alpha = 1$ coefficient and the spectral exponent approaches a value close to 2. We interpret the deviation from $\alpha = 1$ with the presence of an inhomogeneous distribution of TLFs following the gate voltage increase. This interpretation also comprises the presence of a single or few TLFs.
Moreover, we observe, that the noise amplitude value measured at 1 Hz increases significantly following the gate voltage increase.

With this idea in mind, we consequently further increase all relevant gate voltages in our qubit device, thereby also further increasing the risk of electrons tunneling out of the quantum well towards the semiconductor interface.
We immediately observe an increase in the current fluctuation frequency, exemplary shown in Figure 7.4a. But also in the PSD, shown in Figure 7.4b, the f^{-2} branch extends now beyond 10 Hz, here indicated by the red fit, before terminating in the noise floor baseline. This is a further indication that we indeed either create, activate or increase the fluctuation frequency of some intrinsic trap states in the device with an inhomogeneous distribution either in frequency or in space.

Note, that we have previously observed a f^{-2} dependence of the sensor noise PSD in the depletion-gate qubit device measured during the Bachelor's project of Leonie Fey [131]. At that time, the exponent of $\alpha = 2$ was not interpreted. In the context of the current discussion, the exponent might indicate that the respective sensor dot gate voltages have already been tuned into a regime in which tunneling from the quantum well towards the interface was favored.
Comparing the noise amplitude of the chemical potential fluctuation, we also observe that the value of 9.8 $\mu eV^2/Hz$ measured in 7.3b for 1 Hz increases to a value of about



(a) **(b)**

Figure 7.4: Second gate voltage increase. **(a)** Measurement of the current through the sensor. **(b)** PSD after the second gate voltage increase.

30 $\mu eV^2/Hz$ after the second gate voltage increase.

Quite recently, during the writing up of this thesis, complementary results to this work have been pre-published in L. Massai et al. [130]. The authors present noise measurements, that were recorded by tracking the Coulomb peak voltage of a sensor dot in an accumulation-type hole spin qubit device in a germanium quantum well heterostructure. By increasing the applied negative voltages they demonstrated a variation of the spectral exponent in between $1.4 \leq \alpha \leq 1.8$ in a frequency range of approximately [0.1 mHz - 0.1 Hz] and an increase in the charge noise level, which recovers slightly again on a time scale of days. Interestingly, supported by Hall bar measurements, similar to our data, the authors attribute the gate voltage induced variation to a local population of charge traps at the SiGe-oxide interface.

To conclude the characterization of the charge noise present in our qubit device, we want to discuss the impact of charge noise on the coherence of a spin qubit in the same device. We assume that a flat course of the spectrum, represented by a small coefficient α, as well as a low noise amplitude, for example given by the value at 1 Hz S_0(1 Hz), favor a lower mitigation of charge noise to the spin qubit and hence support a lower decoherence of the qubit information.
In [59] we now measured state-of-the-art T_2^*-times while observing a change from f^{-1} to a f^{-2} dependence below 1 mHz, raising the question of the impact of such low-frequency components in the noise PSD. We conclude that an increase in the polynomial power

law exponent at a certain frequency may not be limiting qubit gate operations as long as it occurs at low enough frequencies, lower than typical measurement and gate duration times [5, 59]. To give an example, we observed a dependence of the qubit dephasing time $T_2^*(t_m)$ on the measurement time t_m in [59]: The qubit dephasing constant decreased the longer data were integrated for the measurement as probably lower frequency components in the noise spectrum started to contribute to the dephasing. In many recent publications, merely a value of the qubit dephasing is reported, but a more precise statement would be to also indicate the integration time needed for the T_2^* measurement. There is a second study [5] that confirms this line of though, also reporting the $T_2^*(t_m)$ dependence.

7.5 Conclusion

In the past years in the quantum dot spin qubit community multiple studies suggested that electrical noise limits fidelities for qubit gate operations and that a charge noise spectroscopy via a sensor current measurement seems to accurately describe also the charge noise seen by the qubit electron spin [59, 121, 125]. Thereby, a sensor noise spectroscopy measurement is far more simple and straightforward to implement in the qubit experiment.
We presented measurements of the noise power spectral density measured via the current through the sensor dot. We observed a charge noise amplitude value at one Hertz of $S_0(1\text{ Hz}) = 0.64\ \mu\text{eV}/\sqrt{\text{Hz}}$ which resembles other state-of-the-art gate defined silicon spin qubit devices and measurements. We measured a polynomial dependence of the noise spectrum proportional to $f^{-\alpha}$, and measured an exponent $\alpha \simeq 1$ for a frequency interval of [10 mHz - 1 kHz] for normal tuning of the qubit device.
We extensively discussed using the parameters $S_0(1\text{ Hz})$ as well as the spectral exponent α as benchmark for the charge noise in a qubit device and recommend to always record and consider both values.
We also demonstrated a dependence of the power law exponent α on the applied gate voltages which has not yet been analyzed in that detail in literature so far. An increased voltage potential may promote the formation and switching of two level fluctuators in close proximity to the respective quantum dots for example at the oxide interface. Switching of a non-uniform distribution of a few or even only a single TLF changes the f^{-1} power law to $f^{-\alpha}$ with $1 \leq \alpha \leq 2$. Here we measured a value close to 2 after drastically increasing all relevant gate voltages. Also the noise amplitude itself did increase significantly by increasing the gate voltages.

For upcoming experiments, we recommend to record PSDs on a regular basis and to monitor both, $S_0(1\text{ Hz})$ as well as the polynomial coefficient α following a gate voltage

increase. Moreover, the investigation of local correlation of noise across a qubit device seems interesting to further develop a microscopic image of the charge noise origin [132]. In general, we recommend a conservative tuning strategy, in accordance with [130], for the operation of any gate-defined spin qubit device.

8 Conclusion

The main objective of this thesis was the investigation of components for gate-defined Si/SiGe spin qubit devices, amid the currently ongoing scaling from demonstrator spin qubit devices to large-scale fault-tolerant quantum computing. We focused in particular on the sensor of such a spin qubit device which is a pivotal component of a quantum processor. Not only is fast and high fidelity single-shot readout of the quantum mechanical two-level system the foundation for eventual quantum error correction schemes, but a low readout error rate just as well is necessary on a research level to develop a deeper physics understanding in the still vastly and dynamically advancing field of quantum computing. As one aspect in that regard we introduced a new sensor dot design in chapter 5, aiming to improve the readout signal of a capacitively coupled qubit dot by an order of magnitude compared to a standard SET-based readout. We employed a simulation based ansatz to develop a gate design that allowed a larger physical separation of the drain reservoir, reducing the capacity to the reservoir, while preserving the tunnel coupling by the introduction of a 1000 nm long potential slide. The asymmetric design of the capacitances reflects in the measurement of tilted Coulomb diamonds. By operating this new sensor not with a constant voltage but with a constant current bias, we used the tilting of the steep Coulomb diamond edge to significantly increase the sensor output signal. We introduced the asymmetry factor AS, which is the ratio of the positive and the negative diamond slope, as a direct measure of the sensor signal increase. The AS factor is inverse proportional to the drain reservoir capacity. We experimentally demonstrated a tuning of the AS factor between values of 15 to 175 by gate-induced activation of the potential slide, corresponding to a more than 10-fold reduction of the drain capacity. In complementary measurements to this thesis, performed on a GaAs-based qubit device, a similar tunability

of the Coulomb diamond edge was observed and constant current bias charge sensing was successfully demonstrated, thereby increasing the charge-sensing signal for the inter-dot charge transition of a capacitively coupled doubled quantum dot to 3 mV, also a 10-fold increase compared to the signal of a symmetric sensor dot. By linking the spin information of the qubit to the dots electron occupation (spin-to-charge-conversion) the asymmetric sensor will allow a sensitive spin-state readout of the qubit. In terms of scaling, the large output voltage swing allows to reduce the ensuing amplification requirements which will be based on classical electronics. Hence, the asymmetric sensor dot (ASD) allows easier integration of classical electronics components in the vicinity of the qubit processor also at low temperatures due to the reduced heat load from the classical electronics.
As another aspect of this PhD project, we focused on the operation of a second qubit device in chapter 6. The device featured two new characteristics compared to all previously measured qubit devices in our research group. For one thing, the device was designed very compact, featuring four serial quantum dots in a linear array and two sensor dots at both ends. Notably, the gate layout featured no 2DEG area which may have served as an electron reservoir for electron exchange with the serial qubit dots. Instead, the qubits were intended to be directly loaded from the sensor dots at both ends of the quantum dot array, so the sensor dots filled the role of the electron reservoirs. As a second new aspect, this compact device design was realized by using the accumulation-architecture gate layout, which enabled local electron accumulation on the size as small as 100 nm. We observed, that using this accumulation-architecture, both qubit and sensor quantum dots formed exactly where intended and the tuning was very reproducible for multiple thermal and subsequent cool down cycles in terms of the used gate voltages and the estimated quantum dot location. This is in strong contrast to our experiences with samples employing the depletion mode architecture, for which the suppression of disruptive additional quantum dots has turned out challenging. During the tuning of the compact qubit device, we observed a fizzling of the N=1 charge-sensed loading transition, using the left sensor dot of the device as electron reservoir. Although the qubit was energetically tuned into the N=1 regime, we measured the occurrence of multiple tunneling events, despite expecting an once loaded electron to remain confined and to not tunnel off the qubit again. The attempt of spin-to-charge conversion, by spin dependent tunneling of this last electron to the sensor dot, failed, as we could not separate the real spin signal from the detection of such additional tunneling events in a single-shot readout window, leading to a large false-counting rate. We could significantly reduce both, the fizzling of the transition line and the false-counting error rate by accumulating electrons in the whole right half of the device, forming thereby an about 100 nm wide and 500 nm long channel, which we then used as electron reservoir. We successfully recorded single-shot spin readout and determined a spin relaxation constant exceeding 25 ms. However, we still faced a large detection error rate. We estimate that from a spin up detection of about 12 %, more

than half the signal was falsely identified as spin up signal. We interpreted the result as sign that the discrete DOS of an electron reservoir is problematic, completely hindering a Elzerman-type spin readout when using the fully-discrete sensor dot as reservoir and resulting in a large error rate when using the 1D-like channel for the reservoir. While tuning the accumulation-type device appears remarkably easier, in the compact design the single-shot spin readout here turned out to be much more error prone compared to the depletion-type device that featured a 2DEG reservoir and was measured in [75]. In this reference sample, a large spin up detection rate of nearly 30% had been measured at an error rate as low as 2%, allowing to perform a relaxation constant measurement at magnetic fields as low as 400 mT, albeit the valley splitting energy had been considerably larger. For upcoming measurements in a compact qubit device we recommend to use PSB for the spin readout. For this method no alignment of the qubit dot and the reservoir is required and the readout becomes independent of the reservoir DOS.
As a further usage of the sensor dot, we employed the current measurement of the SET sensor in an accumulation-type device for a spectral analysis of the charge noise in chapter 7. We measured state-of-the-art power spectral densities of the sensor current, that featured a white noise floor for frequencies exceeding 10^3 Hz and a f^{-1} charge noise course for lower frequencies. As we set up a new dilution cryostat setup we used the PSD measurement as a tool to classify the noise floor in this setup and technically optimized the amplification and filtering strategy, yielding a state-of-the art noise amplitude in the new setup, measuring $S_0(1\ \text{Hz}) = 0.64\ \mu\text{eV}/\sqrt{\text{Hz}}$.
In the silicon spin qubit research field recently the hypothesis has been developed, that two-level fluctuators play a decisive role for the f^{-1} charge noise amplitude. We also faced such trap states at the semiconductor to oxide interface in chapter 4, which caused current instabilities in the Hall bar measurements and were significantly enhanced when increasing the TG voltage. Above a threshold, no increase in the quantum well electron density was measured which we explained by electrons from quantum well being attracted into these trap states, screening a further electric field enhancement. In chapter 7 we experimentally investigated whether such trap states also affect the electrical noise amplitude measured by the sensor dot when we intentionally increased the applied gate voltages. We observed that an initial f^{-1} power law dependence was modified into a f^{-2} branch with increasing gate voltages, which we interpreted as an evidence that also for a qubit device 2-level fluctuators may dominate the noise amplitude. Moreover, we also measured a significant increase in the noise amplitude value. We explained this gate voltage induced transformation with either the formation or the activation and enhancement of two-level-fluctuators with a non-uniform distribution across the qubit device.
These results may motivate to improve the interface and oxide quality in upcoming qubit devices, for example by incorporating high-quality MBE grown oxide or improvements to the crystal annealing procedure following the ion implantation.

A

Appendix A

A.1 Appendix - Hall bar

In the main text in chapter 4 we mostly analyzed the electron density as a function of the gate voltage and presented concepts of different electron density operation regimes which may be transferred to qubit device measurements. In the following section we focus on the electron mobility as a function of the electron density. We analyze measurements for magnetic fields up to ±12 T and observe a divergence of the longitudinal resistivity for filling factors $\nu \leq 2$ which is reached for these magnetic field strengths. We then investigate the Landau-level broadening with increasing temperature and current amplitude and end the section with a technical optimization of the 4-point measurements. All measurements are performed in the ^{3}He-cryostat.

A.1.1 Approaching filling factor ν = 2, spin and valley splitting

We begin with a study of the mobility as a function of the electron density. Figure A.1 presents a measurement series of the longitudinal resistivity for different electron densities, tuned by the gate voltage. In the measurement, the resistivity is plotted as a function of the filling factor ν. The electron density was estimated by the longitudinal resistivity minima, for which the filling factor turned out to fit more accurately compared to the calculated density from the linear transversal resistivity slope. We measure a maximal electron mobility of 47.000 cm^2/Vs at an electron density of $n_{2DEG} = 5.5 \cdot 10^{11} \frac{1}{cm^2}$.
On first sight, the resistivity decreases with increasing electron density. In fact, the resistivity measurement for the lowest density of $n_{2DEG} = 2.7 \cdot 10^{11} \frac{1}{cm^2}$ is beyond the

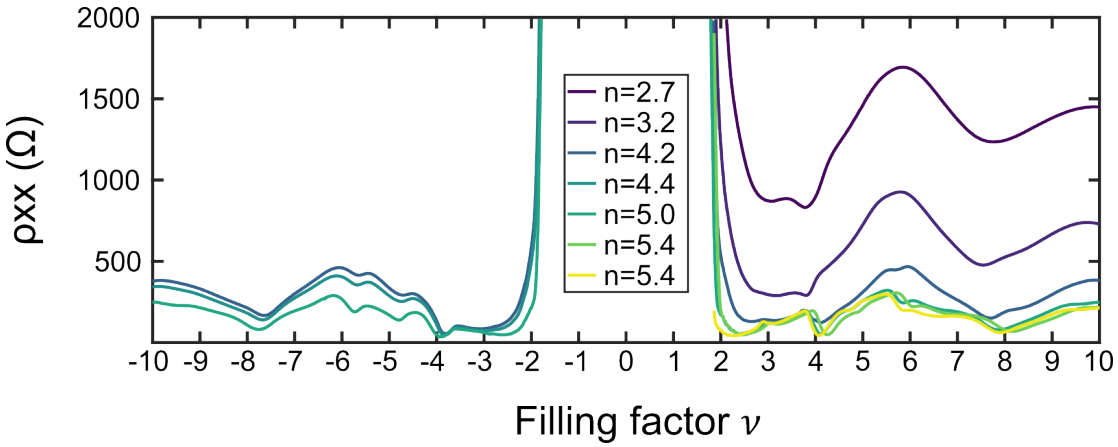


Figure A.1: Filling factor plot of the longitudinal resistivity. Lifting of the four-fold degeneracy.

scale of the figure.
We observe a lifting of the 4-fold degeneracy of the Landau levels due to spin and valley splitting at a filling factor of $\nu = 10$. The lifting becomes only visible for increasing electron density: While for $n_{2DEG} < 5.0 \cdot 10^{11} \frac{1}{cm^2}$ barley a modulation for $\nu = \pm 10$ is visible, starting with $n_{2DEG} = 5.0 \cdot 10^{11} \frac{1}{cm^2}$, a slight dip in the resistance can be observed. We attribute this indicated resistivity minimum to the lifting of the spin degeneracy, which we expect to occur for lower magnetic fields than the lifting of the valley degeneracy. However, we did not perform a verification of that assumption, for example by tilting the sample in the magnetic field [133, 134]. We do however perform an estimation of the electron g-factor $g^*(n_{2DEG} = 5.0 \cdot 10^{11} \frac{1}{cm^2})$ following [135]. The idea behind this estimation is to first estimate the Landau level broadening Γ and then to compare the Zeeman splitting at filling factor $\nu = 10$ to Γ.
For the estimation of the Landau level broadening we consider the onset of the SdH-oscillations at a magnetic field of B = 500 mT. Without valley splitting, the separation of two Landau levels is given by

$$\Gamma = \left(\frac{e\hbar}{m^*} - g^* \cdot \mu_B \right) \cdot 500 \text{ mT} .$$

The spin-splitting at $n_{2DEG} = 5.0 \cdot 10^{11} \frac{1}{cm^2}$ for a magnetic field of $B_{SS} = 2.1$ T now equals Γ so we conclude

$$\left(\frac{e\hbar}{m^*} - g^* \cdot \mu_B \right) \cdot 2.1 \text{ T} = g^* \cdot \mu_B \cdot 2.1 \text{ T}$$

and we calculate $g^* = 1.75$. This is a lower estimate, as the magnetic field required to resolve spin splitting B_{SS} may be lower than 2.1 T. Here we extracted the first magnetic field value in which the four-fold degeneracy was lifted clearly visible.
The valley splitting is observed starting at a filling factor of $\nu = 7$ for densities of $n_{2DEG} \geq 5.0 \cdot 10^{11} \frac{1}{cm^2}$ when a blip in the longitudinal resistance for an odd filling factor forms.
Moreover, for all measurements here we observe that no real zero-resistivity plateau forms which we would expect in the quantum Hall effect. We expect the Landau level broadening to be as large such that two neighboring levels overlap and no real zero-resistivity transport occurs. The thermal broadening is discussed later on in the Appendix in the section A.1.3 Furthermore, we want to point out that all longitudinal resistivity data diverge for large magnetic fields when the filling factor approaches or exceeds 2. The minimum at $\nu = 2$ is just visible, before the resistivity becomes arbitrarily large, easily exceeding tens of kΩ.

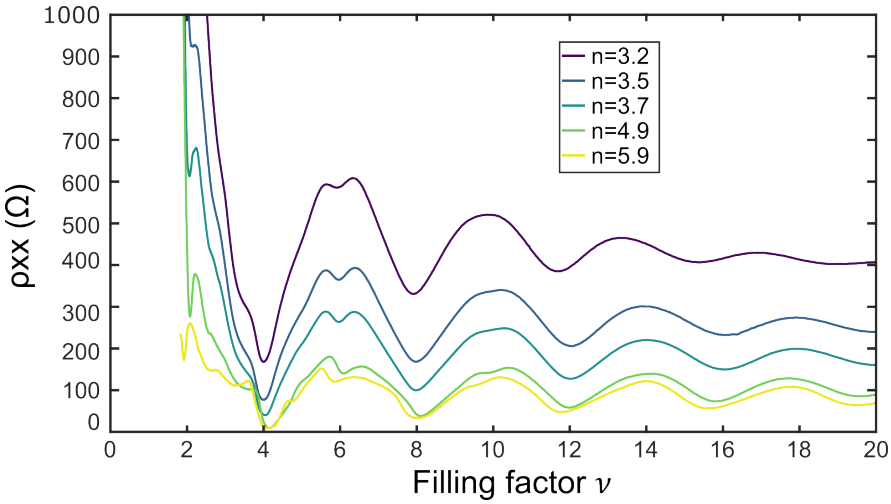


Figure A.2: Filling factor plot of the longitudinal resistivity. Observation of odd filing factors on a high-mobility sample at $\nu = 5$.

We repeated the measurement on a Hall bar device on a nominally identical heterostructure with significantly larger mobility, exceeding 180.000 cm^2/Vs, shown in Figure A.2. Interestingly, in this higher-mobility sample we do not see odd filling factors up to a value of $\nu = 5$, and even for this value, the dip in the longitudinal resistivity is very faded. Similar to the previous measurement, the resistivity starts to diverge just after the beginning of the $\nu = 2$ minimum formation.
To exclude just a large increase in the SdH oscillation amplitude, we performed a measurement on a third sample fabricated onto the same heterostructure which is shown in Figure A.3. Note that in this measurement, the scale bar for the resistivity is orders

of magnitude larger compared to the previous two measurements. We observe barely a kink in the graph at $\nu = 1$, marked by the arrow, ruling out an extreme increase of the oscillation amplitude to prohibit the formation of the $\nu = 1$ minimum.

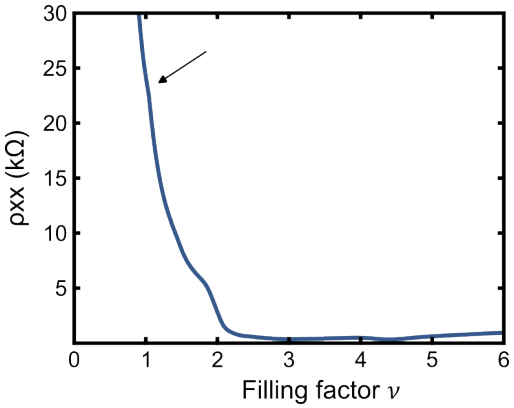


Figure A.3: Filling factor plot of the longitudinal resistivity. We barely observe a kink on the resistivity when the filling factor equals the integer value of 1.

In the next section we make a technical consideration of our measurement and if we accidentally influence the measurement results.

A.1.2 Measurements at low mobility and low filling factor: A technical consideration

We have clear indications that our currently used measurement setup affects the quantum Hall measurements when reaching low filling factors. Besides the divergence of the longitudinal resistivity, we also see a non-physical behavior of the transversal resistivity which is shown in Figure A.4a. The measurement shows the transverse resistivity as a function of the magnetic field for three segments of a Hall bar device. All segments were measured simultaneously. We observe the formation of plateaus of constant resistance for integer filling factors, in accordance with the quantum Hall theory. We also observe that starting from a filling factor of $\nu = 4$, the different segments show different resistivity values. Especially for $\nu > 2$, the courses of the graphs differ drastically. One segment ends up with a negative resistivity value for a magnetic field of 12 T.
We assume a technical error in the 4-point measurement so we quickly introduce here our standard measurement configuration.
Our measurement concept is based on an induced current along the Hall bar by a Lock-In amplifier. The voltage output of this Lock-In oscillates at ±5 V, at a frequency of about

17 Hz and has a pre-resistor of 100 MΩ connected to its output, that limits the maximal current through the Hall bar to 50 nA. When the 2DEG is well and fully accumulated it shows typically a two-point (contact) resistance of a few 10 kOhm, much lower than the value of the pre-resistor. So the current the Lock-In amplifier measures amounts typically close to the limit of 50 nA. We use at least two further Lock-In amplifiers in our setup, one to measure the transversal Hall voltage and a third one to measure the longitudinal voltage drop, respectively. This concept works well when the sample has a total resistance well below the pre-resistance of 100 MΩ as well as below the input resistance of the Lock-In amplifiers for the voltage measurements which is 10 MΩ.

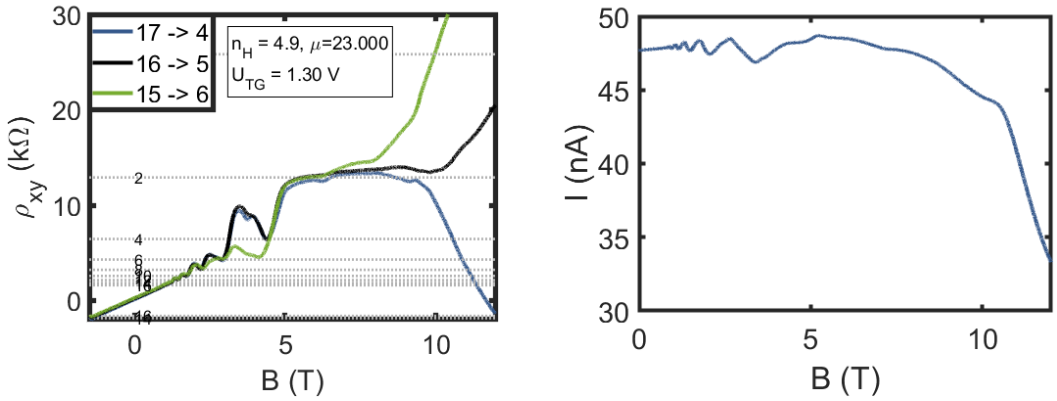


Figure A.4: Divergence of the transversal resistivity for magnetic fields larger than 10 T. (a) Measurement of the Hall resistance on three segments of a single Hall bar device at the same time. **(b)** A decline of the current indicates an increase of the serial resistance of the Hall bar device.

In our measurements, the current drops for a field strength larger than 10 T, shown in Figure A.4b, in sync with the deviation in the transversal resistivity. The figure shows the amplitude of the Lock-In current measurement. The y-component increases when the amplitude starts to decrease but remains below about 3.5 nA, so we expect the total resistance of the Hall bar to reach a value of $O(\text{M}\Omega)$.
As this is of the order of magnitude compared to the input of the Lock-In amplifier and the pre-resistor, we tried to correct the measurements and repeated them with a larger pre-resistor value and by subsequently including a voltage amplifier with nominally 1 TΩ input resistance connected between Hall bar and voltage-measurement Lock-Ins. We also tried to correct the measurement by using not multiple but only a single Lock-In to measure either the longitudinal or the transversal voltage on a single Hall bar segment at

the same time.
All three measures had a slight impact on the course of the transversal and longitudinal voltage measurement (the resistivity altered by up to about 5%), but neither measure solved either the longitudinal divergence nor the deviation in transversal resistivity for magnetic fields above 10 T here. We observed a similar behavior in samples with much larger mobility than shown here and are currently not able to correct the quantum Hall measurements for such low filling factors.

A second aspect that has to be considered when the resistance of a device increases is especially important for measurements inside the dilution cryostat. This setup is equipped with a RC-lowpass filter, as introduced in section 3.3.1. The cutoff frequency of the filter is mainly set by the capacity of 10 nF and the serial resistance $O(\mathrm{k}\Omega)$ and is set to about 8 kHz. If the serial resistance increases to $O(\mathrm{M}\Omega)$ also the cutoff frequency will affect quasi-DC measurements of our Lock-In frequency, which is typically set to 17 Hz. We do not have urgent indications, that filtering in the here presented measurements cause the non-physical effects, which were measured in the ^{3}He cryostat.

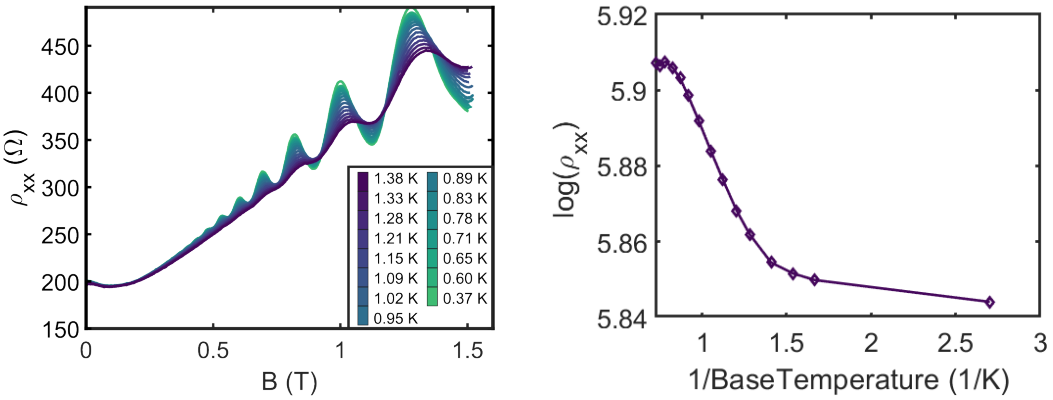
A.1.3 Base temperature ≠ electron temperature

The Hall bar measurements presented in the main text of this thesis were mainly performed within the ^{3}He cryostat with a base temperature of about 360 mK. Following the SdH theory [83], the longitudinal resistance is constant for low magnetic fields, as Landau levels are not well separated, because the Landau level separation $\hbar\omega < \mathrm{k_B} \cdot \mathrm{T}$. Increasing the magnetic field, the levels start to split, resulting in an oscillatory behavior of ρ_{xx}. The splitting and hence the transport now depends on the temperature. The textbook [83] distinguishes two different temperature regimes: For very low temperatures, there is no thermal activation of charge carriers. Transport in this regime is predicted by hopping between extended states. At elevated temperatures, thermal activation of charge carriers from one Landau level to the next higher one enables transport. This activation depends exponentially on the temperature. The SdH resistivity minimum is therefore proportional as follows [83]:

$$\Delta \mathrm{E} \sim \rho_{\mathrm{xx}}^{\mathrm{min}} \sim \exp(-\Delta \mathrm{E}/2\mathrm{k_B T}) \tag{A.1}$$

Δ E is the activation energy to the nearest extended unoccupied state, which is around the center of the next higher Landau level.
In our experiments we now distinguish between the crystal or base temperature and the electron temperature. The later is expected to be larger than the base temperature, as e.g. the measurement lines from room temperature may not be thermalized well. By

increasing the base temperature, at some value the base temperature eventually equals the electron temperature. Increasing the base temperature further, we expect the electron temperature to scale accordingly.
The dependence of the SdH oscillations on the base temperature is shown in the measurement in Figure A.5a. The graphs show the longitudinal resistance ρ_{xx} recorded as a function of the magnetic field B for different base temperatures of the cryostat. The



(a) **(b)**

Figure A.5: Estimation of the electron temperature. **(a)** Measurement of ρ_{xx} while varying the base temperature of the ^{3}He cryostat. **(b)** Arrhenius plot of the $\nu = 16$ minimum.

colder the base temperature, the more pronounced the SdH oscillations become. For the analysis we choose the minimum of the resistance close to 1.2 T, corresponding to a filling factor of $\nu = 16$. Figure A.5b shows the dependence of the minimal resistivity value in dependence of the inverse temperature on a logarithmic scale. Following the explanation from [83] there is a transition in the slope: Above about 700 mK base temperature, the resistance increases with temperature with a much steeper slope than for lower temperatures. This point marks the transition from hopping between extended states to thermally activated transport. For the high-temperature dependence we can perform a linear fit and the slope is proportional to the energy separation between neighboring states according to equation A.1.3. The slope is given by

$$\mathrm{m} = \frac{\delta \log(\rho_{xx})}{\delta \frac{1}{\mathrm{T}}} = -0.105\ \mathrm{K} = -\frac{\Delta\, \mathrm{E}}{2\mathrm{k_B}} \tag{A.2}$$

We expect the neighboring states to be separated by the Landau level splitting minus the Zeeman splitting, giving for a magnetic field of B = 1.125 T:

$$\begin{aligned} \Delta E^* &= \hbar\omega_c - g\mu_B B = (\hbar\tfrac{e}{m^*} - 2\mu_B)\cdot Bs = (\hbar\tfrac{e}{m^*} - 2\tfrac{e\hbar}{2m_e})\cdot B \\ &= 2(\tfrac{m_e}{m^*} - 1)\mu_B \cdot B = 8.52 \cdot 5.79 \cdot 10^{-5}\ \text{eV/T} \cdot 1.125\ \text{T} = 555\ \mu\text{eV} \end{aligned} \tag{A.3}$$

From the linear fit however we extract a much smaller energy separation of $\Delta E = 18.1\ \mu$eV. Such a large discrepancy has already been observed in different experiments. A possible explanation [136] is that the levels are not only temperature broadened, but that there is also impurity broadening, which reduces the Energy separation $\Delta E^* = \Delta E - \Gamma$. Note that the energy difference here is a few hundreds of µeV. A second explanation ansatz in [83] is that the electron g-factor differs from the vacuum one for large magnetic fields where spins tend to align parallel due to exchange interaction. This effect however becomes only relevant for magnetic fields larger than 1 T used here. Next, we perform a second study,

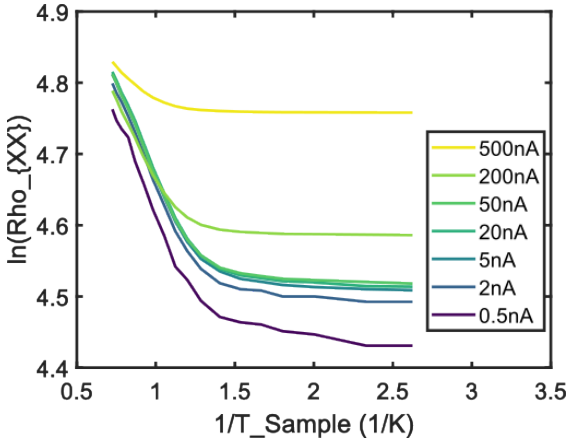


Figure A.6: Arrhenius plot for different current amplitudes.

for testing how the current amplitude affects the electron temperature. The Arrhenius plot evaluated at the $\nu = 12$ minimum is shown in Figure A.6. The figure shows a clear increase in the resistivity for larger currents. For an upper bound estimation of the electron temperature, we evaluate the intersection of the linear slope for high base temperatures and an extension of the approximately constant ρ_{xx} value for low base temperatures.
We extract by this method an estimation of 740-780 mK for currents up to 50 nA. For higher currents the electron temperature estimate here increases strongly to 900 mK for 200 nA or 1200 mK for 500 nA.
As results from this electron temperature analysis, we recommend to not use currents larger than 50 nA. The 0.5 nA data were very noise here, albeit the data showed an even

lower electron temperature. There have been studies like this for Zeeman split Landau levels at low magnetic fields (B < 0.35 T) for example on a GaAs heterostructure in [137]. The analysis using the Zeeman splitting only is possible for very low electron temperatures (T < 50 mK). For our Si samples in combination with the ^{3}He setup the spin-splitting is not resolvable for such low magnetic fields, as discussed in section A.1.1. There is a second study regarding this topic in [138] in which the effects of the current amplitude on resistivity overshoots of quantized plateaus is discussed.
We also performed the analysis of the energy separation of the neighboring states for the measurement series in Figure A.6. For the slope we extract m = 0.54 K and the corresponding activation energy to the next unoccupied extended states is $\Delta E^* = 93$ µeV. Again this value is significantly smaller than the value of 809 µeV, calculated analogously to A.1.3 and with the applied magnetic field 1.64 T here.

A.2 Appendix - ASD

A.2.1 Reverse bias application

In all Coulomb diamond measurement presented in the main text of this thesis the bias voltage was applied asymmetrically: The source reservoir was held at ground potential and the drain reservoir potential was controlled by the bias voltage of up to ±15 mV. To exclude that this measurement asymmetry leads to the tilting of the Coulomb diamonds, we present in Figure A.7 a study on one of the 2nd generation type of ASD devices and applied the voltage bias in the opposite configuration, by keeping the drain reservoir at ground potential and tuning the source potential. The figure shows a measurement series featuring three Coulomb diamond measurements for different sliding gate voltages ranging between 215 mV and 340 mV. The measurements show that when biasing the source reservoir, the steepness of the diamond edges barely changes. Also we observe that the diamonds appear very symmetric. This is a confirmation that the tilting of the diamonds in normal voltage biasing operation indeed is a consequence of the potential slide formation in combination with the spatial separation of sensor dot and drain reservoir. The sliding gate voltages were chosen such that for the normal voltage bias operation the

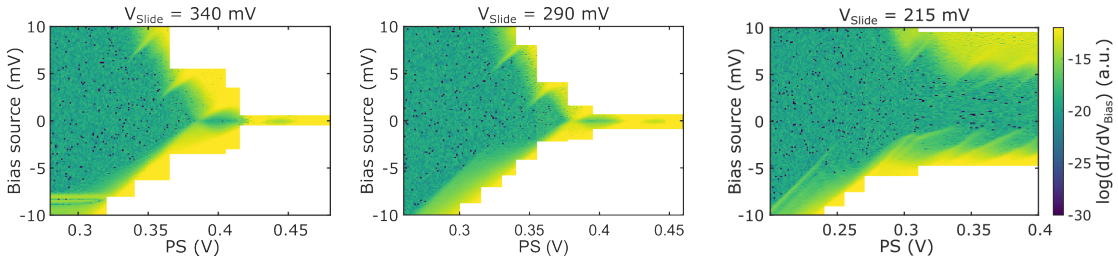


Figure A.7: Reverse bias application. Three Coulomb diamond measurements recorded by fixing the drain reservoir behind the sliding gates at ground potential and biasing the source reservoir. We barely observe a change in the slope of the Coulomb diamond edges which remain very symmetric throughout the sliding gate variation.

potential slide would be deactivated for V_{Slide} = 340 mV, and the spatial separation in turn would be activated for V_{Slide} = 215 mV. For the normal bias application we observed a strong tilting of the diamonds in the main text in Figure 5.12d.

A.2.2 Back-action

In the introduction of the charge state readout concept by an asymmetric sensor dot we already noted that in general a larger bias voltage will be required for the operation of the ASD compared to the commonly used symmetric sensor dot. The increased bias voltage

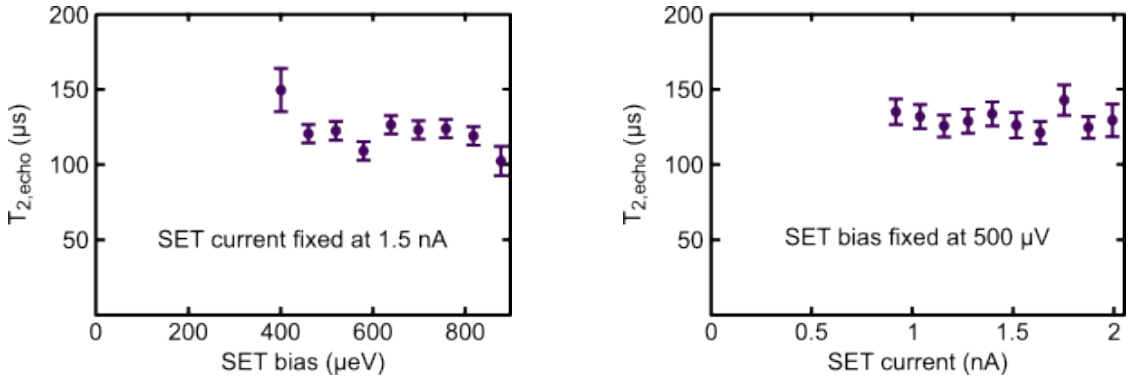


Figure A.8: Back-action effect on the spin-qubit coherence time. **(a)** Measurement of the $T_{2,echo}$ dephasing time of a spin qubit using a symmetric SET sensor for the readout and varying the SET bias voltage. **(b)** Measurement of the $T_{2,echo}$ time for a variation of the SET current. Both measurements were performed by T.Struck and Dr. A. Hollmann at the RWTH Aachen University.

may now increase the risk of a back-action effect on the qubit, as the energy dissipated via phonons or photons by transport across the SET exceeds the typical Zeeman splitting of the spin qubit which amounts to about 100 µeV and may interact with the spin qubit. In Figure A.8 we show measurements of the spin decoherence time $T_{2,echo}$, recorded on a Si-based qubit device featuring a symmetric sensor dot for the readout. Measurements on that device are published in [58, 119] and were performed by T. Struck and Dr. A. Hollmann at the RWTH Aachen University.
Figure A.8a shows the $T_{2,echo}$ time as a function of the SET bias, varying the bias voltage from 400 µV for normal operation up to close to 1 mV. Figure A.8b shows the $T_{2,echo}$ in dependence of the SET bias for currents up to 2 nA. In both measurements we do not observe a variation of the dephasing time. This is a promising first result considering a possible back-action effect, but a final exclusion of potential drawbacks by a working ASD device is currently pending.

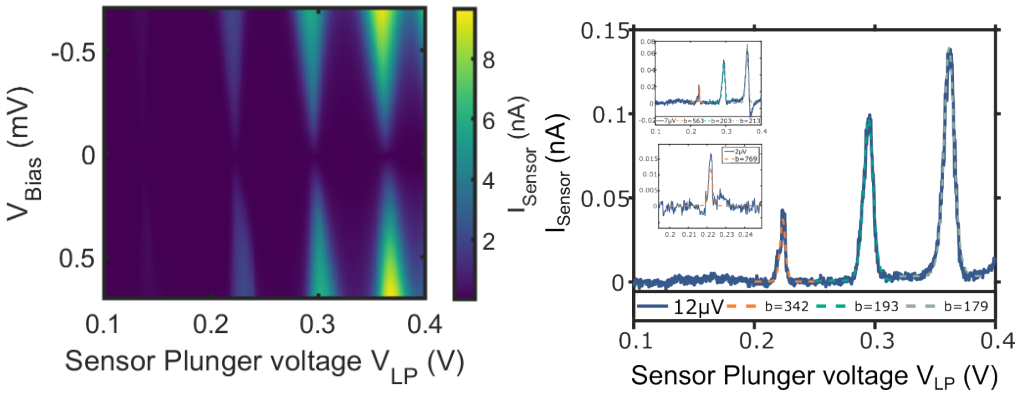
A.3 Appendix - Spin qubit device (Qubus)

A.3.1 Electron temperature

In the main text, the electron temperature of the Qubus device received a major role during the discussion of the additional tunnel events that appeared when the qubit dot was loaded from the SET.
Moreover, the electron temperature was also significant during the discussion of the visibility of single-shot spin readout measurements for low magnetic fields, when the Zeeman splitting did no longer exceed the thermal broadening of reservoir and qubit dot level energy.
As we avoided using the SET as electron reservoir for the qubit dot, the critical measure which we do not want to cross with the thermal energy broadening will be set by the Zeeman energy of the spin-splitting which we eventually want to exploit as our qubit two-level system. The spin splitting for reasonable magnetic fields not exceeding 1 T is typically around a hundred micro electron volt. A larger magnetic field in principle is possible, but soon we will be technically limited by the required RF-frequency needed for the qubit manipulation and eventually exceeds the intrinsic valley splitting hotspot.
Here, we present two measurements of the electron temperature. One measurement uses the Coulomb oscillations in the sensor dot to give a first estimation of the electron temperature, but is prone to a large error bar. In a second measurement we fit the charge-sensing signal of the loading of the N=1 electron into the qubit dot, which gives us a second estimation of the electron temperature.
We already assume that the electron temperature exceeds the base temperature of the cryostat due to heat input via the electrical connections of the device to measurement equipment at room temperature. Therefore, in the following section we also emphasize the impact of the installation of a low-pass filter at cryogenic temperatures halfway through the Qubus measurement series.

Coulomb diamonds

For a first estimation of the electron temperature, we record a Coulomb diamond measurement of the SET, shown in Figure A.9a. It is important to note, that this measurement was recorded ahead of the installation of a DC-cryostat filter mounted at the mixing plate of the mixing cryostat. Three transport peaks along which current is conducted through the SET are visible in the measurement. A fourth peak around 130 mV gate voltage on plunger LP on the very left of the measurement is barely visible. The Coulomb blockade theory was introduced in chapter 2.3.1.
The width of the transport peaks in this measurement critically depends on the electron



(a) **(b)**

Figure A.9: Coulomb diamond measurement for an evaluation of the electron temperature without installed cryogenic filter. **(a)** Coulomb diamond measurement. **(b)** Line-cut for a bias voltage of 12 µV. In the two insets, line-cuts at bias voltages of 7 µV and 2 µV are shown.

temperature of the system. For the lowest bias voltage applied to the SET in the measurement, the peak width is only set by the thermal broadening of the SET level and the source and drain Ohmic contacts. Here, the current peaks can be fitted by the formula [139, 140][83, 18.57 p. 396].

$$I(V_{LP}) = \frac{I_0}{\cosh^2(b \cdot (V_{LP} - V_0))} \tag{A.4}$$

In this equation the width b of the peaks is described by

$$b = \frac{\alpha_{LP}}{2 \cdot k_B \cdot T} \tag{A.5}$$

α_{LP} is the lever arm of gate LP on the sensor quantum dot and can directly be determined from the Coulomb diamond edges in Fig A.9a. Here we extract the lever arm at a current of I_{SET} = 500 pA and calculate [83, 122, 123]:

$$\alpha_{LP} = \left| \frac{m_S \cdot m_D}{m_S - m_D} \right| = 0.058 \, \frac{eV}{V}.$$

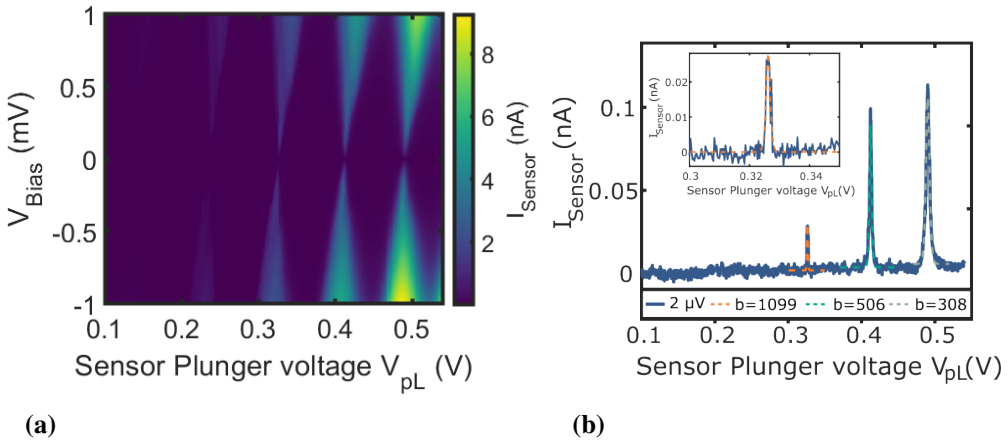
Figure A.9b shows three line-cuts of the diamond measurement for 12, 7 and 2 µV bias.

We fit the data for the 12 µV bias line-cut and extract electron temperatures of

$$T_1 = 884\,\text{mK} \pm 40\%, \quad T_2 = 1567\,\text{mK} \pm 40\%, \quad T_3 = 1689\,\text{mK} \pm 40\%$$

for the peaks from left to right. We attribute the large error bar due to the evaluation of the lever arm, which we already identified as challenging in the ASD chapter.
Note, for the two lower bias voltages of 7 µV and 2 µV the peaks are not clearly resolved any longer. Although we cannot precisely estimate the error bar for the temperature evaluation for these two low-bias line-cuts, we estimate an increase to the already large error bar of 40 %.
If we calculated the temperature for the only resolvable peak in the 2 µV line-cut, we extract a temperature of about 393 mK plus the large error bar.

All these extracted electron temperatures seem very high. Also, we observed during the analysis, that the method of calculating the electron temperature from Coulomb diamond broadening is a rather imprecise method that comes with a large error bar. We will use these measurements nevertheless and compare them to Coulomb diamond measurements recorded after the installation of a DC cryostat filter mounted to the mixing plate which will be presented in the following.



(a) **(b)**

Figure A.10: Coulomb diamond measurement for evaluation of the electron temperature after installation of the cryogenic filter. **(a)** Coulomb diamond measurement. **(b)** Line-cut for a bias voltage of 2 µV and a zoom in of the last transport peak around 320 mV in the insert.

We record a second Coulomb diamond measurement, presented in Figure A.10a af-

ter the installation of a DC filter as introduced in the setup section in 3.3.1. Note, the sample could be thermally cycled many times and always returned to the exact same tuning configuration upon an anew cool down cycle. For the measurement presented here, we tuned to a similar configuration compared to the previously presented Coulomb diamond measurement.
In this measurement of the Coulomb diamonds with installed cryogenic DC filter we again observe 4 Coulomb blockade transport peaks of the SET sensor, of which the peak for the lowest sensor plunger gate voltage is barely visible. In this measurement, we were no longer limited by the used bias voltage for taking a line-cut across the Coulomb diamond measurement. Figure A.10b shows a line-cut of the measurement taken at at bias voltage of 2 µV. The figure also shows a zoom-in of the smallest Coulomb peak around a plunger gate voltage of about 320 mV.
We determine a lever arm of the LP gate from the Coulomb diamond measurement of $\alpha_{\mathrm{LP}} = 0.072\ \frac{\mathrm{eV}}{\mathrm{V}}$, extracted at a current of 500 pA.
Using this lever arm, we fit the three peaks in Figure A.10b and extract electron temperatures of the device with installed cryogenic filter of

$$\mathrm{T}_1 = 380\ \mathrm{mK} \pm 40\% \quad \mathrm{T}_2 = 826\ \mathrm{mK} \pm 40\% \quad \mathrm{T}_3 = 1.36\ \mathrm{K} \pm 40\%.$$

At first glance these extracted temperatures seem lower compared to the electron temperature evaluation of from the Coulomb diamond measurements recorded before the filter installation. However, comparing the two lowest extracted temperatures of $\mathrm{T}^{\mathrm{low}}_{\mathrm{NoFilter}} = 393$ mK and $\mathrm{T}^{\mathrm{low}}_{\mathrm{Filter}} = 380$ mK we do not observe a large quantitative difference.

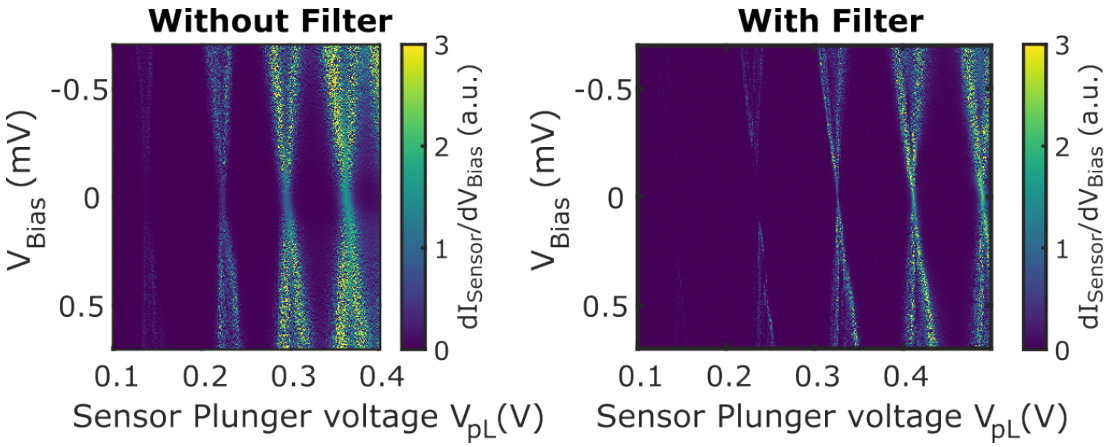
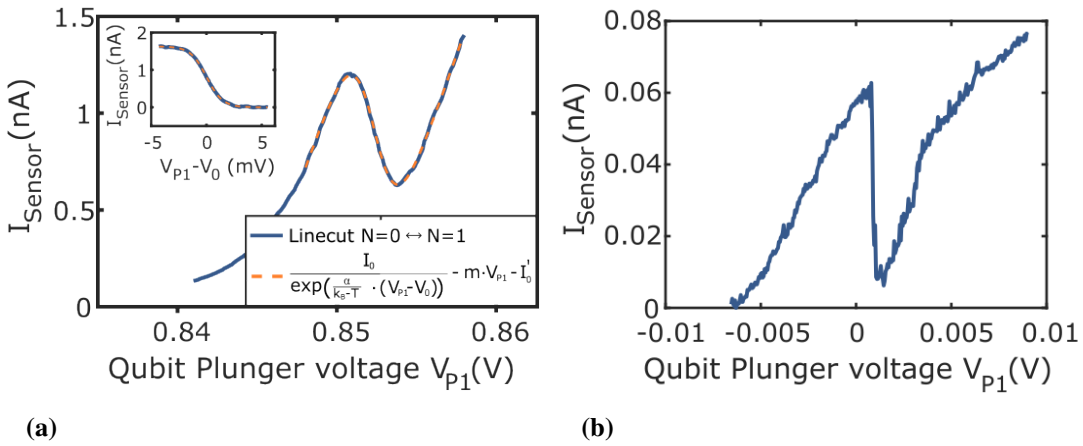


Figure A.11: Comparison of the Coulomb diamond measurements before and after the installation of a DC filter mounted to the mixing plate of the cryostat.

We found the largest qualitative difference between both measurements before and after the filter installation by comparing the two measurements next to each other, as shown in Figure A.11. Note, for both measurements, the x-axis as well as the color bar match.
We observe that for the lowest bias, so when the Coulomb blockade peak is dominated by the electron temperature, the transport peaks after the filter installation appear significantly smaller compared to the measurement before the filter installation.

Transition width fit

For the electron temperature analysis by fitting of a low-bias line-cut across a Coulomb diamond measurement we observed a very large error bar in the temperature evaluation. Hence, in the following we introduce a second and potentially more precise measurement which allows to directly measure the thermal broadening of the SET and the qubit dot level. The technique is adapted from [94].



(a) **(b)**

Figure A.12: Broadening of the charging transition width. **(a)** Measurement of the sensor current for charging of the qubit dot by one electron before the installation of the cryostat DC filter. **(b)** Measurement of the transition width after a DC filter was installed.

Here, we use a charge sensing transition, as shown in both graphs of Figure A.12 for the determination of the electron temperature. The kink in the sensor Coulomb peak arises when the qubit dot level is aligned with the reservoir energy. Hence, we expect the kink to be broadened the same way as the involved energy states: The higher the electron temperature, the broader the transition appears in the measurement, following a Fermi-broadening function.
For the measurement of the charging kink it is important that we cannot use a single-shot

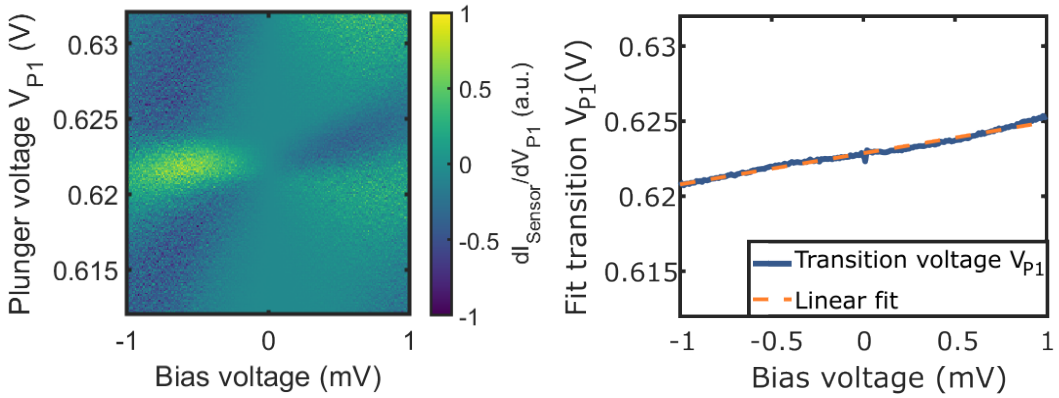
measurement but we have to average multiple scans across the transition to measure the temperature-broadened kink. For the measurement it is important to adjust the tunnel rate faster than the measurement speed but not too fast to not allow additional transition broadening which may be caused by an enhanced interaction with the reservoir [94]. Here we set a tunneling rate of about 100 µs. Also for the averaging of multiple line-scans we must avoid to pick up artificial broadening of the transition that is caused by a slow drift on the timescale of minutes. Therefore we only average measurements of the linescan for a duration of less than one minute at once and rather average electron temperature estimations of subsequent linescan packages afterwards. Also for the bias we prefer a low bias to not induce heating from the reservoir.
Figure A.12 shows two measurements of the charging of the first electron onto the qubit dot. Figure A.12a was recorded before the installation of the DC cryostat filter while Figure A.12b presents a measurement with installed DC filter. Already at first sight we observe that the transition with installed filter appears much sharper compared to the measurement without filtering.
We can fit this current signal of the charging kink, assuming that the sensor peak slope is locally linear in first estimation. The kink is broadened by a Fermi distribution. Hence, a fit formula is given by

$$I(V_{P1}) = \frac{I_0}{\exp\left(\frac{\alpha_{P1}\cdot(V_{P1}-V_0)}{k_B\cdot T}\right)+1} - m\cdot V_{P1} - I_0' \tag{A.6}$$

Here, m is the first order linear approximation of the sensor peak and α_{P1} is the lever arm of the plunger gate P1. The formula accounts for the thermal broadening as for increasing temperature the transition step will be broader (= longer voltage span). Using a lever arm of $\alpha_{P1} = 0.48$, which will be estimated in the ensuing section A.3.2, we calculate an electron temperature of $T_{el} = 1.8$ K ± 7% for the linescan before the filter installation. We apply the same formula and the same lever arm also to the measurement recorded with DC filtering and here the temperature fit average results in $T_{el} = 475$ mK ± 7%. Both values appear rather high, especially compared to the temperature estimation performed in [94], which resulted in an electron temperature of just above 100 mK.
We recommend at this point to repeat the transition width analysis while also varying the base temperature of the cryostat. We could not perform this measurement here due to time constraints. We expect no difference in the evaluation as long as the cryostat base temperature remains below the electron temperature. Once the base temperature exceeds the electron temperature, the electron temperature follows the set cryostat base temperature. A variation of the base temperature also provides a good estimation of α_{P1}. Here, we used a different estimation of the lever arm presented in the following.

A.3.2 Lever arm α_{P1} determination

A requirement for determining the electron temperature is knowledge of the lever arm α_{P1}. A simple estimation of the gate lever arm can be given when we align a qubit dot transition with the reservoir Fermi energy. If we now decreased the Fermi energy by 1 meV, for example if we applied a bias voltage of +1 mV to the Ohmic contact, we have to apply the voltage ΔV_{LP} to gate LP to reduce the potential of the qubit state by $\alpha_{P1} \cdot \Delta V_{LP} = 1$ meV.



(a) **(b)**

Figure A.13: Determination of the lever arm α_{P1}. **(a)** Measurement of the N=1 qubit charging transition as a function of the reservoir bias and the qubit plunger gate. **(b)** Transition voltage from a fit of **(a)** for every bias voltage value. A linear fit to the data provides the lever arm of the P1 plunger gate.

Figure A.13a shows a measurement of the current derivative through sensor as function of both the qubit plunger voltage V_{P1} and the sensor bias. For every bias voltage we fit the corresponding linescan measurement with equation A.6. Figure A.13b shows the extracted transition voltage V_{P1}. A linear fit to the data now provides $\alpha_{P1} = 0.48$ eV/V.

A.3.3 Sweep direction

A prominent measurement artifact becomes visible when the tunnel barrier separating qubit quantum dot and reservoir becomes opaque, or more precise when the tunnel rate is on the order of magnitude of the measurement speed.
Figure A.14a and Figure A.14b show the same measurement of the charge stability of the qubit quantum dot via charge sensing. The notable difference is that for one measurement the voltage at plunger P1 is ramped from 850 mV to 750 mV in Figure A.14a and in the other direction from 750 mV to 850 mV in A.14b. The figures now differ for B1 voltages

below 450 mV, as here the tunnel barrier becomes increasingly opaque the lower the barrier voltage is set. Accordingly, the tunnel rate for the electron decreases and tunneling events occur on a longer time scale compared to the measurement speed, which is was set to 10 mV/s for both measurements. As a result, the transition lines of the qubit quantum dot are bent towards one direction.

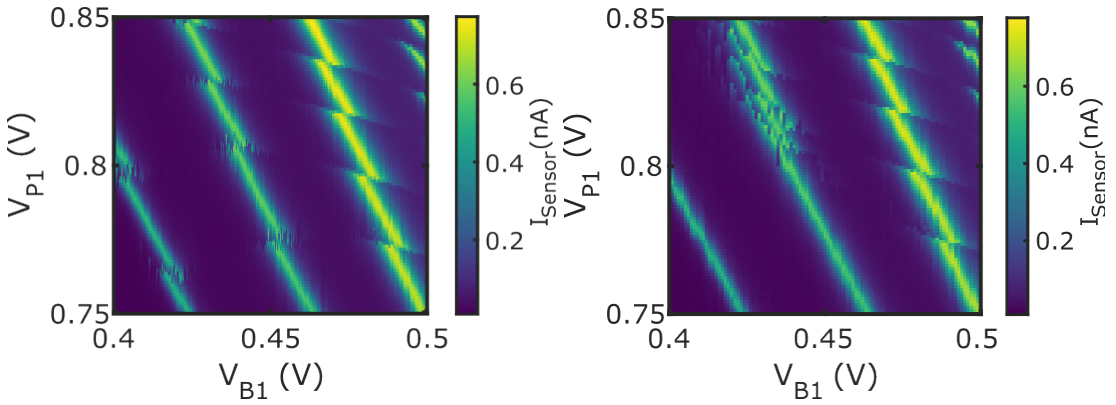


Figure A.14: Measurement artifact when the tunnel rate becomes lower than the measurement speed. (a),(b) Same charge stability measurement of the qubit dot. For **(a)** the gate sweep direction was from larger P1 voltages to lower P1 gate voltages, while for **(b)** the sweep direction was reversed.

The difference in voltages for the transition lines for both measurements amounts to multiples of 10 mV. Hence, the tunnel rate can also be estimated to multiple seconds in accordance with the measurement speed of 10 mV/s. Note, that this low tunnel coupling regime is not suited for single-shot spin or electron charge readout measurements.
In contrast, for higher tunnel rates (B1>450 mV) both graphs resemble as the tunneling of the qubit electron occurs on a much faster timescale compared to the measurement speed.

A.3.4 Spikes

A second measurement artifact can be observed in pulsed measurements. To demonstrate this artifact, Figure A.15a shows again the measurement series to record the T1 relaxation constant. The figure shows the tenfold repetition of the three level pulse sequence of unloading, loading and reading out of the qubit as introduced in the main text of this thesis.
Figure A.15a highlights spikes in three of the 10 measurement cycles at the transition

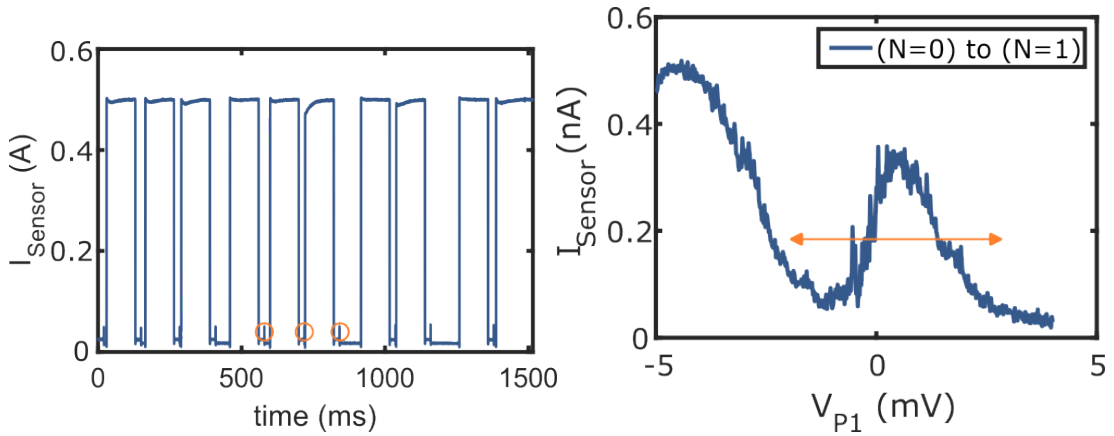


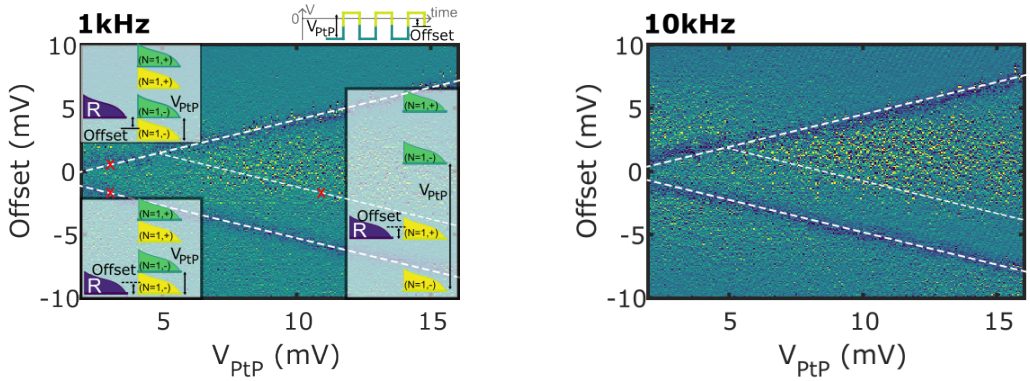
Figure A.15: Spikes as measurement artifacts for pulsed measurements. (a) T1-measurement sequence consisting of 10 three-phase pulse sequences. **(b)** Scan of the sensor Coulomb blockade. The arrow indicates the pulsing between unloading and loading stage of the pulse sequence.

from the unloading to the loading phase, but spikes can be observed in all 10 cycles. We interpret these spikes as measurement artifacts and attribute their origin to the finite pulse ramp provided by our AWG and the bandwidth of our setup. Note, we pass the AWG along the DC lines to the sample. Figure A.15b explains the origin of such spikes. While the unloading of the qubit occurs at a negative P1 gate voltage offset, loading of the qubit appears for a positive gate voltage offset. The pulse between both stages is indicated by the orange arrow. When pulsing now from the unloading to the loading stage, the Coulomb oscillation in between has to be traversed. If the pulsing ramp is slower than the measurement speed, we detect some portion of the larger current on top of the Coulomb oscillation in our averaged current measurement, which causes the spikes observed in Figure A.15a.

This observation is not just an artifact in the measured data. This finite and potentially too long pulse ramp may cause a severe problem especially for the initialization of the qubit in our measurements: When pulsing into the loading stage, both spin-split qubit states are tuned below the Fermi energy of the reservoir. If the pulse ramp is now relatively long (compared to the tunneling rate), the spin down state is pulled below the reservoir energy earlier than the spin up state. This discrepancy may lead to an initialization of spin down electrons with much larger rate than spin up electrons.

A.3.5 Pulsed gate spectroscopy

We can use the sensitive dependence of tunnel rate on alignment to the reservoir Fermi energy to resolve the quantum dot excited valley, Zeeman and orbital states. The technique in the following is inspired by [117].
We apply a 50% duty cycle rectangular pulse and alter both, the amplitude of the rectangular pulse as well as the gate voltage offset. Two graphs of such measurement, recorded for frequencies of 1 kHz and 10 kHz, are shown in Figures A.16a and A.16b. In both measurements, we observe a V-shape in the derivative of the sensor current. On the upper branch the N=1 ground state transition is aligned with the reservoir during the positive amplitude phase of the pulse, on the lower branch it is just vice versa. These two transition lines are clearly visible in both figures due to the tunneling enhancement when the qubit level is exactly aligned with the reservoir.



(a) **(b)**

Figure A.16: Pulsed gate spectroscopy. **(a)** Measurement at a frequency of 1 kHz. **(b)** Same measurement as in **(a)** but recorded at a frequency of 10 kHz.

The idea of this pulsed spectroscopy is that when an excited qubit level is aligned with the reservoir, we aim to see additional parallel lines to the ground state line due to the enhancement of the tunneling. In both measurements, we observe one additional line, separated by about 2 meV from the ground state. We attribute this line to an excited state and due to the energy difference we can exclude Zeeman or valley excited states, which are few hundreds of µeV or less at the applied magnetic field of 1.5 T. We can also exclude the (N=2) electron state, which is much larger in energy. We attribute this line to an orbital excited state.
Note, that we only measure one line of the excited state parallel to the lower ground state line, and not the upper one: We only see loading through an excited state but not unloading as typically the relaxation from excited states to the ground state is very fast.

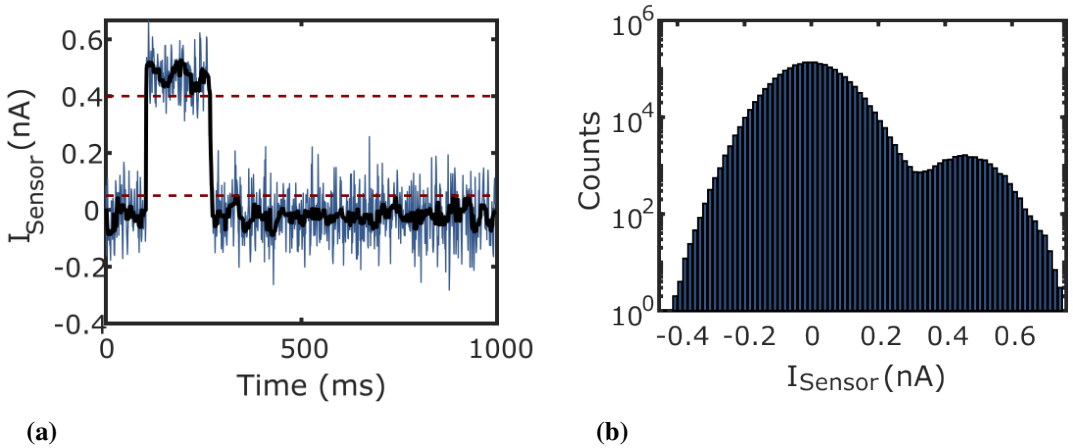
We need very sensitive tuning to resolve valley and Zeeman split states. Best for this experiment would be to compensate the sensor also during the pulse applications which we could not do for the presented measurements here. Also the measurements presented here were recorded before the installation of the cryostat filter. Besides the sensitivity of the sensor, also the pulse duration has to match the expected tunnel rate to the excited states. This is crucial, but hard to implement. So for an upcoming experiment, we recommend to not record a measurement varying offset voltage and pulse amplitude V_{PtP} but to fix the pulse amplitude and vary the gate voltage offset and the pulsing frequency. Also an averaging scheme like introduced in [117] may improve the data quality.

A.3.6 Digitizing

The concepts of digitizing single-shot measurement traces follows the ansatz presented in my Master's thesis [75]. The basic procedure for any single-shot trace is as follows:

- Apply a median filter with a kernel of about 1% of the readout length
- Subtract the median from the measurement data. Normally, for most of the readout phase, the qubit dot is loaded and the median value corresponds to the sensor current for the N=1 configuration. The subtraction of the median for each single-shot trace accounts for slow drifts of the sensor configuration. Typically we also apply a sign flip if necessary, such that a current of 0 nA current always corresponds to a loaded dot and that tunneling results in positive current blip.
- Apply a Schmidt trigger instead of a single threshold value to determine whether a trace features a tunneling blip or not. Here, we define two values for the upper and lower level of the Schmidt trigger. The two trigger thresholds together with a median filtered example trace is shown in Figure A.17a. The two trigger levels can either be chosen by eye or by plotting a histogram of all readout data (A.17b).

To check if the qubit initialization is successful, we typically control if during the first 0.5% of the single-shot readout data the current exceeds the upper limit. If it does we term the trace as badly initialized. Otherwise we consider the qubit as loaded. For identifying a spin up trace, we wait until the current surpasses the upper limit. At this point we consider the qubit as unloaded. Afterwards we wait until the current drops below the lower limit and then the qubit is considered loaded again. We then define a minimal length of typically 1.5% of the whole readout length. Only when the measurement signal after surpassing the upper limit did not drop below the lower threshold during that length, we consider the signal as valid. Otherwise we term it a spike and do not use it for our spin up rate analysis. All traces that have at least one valid blip and are not defined badly



(a) **(b)**

Figure A.17: Post processing of the single-shot readout data. **(a)** Two Schmidt trigger levels applied to an exemplary spin-up readout trace. **(b)** Histogram of all readout data to determine the two levels of the Schmidt trigger.

initialized are considered spin up. Note, multiple-blip traces have not been excluded: Simply eliminating them would lead to evaluation errors [75].
We also published an evaluation scheme to detect single electron tunneling events using a neural network in [119].

A.4 Appendix - Charge noise power spectral density

A.4.1 PSD measurements before installation of a DC cryostat filter

In this supplementary section we want to show the comparison of noise spectra that were recorded by direct transport measurements through the SET sensor of the Qubus device. The spectra shown in Figure A.18a were recorded in the dilution cryostat system after the installation of the DC cryostat filter, introduced in section 3.3.1, while the spectra in Figure A.18b were recorded before its installation. Both figures show an insensitive measurement as well as a sensitive measurement. The corresponding tuning of the SET is indicated by colored dots in the insets.

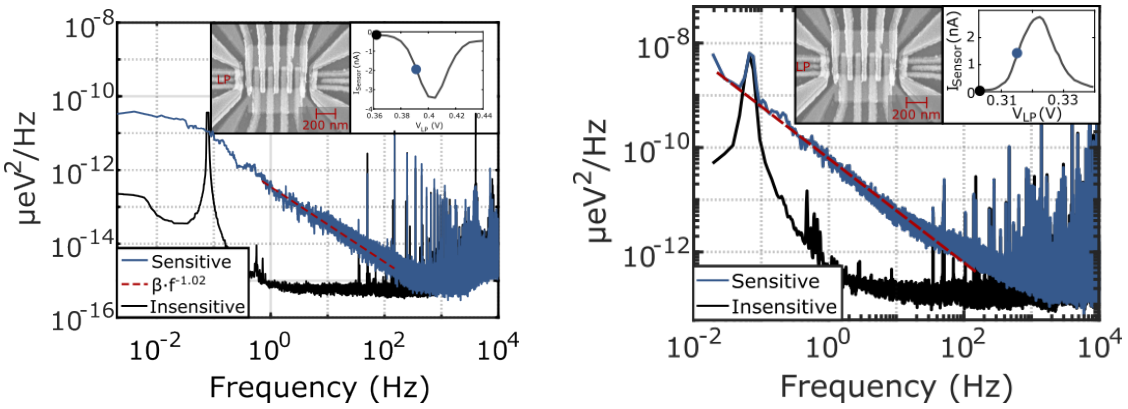


Figure A.18: Impact of the cryostat DC filter on the measured noise amplitude. **(a)** PSD measurements after the filter installation using the optimized amplification of $10^8 \cdot 10$. **(b)** Measurements before the filter installation, using the slightly worse amplification of $10^7 \cdot 10$. The red dashed line is a guide to the eye following a $f^{-1.0}$ power law.

Both sensitive measurements show a f^{-1} power law dependence for the frequency interval of [10 mHz - 1 kHz], indicated by the red dashed lines. Comparing the S_0(1 Hz) values of the noise amplitude exacted at 1 Hz we find that the value of about 9 $\mu eV/\sqrt{Hz}$ measured before the filter installation significantly exceeds the value of 0.64 $\mu eV/\sqrt{Hz}$ before installation of the filter. This deviation also exceeds the difference expected for the different settings of the amplification factor of the pre-amplifiers, which was set to $10^8 \cdot 10$

in the measurement here after filter installation in comparison to the value of $10^7 \cdot 10$ before.

A.4.2 Complementary accumulation-mode device PSD measurement

In the main text, we observed a f^{-1} power law dependence of the charge noise amplitude by direct transport through the SET of an accumulation-type qubit device, fabricated on a custom tailored heterostructure by Lawrence semiconductors (S4840R/S39) at the RWTH Aachen University by Ran Xue (Qubus device). This PSD is shown in Figure A.19a.

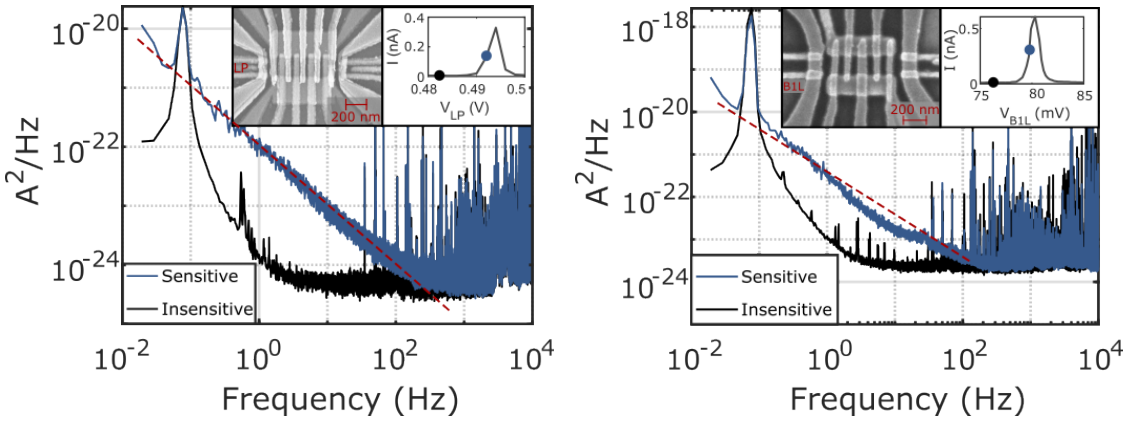


Figure A.19: PSD of two accumulation-mode devices. **(a)** Qubus device fabricated at the RWTH Aachen University on a Lawrence Semiconductor heterostructure. **(b)** Device with comparable gate design, fabricated at the University of Regensburg on a MBE-grown heterostructure.

We measured a comparable spectral dependence in a second accumulation-type qubit device, shown in Figure A.19b. The gate design, that was fabricated by Michaela Zoth [129], is shown in the inset of the figure. The sample was fabricated on a MBE grown Si/SiGe heterostructure and processed at the University of Regensburg. The sensitive spectrum in Figure A.19b slightly deviates from the f^{-1} power law dependence around 10 Hz, comparable to the observation made in [122].

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