Design and Performance of a sub-5 ps jitter Time-to-Digital Converter ASIC in 22 nm CMOS

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Abstract

We present the design of a Time-to-Digital Converter (TDC) ASIC together with performance characterization results at cryogenic temperature (6-8 K), and at room temperature using Low-Gain Avalanche Detector (LGAD) signals. The TDC design uses a two-step architecture with a ring-oscillator based counter and a Vernier delay line "fine TDC," combining low power (0.5 mW) and area (0.003 mm^2). The TDC is implemented in an FD-SOI process, and back-gate tuning is used both to correct threshold variation due to cryogenic operation and to enable tuning of the fine TDC delay elements with very little overhead. We present test results using the Fermilab Constant Fraction Discriminator (FCFD) ASIC to produce discriminated signals from an internal charge injection mechanism that mimics the waveform and signal amplitude of minimum ionizing particles impinging on LGAD sensors. The TDC ASIC and its associated readout system is used to measure the time-of-arrival of the injected signal relative to an external clock trigger. We characterize the time resolution performance of the full system and verify that the TDC ASIC contributes a negligible amount to the total system time resolution, fully consistent with the expected time resolution contribution of less than 4 ps. The results presented here demonstrate the utility of our TDC for applications in physics and quantum communications.

Keywords: Solid state detectors, Timing detectors, Particle tracking detectors (Solid-state detectors), Time-to-digital Converter, TDC, cryo-CMOS, SNSPD, LGAD

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Contents

1. Introduction

Precise timing information plays a critical role in many detector systems used for fundamental science ranging from applications as diverse as single photon detectors for quantum communications [1] to tracking detectors for future particle colliders [2]. For the former, exploiting and preserving the exquisite temporal resolution of fast timing detectors such as superconducting nanowire single photon detectors (SNSPDs), which have demonstrated sub-3 ps resolution [3], requires close integration with high-performance front-end readout and time-tagging circuits capable of operating at cryogenic temperature (4-20 K) at low power [4].

In the field of high energy particle physics, tracking detectors capable of achieving 5–25 ps timing resolution are necessary for many proposed future particle colliders including the Muon Collider [5], the FCC-hh [6, 7], and the Electron–Ion Collider (EIC) [8]. Extracting precision timing information from low gain avalanche detectors (LGAD), which is a leading candidate detector technology for precision timing tracking detector systems and has been demonstrated to achieve 20–30 ps time resolution [9–13], is an important representative challenge in particle physics. These future detectors aim to implement sensors with pixels as small as 25×25 μm^2. While the power of the front-end amplifier for these detectors will benefit from the significant reduction in input capacitance associated with the increased granularity, the comparator and the TDC will not, and therefore the contribution to power from TDC will become among the dominant contributions to the total power budget.

As such, the design and implementation of low-power front-end electronics capable of extracting precision timing information from LGAD sensors represents a key technical milestone. Our two-step time-to-digital-converter is designed to minimize power and area consumption while providing picosecond resolution. Our design leverages back-gate biasing in the GlobalFoundries 22FDX silicon-on-insulator node as a novel tuning mechanism for delay stages, as well as a compensation strategy to enable operation from 4 Kelvin to room temperature.

In this paper, we present the design and performance characterization of our Time-to-Digital Converter (TDC) ASIC. Its performance is characterized as a function of the delay between the start and stop signals, and the TDC resolution is measured as a function of the back-gate tuning voltage. Finally, the timing jitter performance of the TDC is measured using the discriminator output signals from the Fermilab Constant Fraction Discriminator (FCFD) ASIC, presented in [14], which converts signal pulses into discriminated waveforms robust against amplitude-induced time-walk, mimicking the output signal of an LGAD detector.

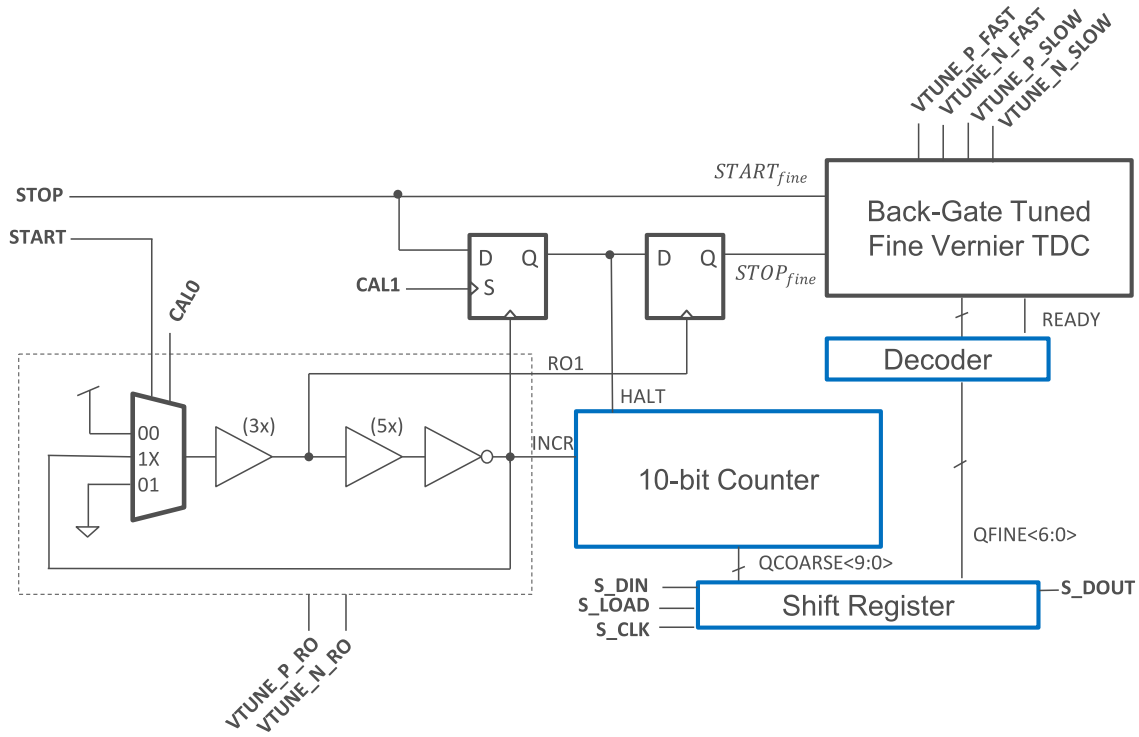

Figure 1: A block diagram of the TDC ASIC design, showing the coarse ring oscillator, DFF interlock, fine Vernier TDC, and serial readout. Bolded signals are inputs or outputs of the test ASIC.

2. TDC Design and Readout

The design of precision Time-to-Digital Converters (TDCs) involves a trade-off between figures of merit. Compact, low-power TDCs are highly desirable for quantum communication applications in order to be closely integrated with cryogenic control and readout electronics, as well as for particle tracking applications where a large number of channels must be integrated to disambiguate particle tracks. However, fine time resolution, which implies both a small bin size and low jitter, cannot be sacrificed in either application, and sufficient dynamic range is necessary to allow synchronization with a distributed system reference clock.

The TDC we present is designed with a two-step architecture consisting of a ring-oscillator coarse TDC and a linear Vernier delay line fine TDC. It makes novel use of the back-gate biasing capabilities of the GlobalFoundries 22FDX node to provide fine-tuning for both stages, as well mitigating undesirable effects of cryogenic operation. A single-channel prototype TDC is implemented with simple, low-speed readout capabilities, laying the groundwork for a second ASIC integrating many channels with readout and synchronization logic.

2.1. Time-to-Digital Converter Design

A generalized Time-to-Digital Converter produces a digital code which represents the time interval T_{in} between the rising edges of two signals, generally termed *start* and *stop*. A two-step TDC like the design we present consists of two components: a "coarse" TDC which produces an output digital code Q_{coarse} such that $T_{in} \approx T_{lsb(coarse)}Q_{coarse}$, and a "fine" TDC which measures the error between the coarse prediction and the actual time interval, producing an output Q_{fine} such that $T_{in} = T_{lsb(coarse)}Q_{coarse} + T_{lsb(fine)}Q_{fine}$.

Two-step TDCs can typically outperform single-step TDCs in terms of the combination of dynamic range and resolution, since the circuits which allow a fine TDC to achieve high resolution typically scale poorly

for large values of T_{in}. However, a critical concern for two-step TDCs is the method of coupling signals between the two stages, which must not introduce undue jitter or nonlinearity.

The two-step architecture of our TDC (see Fig. 1) follows closely from the design reported by Enomoto et al. [15], which uses a two-DFF interlock to couple signals between a coarse ring oscillator and a fine Vernier TDC. The basic operation of the TDC is as follows:

1. When the *start* signal arrives, the ring oscillator begins to oscillate, and the coarse TDC begins to count.
2. When the *stop* signal arrives, it immediately asserts the start input to the fine TDC ($start_{fine}$).
3. On the next assertion of the clock input to DFF1, *HALT* is asserted, and the coarse TDC count is frozen.
4. On the next assertion of the clock input to DFF2, the stop input to the fine TDC is asserted ($stop_{fine}$). The fine TDC completes its calculation of the difference between $start_{fine}$ and $stop_{fine}$.

The use of two sequential flip-flops ensures that there is always a fixed delay T_{gd} between the halting of the coarse TDC and the assertion of $stop_{fine}$. It also suppresses any metastability that results from the clock and data inputs of DFF1 changing simultaneously before that metastability can propagate to the fine TDC.

The relationship between T_{in} and the TDC digital codes may be derived as follows:

$$T_{in} = T(stop) - T(start) \tag{1}$$

Letting $T(start) = 0$ and noting that the *stop* signal directly triggers $stop_{fine}$ we have:

$$T_{in} = T(stop_{fine}) \tag{2}$$

$$T_{in} = T(stop_{fine}) - T(start_{fine}) + T(start_{fine}) \tag{3}$$

The characteristic equation of the fine TDC is: $T_{lsb(fine)}Q_{fine} = T(stop_{fine}) - T(start_{fine})$, which yields:

$$T_{in} = T_{lsb(fine)}Q_{fine} + T(start_{fine}) \tag{4}$$

Finally, due to the fixed propagation delay from DFF1 through DFF2, we note that: $T(start_{fine}) = T_{lsb(coarse)}Q_{coarse} + T_{gd}$, so we have:

$$T_{in} = T_{lsb(fine)}Q_{fine} + T_{lsb(coarse)}Q_{coarse} + T_{gd} \tag{5}$$

The three calibration parameters $T_{lsb(fine)}$, $T_{lsb(coarse)}$, and T_{gd} may be calculated by applying pulses of known length to the input of the TDC. After establishing these values, T_{in} may be calculated from Q_{coarse} and Q_{fine}.

It should be noted that some fixed offset T_{off} is practically present in any TDC due to wire delays and fixed mismatches, which must be calibrated for. In our TDC, this is absorbed into T_{gd}. Thus the use of the fixed flip-flop interlock does not introduce a new calibration parameter.

The coarse and fine TDC are both constructed of inverter-based delay cells. The coarse TDC is a ring oscillator composed of a loop of delay cells whose total delay determines $T_{lsb(coarse)}$. The fine TDC is a Vernier TDC (Fig. 2), a structure which uses two delay lines with slightly different delays to achieve sub-gate-delay timing resolution. The delay per stage of the delay lines attached to *start* and *stop* are t_1 and t_2 respectively, with $t_1 > t_2$ such that the rising edge of *stop* eventually catches up to the rising edge of *start*. The delay between *start* and *stop* should shrink by $t_1 - t_2 = T_{lsb(fine)}$. At each stage, a latch (in the case of our TDC, a simple SR latch) compares which signal arrived first. The number of stages after which the *start* signal no longer arrives before the *stop* signal yields Q_{fine}.

Our TDC leverages the back-gate bias capabilites of the GlobalFoundries 22FDX fully-depleted silicon-on-insulator (FDSOI) process [16] to set the delay of each cell. Six total tuning voltages are exposed: NMOS and PMOS back-gate bias voltages for the ring oscillator, and for the slow and fast delay lines of the fine TDC.

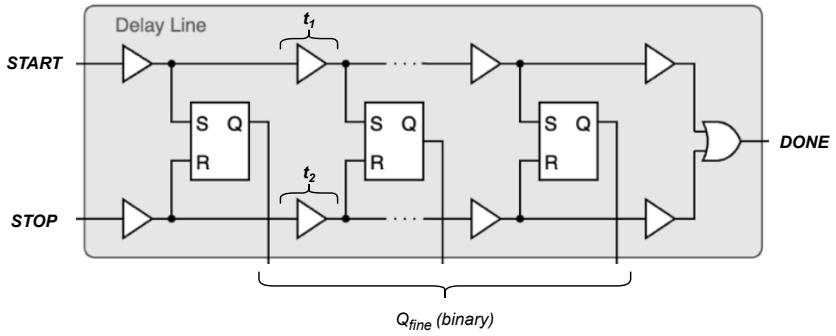

Figure 2: A diagram of a Vernier Delay Line based fine TDC. The TDC is tuned such that $t_1 - t_2 = T_{lsb(fine)} > 0$

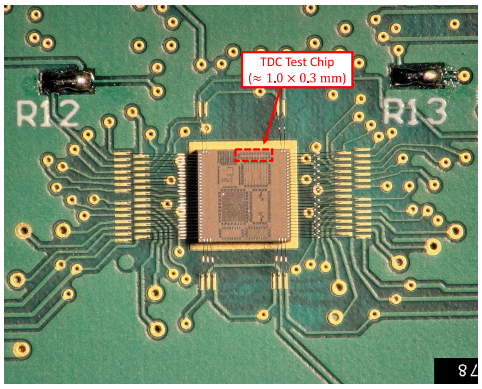

Figure 3: A die photograph of the TDC.

This technique dramatically simplifies the design and shrinks layout area by eliminating all of the auxiliary circuits which are typically required for delay cell tuning using traditional current-starving or capacitive-loading techniques. Crucially, the back-gate bias voltages can be used to forward body-bias transistors to negate the characteristic threshold voltage increase observed at cryogenic temperatures [17], and to compensate for cryogenic temperature shift, maintaining the same TDC resolution across temperature. The design of the fine TDC, in particular, is simplified, as the "fast" and "slow" delay lines are manufactured identical to each other: the difference $\Delta t_2 - \Delta t_1 = T_{lsb(fine)}$ is entirely created by biasing the two delay lines at slightly different bias voltages.

2.2. Test ASIC

We implemented, manufactured, and tested a single-channel prototype of this TDC in GlobalFoundries 22FDX (Fig. 3). The TDC core described above was integrated with simple interfaces and a serial readout to enable testing and debugging, which are described in this section. In some cases, these interfaces limit the performance of the TDC.

A second version of this TDC has also been designed, which is currently under test. This future TDC version incorporates thirty-two channels which are synchronized to a shared reference clock using an on-ASIC PLL. Additionally, this version uses a sophisticated asynchronous readout architecture which is designed to allow all channels to be read out at full rate using 1 Gbps LVDS links.

In the test ASIC, all digital signals including *start* and *stop* are 1.8 V non-return-to-zero (NRZ) CMOS signals, driven by dedicated I/O cells. In an optimized system, the high-speed interfaces would be co-designed with the intended sensor. In the test ASIC, all six TDC core tuning voltages are exposed as

I/Os for manual tuning, along with two additional tuning voltages which control the back-gate bias voltage applied to digital circuits, primarily for the purpose of compensating for cryogenic threshold voltage shift. Finally, the use of a local ring oscillator to drive the coarse TDC is not intended to be scalable due to the limits of accumulated jitter and variability between channels; a single-ended ring oscillator like the one in this design will also suffer from inherently very limited supply rejection [18], which we did not measure. The next version of the TDC will not face this issue due to its on-ASIC PLL.

In this prototype ASIC, programming configuration bits and reading out Q_{coarse} and Q_{fine} are both accomplished using a simple shift register. Each TDC count must be read from the shift register by an external controller before another count can be taken, which is the primary limit on readout speed in our tests reported below. The TDC architecture is designed to operate at 100 Mcounts/s; it is limited by the time taken for the Vernier delay line to converge on a value of Q_{coarse}.

The prototype TDC is implemented as a stand-alone sub-block in a larger 3.0 mm × 3.0 mm ASIC (Fig. 3). The block dimensions of 0.3 mm × 1.0 mm are dominated by the pad ring, while the TDC channel itself is 20 µm × 150 µm.

3. TDC ASIC Characterization

We characterize the TDC ASIC by measuring the TDC resolution as a function of the back-gate tuning voltage, the TDC jitter as a function of the delay between the start and stop signals (T_{in}), and the TDC power as a function of the count rate.

3.1. Readout

In our experiment, a microcontroller (Arduino Portenta) is used for digital control and readout of the ASIC, as shown in Figure 4. The microcontroller interfaces with the ASIC through a simple serial interface (S_CLK, S_DIN, S_DOUT). In order to prevent shift register action from affecting the internal state of the TDC, two additional signals gate the transfer of data between the shift register and the TDC's internal shadow registers: S_PASS is asserted to pass control bits from the shift register into the shadow registers, and S_LOAD is asserted to retrieve data (i.e. Q_{coarse} and Q_{fine}) from the shadow registers and place that data in the scan chain.

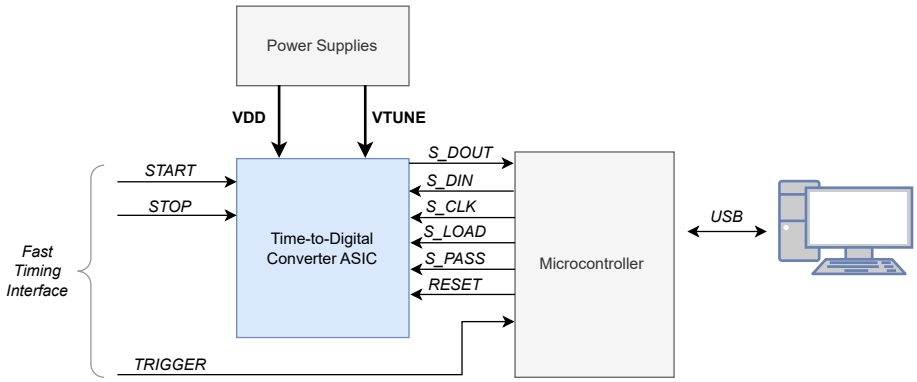

Figure 4: A block diagram illustrating the interfaces between our TDC ASIC and our test setup, including power, digital readout / control, and fast timing interfaces.

A trigger signal is supplied directly from the timing source to the microcontroller, which tells the microcontroller when to retrieve a new measurement from the ASIC. The precise timing of the trigger signal is unimportant: Q_{coarse} and Q_{fine} are determined exclusively by $T_{in} = T(stop) - T(start)$. However, one trigger pulse must be sent for each START/STOP pair to ensure the microcontroller retrieves the current count before it is overwritten by the next count.

3.2. ASIC Characterization

For independent characterization of our TDC we used a Berkley Nucleonics Model 745-OEM Digital Delay Generator to supply the START/STOP and trigger signals. The 745-OEM instrument has a delay resolution of 1 ps and specified RMS jitter of better than $T_{j,rms} = 5$ ps + delay x 10^{-8}, or approximately 5 ps for signals in the range of interest. The jitter of our specific instrument was measured to be 3.5 ps using a 20 GHz oscilloscope at 2 ns delay.

To calibrate the TDC for each test condition, we performed measurements of three fixed input time differentials (0ps, 100ps, and 10ns) supplied by the 745-OEM and averaged the TDC response for each over a large number of cycles to mitigate jitter. This yielded a system of three equations which can be solved for the calibration constants $T_{lsb(fine)}$, $T_{lsb(coarse)}$, and T_{gd} (see Sec 2).

3.3. TDC Resolution vs Tuning Voltage

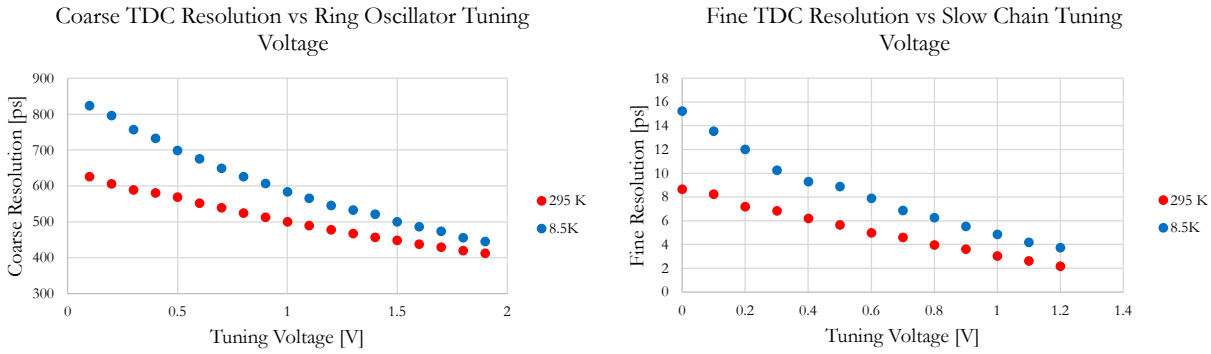

Figure 5: Resolution of the coarse and fine TDCs as a function of back-gate tuning voltage.

In order to assess the tunability of the ASIC, we define two tuning parameters $V_{tune(coarse)}$ and $V_{tune(fine)}$. The actual tuning voltages for the ASIC are derived from these parameters as shown in Table 1. The expressions are defined such that an increase in $V_{tune(coarse)}$ decreases the coarse TDC resolution, and an increase in $V_{tune(fine)}$ decreases the fine TDC resolution, while keeping NMOS and PMOS drive strengths roughly balanced. Nominal values are $V_{tune(coarse)} = 1V$ and $V_{tune(fine)} = 0.55V$.

ASIC Tuning Voltage	**Expression from Tuning Parameters**
VTUNE_N_RO	$V_{tune(coarse)}$
VTUNE_P_RO	$2 - V_{tune(coarse)}$
VTUNE_N_FAST	1.9 V (fixed)
VTUNE_P_FAST	0.1 V (fixed)
VTUNE_N_SLOW	$V_{tune(fine)}$
VTUNE_P_SLOW	$2 - V_{tune(fine)}$

Table 1: Expressions for ASIC tuning voltages as a function of tuning parameters.

To generate each of the two plots in Figure 5 we swept one tuning parameter while keeping the other constant. For each tuning voltage value, we took three measurements of known-length pulses and recorded the output code from the TDC, then solved this system of three equations as described in 2.1 to find the coarse and fine TDC resolution $t_{R(coarse)}$ and $t_{R(fine)}$, which are plotted.

When tuning voltage is held constant, we observe that a larger resolution is measured at cryogenic (8.5 K) temperature versus room temperature. This effect primarily results from the well-known threshold shift of CMOS devices at cryogenic temperature [19], which increases the propagation delay of both ring oscillator stages and Vernier delay line stages [20]. This effect can be mitigated in some cases by choosing a different tuning voltage to compensate for threshold voltage shift. Due to larger overall delays, the tuning slope is also approximately twice as large at cryogenic temperatures: we measured 216 ps/V (coarse) and 9.59 ps/V (fine) at 8.5K, versus 118 ps/V (coarse) and 5.40 ps/V (fine) at room temperature.

3.4. TDC Jitter

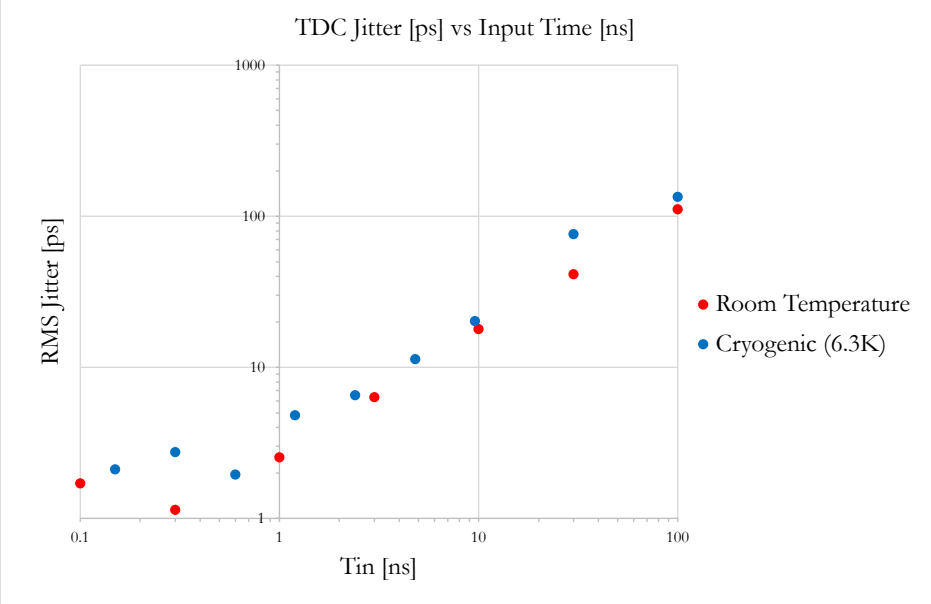

Figure 6: TDC jitter results as a factor of $T_{in} = T(stop) - T(start)$. See note below on temperature.

We assessed the jitter of our TDC in isolation by fixing the START/STOP delay (T_{in}) and taking a large number of samples to build a code distribution. Results as a function of T_{in} are shown in Fig 6. For small values of T_{in} the jitter of 745-OEM instrument dominates, resulting in an approximately flat jitter value in the range of a few picoseconds. For larger values of T_{in}, accumulated flicker noise around the ring oscillator is the dominant noise source, resulting in a roughly linear correlation between jitter and T_{in}. Future ASICs, in which the ring oscillator is replaced by a high-quality PLL, will not exhibit the same jitter accumulation.

We measured the performance of the TDC at both room temperature and cryogenic temperature (6.3 degrees Kelvin). The measurement temperature differs from the previous experiment (8.5K) because different instrumentation of our closed-cycle cryostat results in a different heat load and thus a different minimum achievable temperature.

Because the contribution of thermal noise is already small (<1 ps rms, from simulation) and flicker noise is not reduced by low temperature [21], no significant advantage is obtained from cryogenic operation. In fact, because the tuning voltage is identical, the cryogenic TDC resolution is slightly larger, resulting in slightly higher jitter.

3.5. TDC Power

Our TDC operates in an asynchronous, event-driven fashion, which means that its power consumption is highly dependent on the rate of counts, as well as the average time (t_{RO}) that the ring oscillator must be active in order to resolve each count, which is dependent on the length of START and STOP pulses. For test

purposes, we can control the value of t_{RO} arbitrarily by setting the length of these pulses. Figure 7 illustrates power consumption at cryogenic and room temperature up to 1 Mcps, the limit of our test stand, for t_{RO} values of 100 and 200 nanoseconds. We observe that both quiescent and dynamic power consumption are reduced at cryogenic temperature, due to lower leakage current and slower operation of the TDC at nominal tuning levels.

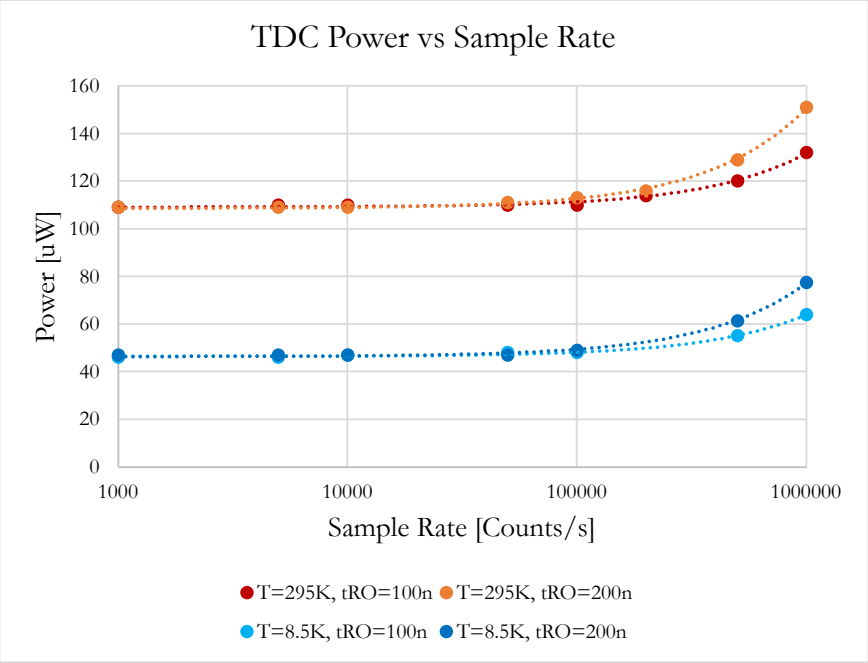

Figure 7: Measured TDC power as a factor of temperature, count rate, and average ring oscillator run time per count (t_{RO}) for count rates up to 1 M counts per second, the limit of our test stand.

Although our test stand is only capable of driving pulses up to 1 Mcps, the TDC is capable of operating with input count rates of at least 100 Mcps. Using the data from Figure 7, we can estimate the breakdown of power consumption per block, and use these numbers to estimate power at 100 Mcps as $P(f_{samp}) = P_{RO}t_{RO}f_{samp} + E_{fine}f_{samp} + P_{Quiescent}$. To calculate the power figures of merit in Table 3.5, we assume $t_{RO} = 10ns$, which means that at an input count rate of 100 Mcps, the ring oscillator is constantly running, which is a conservative estimate.

Figure of Merit	**295 K**	**8.5 K**
Quiescent Power ($P_{Quiescent}$, µW)	109	46.6
Energy per fine ADC Conversion (E_{fine}, pJ)	3.30	3.03
Ring Oscillator Power (P_{RO}, µW)	193	142
Estimated Channel Power at 100 kcps (µW)	110	47
Estimated Channel Power at 100 Mcps (µW)	632	492

Table 2: TDC channel power for count rates of 100 kcps and 100 Mcps, assuming $t_{RO} = 10ns$

3.6. Summary of Figures of Merit

The figures of merit of the TDC design are presented in Figure 8. The figures in the table are calculated by setting the TDC tuning voltages to their nominal settings, and conservatively assuming an input count

rate of 100 Mcps and $t_{RO} = 10ns$. In reality, the TDC's power and resolution are highly dependent on count rate and tuning voltages as detailed in the pervious sections. The range of our TDC is practically limited by the accumulation of jitter on the ring oscillator; given a maximum jitter specification for the TDC, the maximum allowable range is the T_{in} value which corresponds to that level of jitter in Figure 6. To avoid making an arbitrary assumption about required jitter, we do not report a single range value in this table.

	2019 TCASI	2019 JSSC	2023 JSSC	2014 JSSC	2018 JSSC	This Work	
Architecture	Nutt+Cyclic Interpolator	Dynamic Reallocation + dual clock	GRO + Cont. Counter	Pipeline	RNS	Ring Oscillator + Vernier TDC	
Technology (nm)	350	180	180	65	45	22 FDSOI	
Resolution (ps)	19.5	48.8	100	1.12	9.4	295K	8.5K
						6.20	8.52
TDC Area (mm^2)	0.03	0.025	-	0.14	0.08	0.003	
TDC Power (mW)	2.04	2.9	0.5	15.4	24.2	295K	8.5K
						0.63	0.49
Dynamic Range (ns)	640	200	96	0.578	4.6	**	
Conversion Rate (MS/s)	9.17	666	50	250	215	100	

Figure 8: Summary of figures of merit compared to other recent TDC designs.

4. TDC Characterization Using Emulated LGAD Signals

We characterize the performance of our TDC using emulated and realistic LGAD signals provided by the FCFD front-end readout ASIC [14], which achieves a time resolution better than 9 ps. The FCFD ASIC generates discriminated LGAD signal pulses using an internal charge injection circuit triggered by a 745-OEM pulse generator. These pulses are used as inputs to the TDC ASIC for evaluation. The experimental setup, including the readout and data acquisition systems, is described, and photographs of the test board containing the FCFD ASIC connected to the LGAD sensor are shown in Figure 9.

To start, we first measure the timing jitter using signals generated by the 745-OEM pulse generator. A schematic diagram of the pulse generator measurement setup is shown on the top right of Figure 9. The signal waveforms for a characteristic event produced by the pulse generator that enter as input to the TDC are shown on the left of Figure 10.

Next, we perform the charge injection study. The schematic diagram of the charge injection study setup is shown on the bottom right of Figure 9. The FCFD output is used as the start signal for our TDC, while the second output of the pulse generator is used as the stop signal. In order to ensure that the stop signal from the pulse generator arrives later than the start signal from the FCFD output, we introduce a physical delay using longer cables for the pulse generator output. The signal waveforms for a typical event produced by the charge injection testing setup described above are shown on the right of Figure 10, illustrating that the FCFD output signal is typically short with a width of 10 ns.

4.1. Sensor Testing Results

We first characterize the performance of the TDC ASIC using the pulse generator, which, as discussed in Section 4, generates both the start and stop signals. The Arduino-based readout system is used to collect the start and stop time stamps and the elapsed time (Δt) between the start and stop signals is digitized and

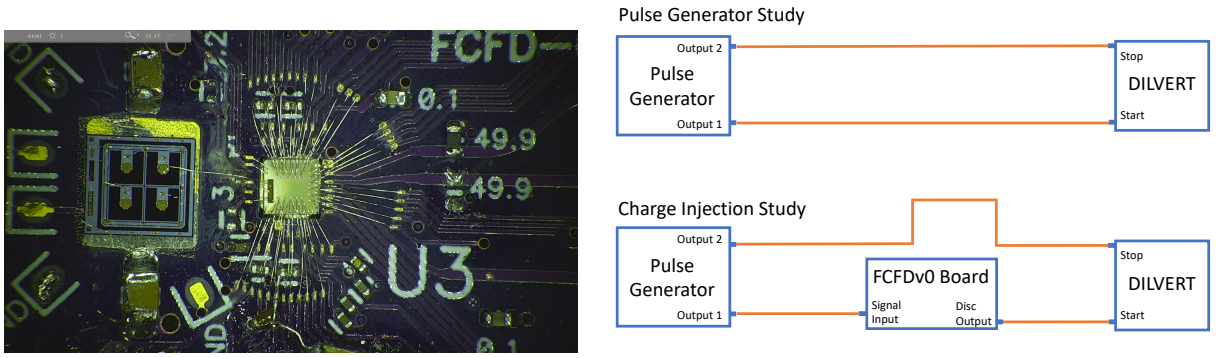

Figure 9: A photograph of the FCFD characterization board with an LGAD sensor mounted showing the FCFD wire-bonded to the readout board and to the LGAD sensor(left). On the right, schematic diagrams of the pulse generator test measurement (top-right) and the FCFD charge injection test measurement (bottom-right) are shown.

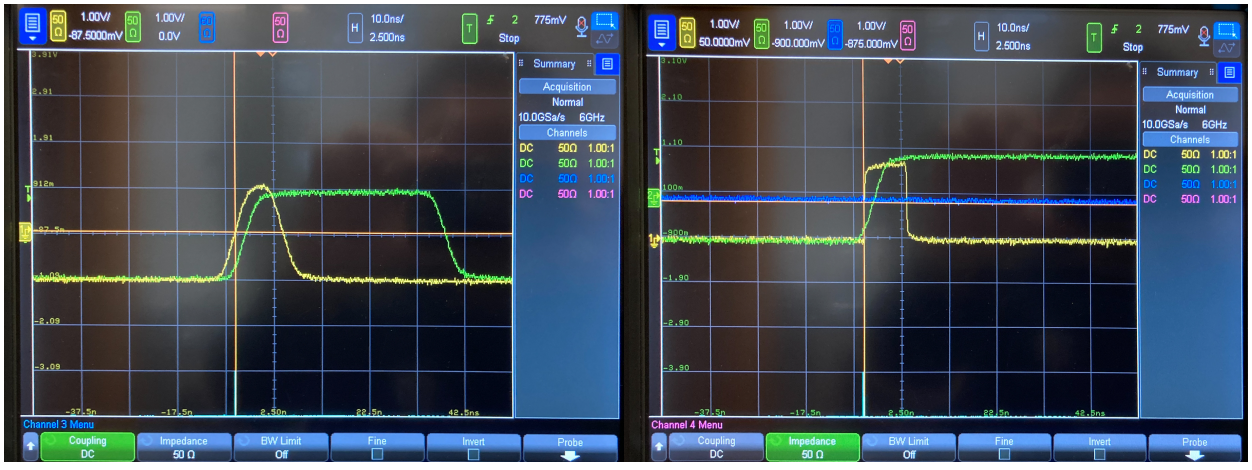

Figure 10: Waveforms of the signals tested acquired by oscilloscope. Left: waveforms for two pulse generator signals to represent the start and stop signals. Right: waveforms for the charge injection trigger (green) and FCFD response (yellow).

stored to file. We plot a histogram of the Δt distribution on the left of Figure 11, and fit the distribution to a Gaussian function to extract its σ parameter as the resolution. We measure a resolution of 3.5 ps, consistent with design expectations.

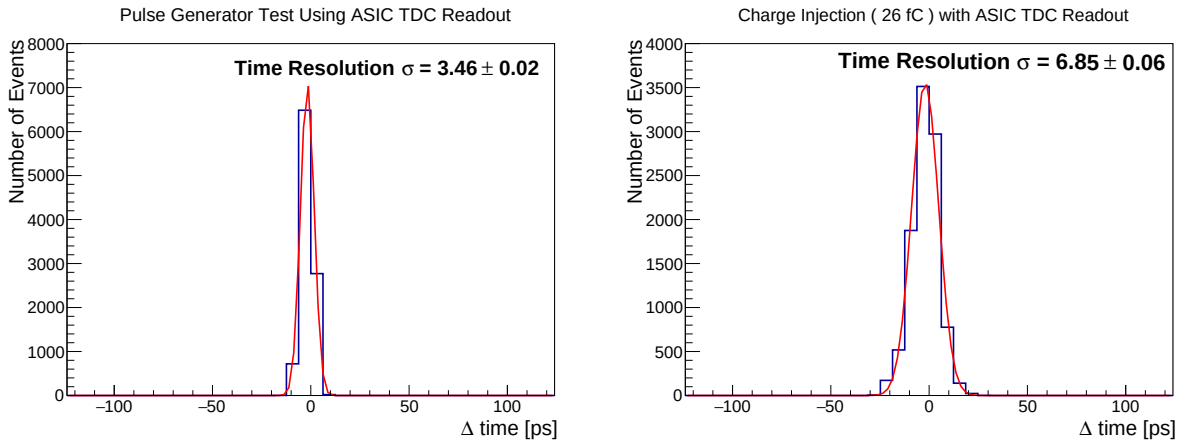

Figure 11: Histograms of the measured time difference between the start and stop signals using our TDC readout for the pulse generator test (left) and one of the charge injection measurements (right).

After confirming the expected performance of our TDC, we employ it to measure timestamps for realistic signals using the internal charge injection mechanism built into the FCFD ASIC. The FCFD discriminator output is used as the start signal and the pulse generator signal used to trigger the charge injection mechanism is used as the stop signal. Both signals are sent to our TDC and the Δt values are digitized by the Arduino-based readout system. On the right of Figure 11, we show the histogram of Δt values for a particular charge injection dataset corresponding to injected signals with charge of 26 fC. The same Gaussian function fit is performed and the time resolution is extracted as the standard deviation σ of the fitted Gaussian. Using the built-in switches of the FCFD ASIC, we can measure the time resolution for various datasets corresponding to signals with injected charge ranging from 1–30 fC. The results are shown in Figure 12 as a function of the injected charge, and are consistent with past measurements using an oscilloscope readout [14]. These measurements confirm that the contribution of the TDC to the time resolution of the full system is below 4 ps, achieving the original design parameters.

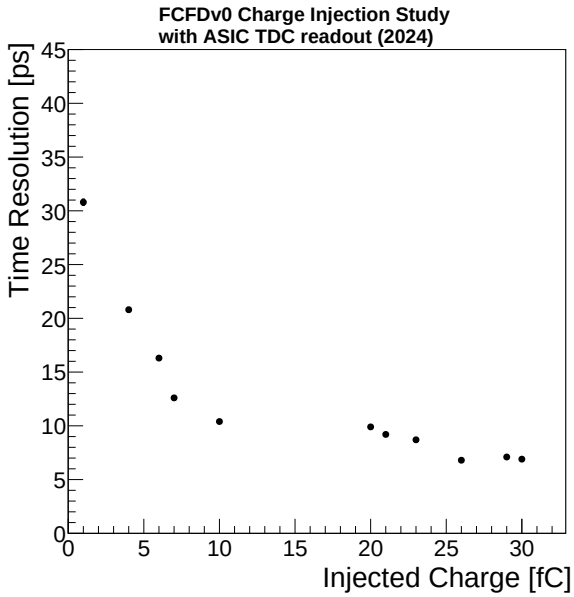

Figure 12: The measured time resolution is shown as a function of the injected charge. The internal charge injection mechanism of the FCFD ASIC is used to produce signals and the TDC ASIC is used to read out and digitize the time stamps.

5. Conclusions and Outlook

Development of low-power, high-resolution TDCs for applications in high precision timing is one of the key challenges towards implementation of large-scale 4D-tracking detectors. Similarly, applications with novel quantum sensors require very high precision TDCs that are capable of operating in ultra-cold environments.

In this paper we presented a novel TDC design architecture, and the characterization results of the test ASIC in various configurations, at both room and cryogenic temperature. The design makes use of the back-gate biasing capabilities of the GlobalFoundries 22FDX node to provide fine-tuning for the coarse and fine TDC stages. Using the GF 22FDX node allowed us to design a low complexity, small footprint TDC with no noise contribution from bias circuits and separate tuning voltages. Our measurements using both a pulse generator and a dedicated LGAD front-end readout ASIC demonstrate that the compact TDC design achieves better than 4 ps timing resolution, with a power consumption below 630 and 110 μW at 100 and 0.1 Mcounts/second respectively.

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References

[1] R. Valivarthi, S. I. Davis, C. Peña, S. Xie, N. Lauk, L. Narváez, J. P. Allmaras, A. D. Beyer, Y. Gim, M. Hussein, G. Iskander, H. L. Kim, B. Korzh, A. Mueller, M. Rominsky, M. Shaw, D. Tang, E. E. Wollman, C. Simon, P. Spentzouris,

D. Oblak, N. Sinclair, M. Spiropulu, Teleportation systems toward a quantum internet, PRX Quantum 1 (2020) 020317. doi:10.1103/PRXQuantum.1.020317.
URL https://link.aps.org/doi/10.1103/PRXQuantum.1.020317
[2] D. Berry, et al., 4-Dimensional Trackers (2022). arXiv:2203.13900.
[3] B. Korzh, Q.-Y. Zhao, J. P. Allmaras, S. Frasca, T. M. Autry, E. A. Bersin, A. D. Beyer, R. M. Briggs, B. Bumble, M. Colangelo, et al., Demonstration of sub-3 ps temporal resolution with a superconducting nanowire single-photon detector, Nature Photonics 14 (4) (2020) 250–255.
[4] J. Chang, J. Gao, I. Esmaeil Zadeh, A. W. Elshaari, V. Zwiller, Nanowire-based integrated photonics for quantum information and quantum sensing, Nanophotonics 12 (3) (2023) 339–358.
[5] C. Accettura, et al., Towards a Muon Collider (2023). arXiv:2303.08533.
[6] E. Sicking, Detector requirements for future high-energy collider experimentsTREDI 2020, Vienna, Austria (2020).
URL https://indico.cern.ch/event/813597/contributions/3727952/
[7] C.-E. Wulz, Report from ecfa, the european committee for future accelerators, EPJ Web of Conferences 95 (2015) 06003. doi:10.1051/epjconf/20149506003.
[8] R. Abdul Khalek, et al., Science Requirements and Detector Concepts for the Electron-Ion Collider: EIC Yellow Report, Nucl. Phys. A 1026 (2022) 122447. arXiv:2103.05419, doi:10.1016/j.nuclphysa.2022.122447.
[9] A. Apresyan, W. Chen, G. D'Amen, K. F. Di Petrillo, G. Giacomini, R. Heller, H. Lee, S. Los, C. S. Moon, A. Tricoli, Measurements of an AC-LGAD strip sensor with a 120 GeV proton beam, JINST 15 (09) (2020) P09038. arXiv:2006.01999, doi:10.1088/1748-0221/15/09/P09038.
[10] R. Heller, C. Madrid, A. Apresyan, W. Brooks, W. Chen, G. D'Amen, G. Giacomini, I. Goya, K. Hara, S. Kita, S. Los, A. Molnar, K. Nakamura, C. Peña, C. S. Martín, A. Tricoli, T. Ueda, S. Xie, Characterization of BNL and HPK AC-LGAD sensors with a 120 GeV proton beam, JINST 17 (05) (2022) P05001. arXiv:2201.07772, doi:10.1088/1748-0221/17/05/p05001.
[11] C. Madrid, et al., First survey of centimeter-scale AC-LGAD strip sensors with a 120 GeV proton beam (2022). arXiv:2211.09698.
[12] J. Ott, et al., Investigation of signal characteristics and charge sharing in ac-lgads with laser and test beam measurements, Nucl. Instr. and Meth. A 1045 (2023) 167541. doi:https://doi.org/10.1016/j.nima.2022.167541.
[13] M. Tornago, R. Arcidiacono, N. Cartiglia, et al., Resistive ac-coupled silicon detectors: Principles of operation and first results from a combined analysis of beam test and laser data, Nucl. Instr. and Meth. A 1003 (2021). doi:https://doi.org/10.1016/j.nima.2021.165319.
[14] S. Xie, A. Apresyan, R. Heller, C. Madrid, I. Dutta, A. Hayrapetyan, S. Los, C. Pena, T. Zimmerman, Design and performance of the Fermilab Constant Fraction Discriminator ASIC, Nucl. Instrum. Meth. A 1056 (2023) 168655. arXiv:2306.07387, doi:10.1016/j.nima.2023.168655.
[15] R. Enomoto, T. Iizuka, T. Koga, T. Nakura, K. Asada, A 16-bit 2.0-ps resolution two-step tdc in 0.18- μ m cmos utilizing pulse-shrinking fine stage with built-in coarse gain calibration, IEEE Transactions on Very Large Scale Integration (VLSI) Systems 27 (1) (2019) 11–19. doi:10.1109/TVLSI.2018.2867505.
[16] S. Ong, L. Chan, K. Chew, C. Lim, W. L. Oo, A. Bellaouar, C. Zhang, W. Chow, T. Chen, R. Rassel, J. Wong, C. Wan, J. Kim, W. Seet, D. Harame, 22nm fd-soi technology with back-biasing capability offers excellent performance for enabling efficient, ultra-low power analog and rf/millimeter-wave designs, in: 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2019, pp. 323–326. doi:10.1109/RFIC.2019.8701768.
[17] C. Enz, A. Beckers, F. Jazaeri, Cryo-cmos compact modeling, in: 2020 IEEE International Electron Devices Meeting (IEDM), IEEE, 2020, pp. 25–3.
[18] B. Razavi, The ring oscillator [a circuit for all seasons] (2019). doi:10.1109/mssc.2019.2939771.
URL http://dx.doi.org/10.1109/MSSC.2019.2939771
[19] W. Clark, B. El-Kareh, R. Pires, S. Titcomb, R. Anderson, Low temperature cmos-a brief review, Components, Hybrids, and Manufacturing Technology, IEEE Transactions on 15 (1992) 397 – 404. doi:10.1109/33.148509.
[20] H. Bohuslavskyi, S. Barraud, V. Barral, M. Cassé, L. Le Guevel, L. Hutin, B. Bertrand, A. Crippa, X. Jehl, G. Pillonnet, A. G. M. Jansen, F. Arnaud, P. Galy, R. Maurand, S. De Franceschi, M. Sanquer, M. Vinet, Cryogenic characterization of 28-nm fd-soi ring oscillators with energy efficiency optimization, IEEE Transactions on Electron Devices 65 (9) (2018) 3682–3688. doi:10.1109/TED.2018.2859636.
[21] G. Kiene, S. İlik, L. Mastrodomenico, M. Babaie, F. Sebastiano, Cryogenic characterization of low-frequency noise in 40-nm cmos, IEEE Journal of the Electron Devices Society (2024).