The CMOS Pseudo-Thyristor: A Zero-Static Current Circuit for Pixelized Detector Front-End Stage

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ABSTRACT: A very low power front-end discriminator circuit for pixelized detectors, called pseudo-thyristor is described in this document. It is a positive feedback topology using regular PMOS and NMOS field-effect transistors (FET's) with zero static current. When a small charge is injected into the circuit, it flips rapidly due to the positive feedback and outputs a logic transition for further digitization. Simulation shows that in 65 nm process, it is possible to achieve a detecting threshold of 5 fC while maintain the average power consumption below 10 micro-Watts when the hit occupancy is < 10% for 40 MHz operation.

KEYWORDS: Front-end electronics for detector readout; Solid state detectors; Timing detectors

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Contents

1. Introduction

In contemporary high energy physics detectors, pixelized detectors, either silicon detectors or Low-Gain Avalanche Detectors (LGADs) are widely used for tracking, timing or calorimeters. As the number of detector elements or pixels continues to increases towards the future, much lower power consumption of the front-end circuits is required or desired. In some applications, power consumption as low as 10 micro-Watts per channel is desired. In typical architecture today, the front-end circuits consist of pre-amplifiers and discriminators, each consumes about 1 milli-Watts power for 65-180 nm CMOS fabrication processes and this is a factor of 100 higher than what's desired in the future. To reduce the power consumption by up to two orders of magnitude, new approaches of the front end design are required. The Pseudo-Thyristor proposed here is a novel CMOS circuit with zero static current for LGAD-like frontend electronics with the potential to have ultra-low power consumption.

The circuit is a positive feedback topology (which is rarely used in analog frontend circuits) using regular PMOS and NMOS field-effect transistors (FET's). The core of the circuit consists of a pair of PMOS and NMOS FET's with the drain and gate terminals of them cross connected to form a positive feedback loop. When a small amount of electric charges is injected into the NMOS gate, both the NMOS and PMOS FET's are turned from OFF to ON state similar as a thyristor, except that in both ON and OFF states, the static current of the circuit is almost zero (with small leakage currents in deep nanometer fabrication processes) as in most digital CMOS circuits. The circuit converts a signal with a small charge into a logic level transition and later resets from ON to OFF state with a set of MOS FET's.

Intrinsically, in typical architecture today, the transistors in the amplifiers and discriminators must operate with a static current so that the transistors are in high conductivity region to follow the input pulse at high speed. The topologies used in amplifiers usually employs deep negative feedback to improve bandwidth and linearity.

However, in pixelized detectors, full waveform information is usually not needed because we usually only care about whether a charged particle passed through a given pixel, or we are also interested in the arrival time of the particle. The full waveform information is also not practical due to the limited data link bandwidth. In many cases, single bit hits indicating the coordinates of the passing points of charged particles in a tracking detector are sufficient. Beyond that, one may digitize the arrival times of the particle hits and sometimes digitize the pulse widths for time walk correction. In these situations, the requirement to the front-end circuit is nothing more than to provide a logic flipping. This requirement can be fulfilled using very low power circuits consuming zero static current. Also, since the detector elements produce only one type of charges (negative charges), symmetric topologies in the front-end circuits are not necessary, which further simplifies the circuits and results in lower power consumption.

While the circuit can be at least utilized for 1-bit hit detection in tracking pixel detectors, timing walk correction is possible when the 4D detection is demanded, although further simulation and testing are needed..

We chose a circuit scheme with positive feedback for fast switching between OFF and ON states that operates like a thyristor. However, unlike a thyristor that needs a static current to maintain the ON state, our front-end circuits consumes zero static currents for both ON and OFF states as in regular CMOS digital circuits. For this reason, we name the circuit as Pseudo-Thyristor Discriminator. In this documents, circuit design of the pseudo-thyristor discriminator is described in Section 2 and simulation results are shown in Section 3, followed with conclusion in Section 4.

2. Design of the Pseudo-Thyristor Discriminator

2.1 Circuit Diagram

Figure 1 illustrates the circuit diagram of the pseudo-thyristor discriminator. The entire circuit is constructed with regular PMOS and NMOS field-effect transistors (FET's) in TSMC 65 nm process.

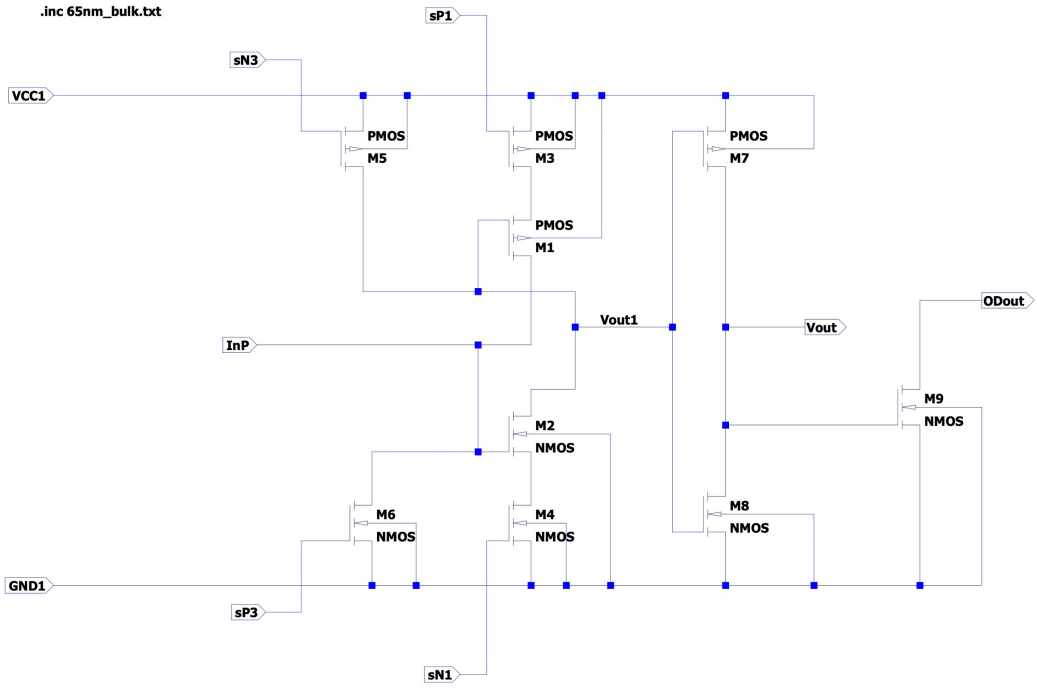

Figure 1. Circuit diagram of the pseudo-thyristor discriminator

The core of the circuit consists of a pair of PMOS (M1)and the NMOS (M2) FET's with the drain and gate terminals of them cross connected to form a positive feedback loop. At standby condition, external control signals sP1=LO and sN1=HI which cause M3 and M4 in ON state while sP3=LO and sN3=HI, causing M6 and M5 in OFF state. After initialization, both M1 and M2 are in OFF state, i.e., the gate of M1 (and the drain of M2) is in HI state while the gate of M2 (and the drain of M1) is in LO state. When a small amount of electric charges (typically several femto-Coulombs) is injected via InP port into the NMOS (M2) gate, after the M2 gate is charged beyond the threshold voltage, both the M2 and M1 are turned from OFF to ON state. Due to positive feedback, the switching process is fast with relatively large instantaneous currents that charge the gates of the FET's in a short amount of time. Once in the ON state, both M1 and M2 are conductive and the gates of M1 and M2 are kept in the LO and HI voltage level, respectively, which maintain both transistors in ON state until the next reset period.

During reset period, sP3 is turned to HI while sN3 is turned to LO causing both M6 and M5 becoming ON. The gates of M1 and M2 are discharged to HI and LO voltage levels, respectively, which force both of them to go OFF state. To prevent shorting power rail that cause large current when M5 and M6 become conductive before M1 and M2 are turned OFF, transistors M3 and M4 are added and controlled by sP1 and sN1 signals. The sP1 and sN1 are flipped slightly earlier than sP3 and sN3 so that they can cut off current paths before M6 and M5 are turned ON. Therefore, the detailed resetting process takes several small steps: (1) M3 and M4 are turned from ON to OFF, (2) M5 and M6 OFF to ON, (3) M1 and M2 ON to OFF, (4) M3 and M4 OFF back to ON, (5) M5 and M6 ON back to OFF. After resetting, M1 and M2 remain OFF until external charges injected into the gate of M1.

The pair of transistors M7 and M8 form a inverting buffer to drive circuits in later stages. The NMOS transistor M9 can be used as an open drain driver.

2.2 An Application Example

An application example of the pseudo-thyristor discriminator interfacing with a negative current source is studied and the circuit diagram is shown in Figure 2.

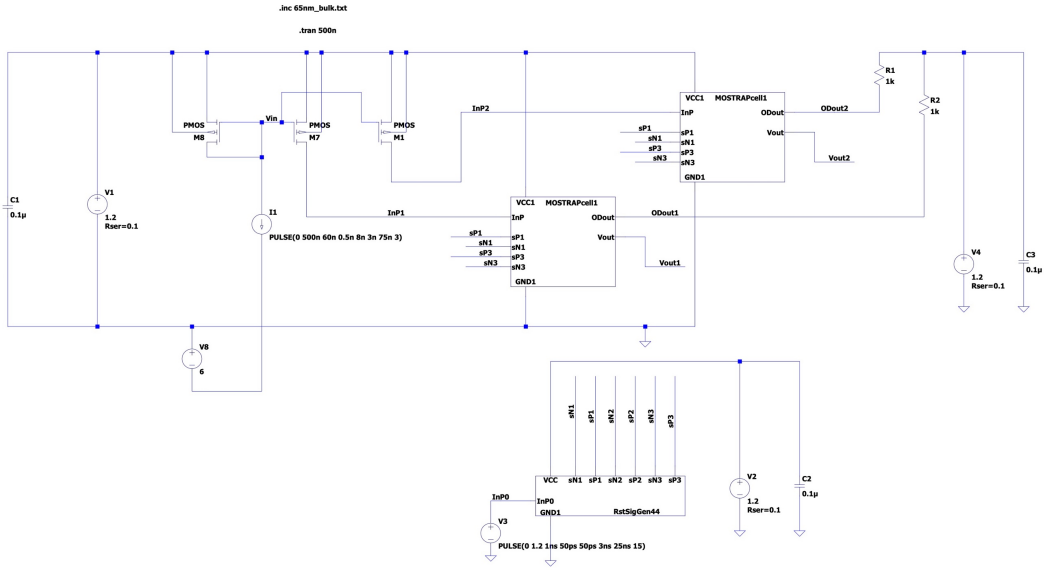

Figure 2. Circuit diagram of the application of pseudo-thyristor discriminator interfacing with a negative current source.

The current source I1 emulates the input from a detector element that generate a short (~10 ns) negative pulse with total charge approximately 5fC. The input current is amplified with a current mirror structure built with M8, M7 and M1. The outputs from M7 and M1 are fed into two identical pseudo-thyristor discriminators in the subcircuit MOSTRAPcell1 blocks with circuit diagram as shown in Figure 1.

The block RstSigGen44 contains a set of inverters and converts the input pulse (InP0) into the control signals sN1, sP1, sN3 and sP3 for reset process as described in previous subsection. In this example, the reset pulse is a 40 MHz periodic signal that emulates resetting the circuits every beam crossing for detectors operating in LHC environment. In fact, the resetting pulse may also be a delayed version of the output logic level, so that the circuit can operate in a self-trigger, self-resetting mode, which we will discuss later.

The outputs of the pseudo-thyristor discriminators Vout1 and Vout2 are used to drive later stages and the open-drain outputs ODout1 and ODout2 are used to drive internal wires with pull-up resistors. The voltage supplies V1, V2 and V4 with some internal resistance are bypassed with capacitors. Note that the values of the resistance and capacitance are not realistic and they are chosen solely for the purpose of measuring the power consumptions of different parts of the circuit conveniently.

In the current mirror, the widths of M7 and M1 are designed to be different so that their outputs have different gains. The gain difference effectively causing the two pseudo-thyristor discriminators to flip with different thresholds of the input charges. For a given input current pulse, the two output logic levels have different flipping times that reflect the pulse height and the time difference is intended to be utilized for time walk correction. Although the time walk correction is yet to be studied.

2.3 Design Considerations

Cautions must be taken during the design of the pseudo-thyristor discriminators. During the standby condition, M1 and M2 in Figure 1 are both in OFF state. The OFF state leakage current of a transistor may charge the gate of the other one which may cause the transistor pair to go to ON state spontaneously via positive feedback if the one of the gates is charged above the conductive threshold. To prevent the transistor pair from spontaneous state changing, the lengths of M1 and M2 are chosen to be relatively large so that they are turned OFF as completely as possible. The transistors M5 and M6, on the other hand, are designed to provide small OFF state leakage currents to maintain M1 and M2 in OFF state.

In standby condition, the transistor M8 is in ON state, leakage current through its gate is not negligible, especially in IC chips fabricated with deep nano-meter processes. The length and width of M8 is chosen to be relatively small and the leakage current of M8 is to be balanced with the OFF state leakage current through the M5 drain.

With appropriate sets of the transistor lengths and widths, the circuit is able to remain in standby condition indefinitely. However, for applications in colliders, periodic resetting is still a reasonable operating mode to reduce fake hit rate and reduce variations of the flipping thresholds.

3. Simulation Results

The operations of the pseudo-thyristor discriminators is simulated in schematic-level with TSMC 65 nm process technology.

3.1 Operations of the pseudo-thyristor discriminators

The simulation is based on an application in a collider with 40 MHz beam crossing as described in Figure 2. The reset pulses generated by V3 in Figure 2 repeat in 25 ns periods with about 3 ns ON state. The external current input is emulated with current source I1 that produces pulses up to 500 nA for about 10 ns, resulting in a total input charge approximately 5 fC.

The reset pulses and the signal input pulses are plotted in the top pane in Figure 3.

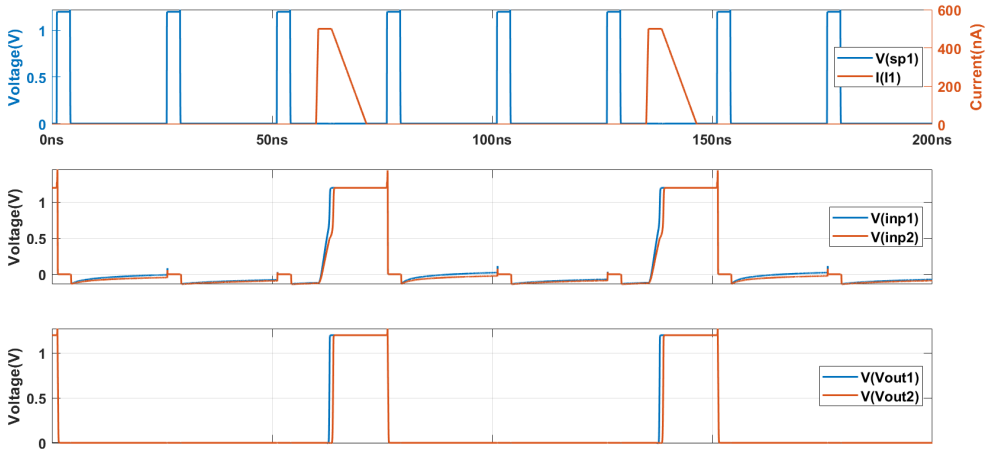

Figure 3. Simulation of the operations of the pseudo-thyristor discriminators

The middle pane shows the voltage at the node InP1 and InP2. The outputs of the current mirrors of the drains of M7 and M1 in Figure 2 charge up the gates of M2 in Figure 1. Since the

mirror ratios for these two outputs are different, the charging speeds of these two nodes are different. They reach the threshold at different time and therefore, the two pseudo-thyristor discriminators flip from OFF to ON state at different time. The time difference can be used to estimate the input pulse height and make time walk correction. If the pulse is higher, the time difference becomes smaller given that the two currents from the current mirrors have a constant relative ratio.

The two pseudo-thyristor discriminators stay at ON state until the reset at the end of each beam crossing.

The bottom pane shows the Vout of the two pseudo-thyristor discriminators. Again the times of their leading edges are different due to different charging threshold for the two branches and their trailing edges are due to reset at the end of beam crossing.

3.2 Power Consumptions

The bottom pane in Figure 4 shows the currents flowing through the voltage supplies V1 and V2 which reflect the power consumptions in different part of the circuit in schematic-level.

In static state, the current flowing through the pseudo-thyristor discriminators and current mirrors is very small as in regular CMOS logic circuits. From the trace of I(V1), the current flowing through power supply V1, one can see a large current pulse due to the operations with an input. The peak of I(V1) is about 5 μA (with the effect of the bypass capacitor and internal resistance), and the average over a short time interval (75 ns in this case) is approximately 1.1 μA. The power consumption in this extreme case (33% hit occupancy) is roughly 1.3 μW. In real applications with pixelized detector, hit occupancy is typically <1% and therefore, the power consumption in this part is very small (<1 μW).

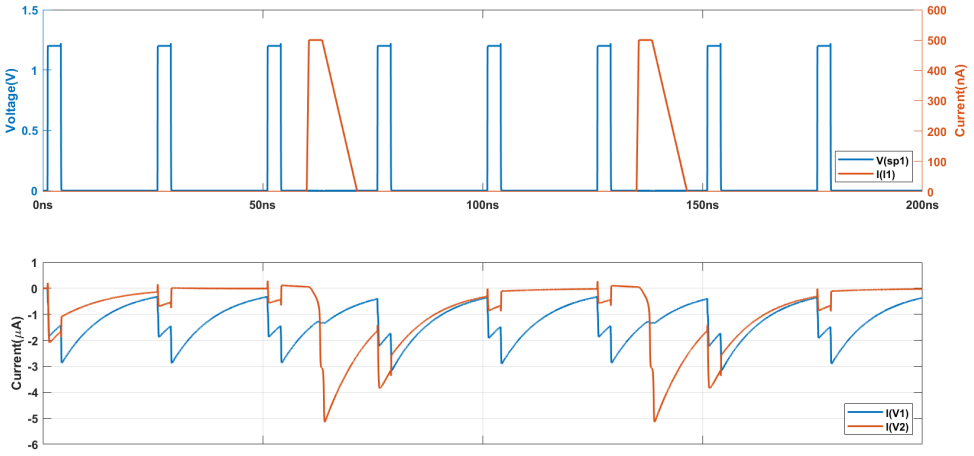

Figure 4. Simulation of the current of the pseudo-thyristor discriminators

The trace I(V2) is the current through the power supply V2, which powers the block RstSigGen44 that produces pulses for resetting process. The peak of this trace is around 3 μA and the average is about 1.3 μA with an average power consumption of about 1.6 μW, which should be acceptable for many applications. Note that this "service" circuit consumes dominating portion of the power in the entire circuit since resetting processes are repeated in all beam crossings.

If a self-trigger self-reset scheme is utilized, much lower total power consumption can be anticipated. However, as mentioned earlier, there are advantages for using periodic resetting approach. It is still possible to optimize the reset pulse generating circuit to further reduce the power consumption.

4. Conclusion and outlook

A very low power consumption front end circuit, pseudo-thyristor discriminator is presented in this document. Simulation results show that a power consumption < 10 μW/channel is achievable for ASIC chips fabricated with TSMC 65 nm process.

The positive feedback employed in the circuit helps reach a fast switching speed with a very simple topology. The CMOS structure ensures current paths are cut off at both ON and OFF state resulting in zero static current, while during the switch process, relative high currents flowing through the transistors bring them into higher conductivity regions to fulfill the speed requirements.

It is worth to mention that positive feedback processes are present in amplifications inside natural materials for charged particle detections, such as in gaseous detectors. The frontend circuit utilizing well-controlled positive feedback can be viewed as an extension beyond the interaction of the charged particle with detecting materials.

Acknowledgments

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