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Development of a TAC-based TDC in 130 nm CMOS technology

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Abstract: The design and measurement results of a prototype Time-to-Digital Converter (TDC) fabricated in 130 nm CMOS technology are presented. The TDC architecture with analog interpolators was chosen, which was motivated by previous experience in Analog-to-Digital Converter (ADC) design [1]. The measured time difference between the event and the trigger signal is converted to the amplitude and then digitised by a 10-bit ADC. The TDC prototype is functional and achieved good Differential Non-Linearity (DNL) and jitter (below 1 LSB), slightly dependent of the selected time precision. The obtained Integral Non-Linearity (INL) is significantly higher than simulated and should be still improved. The prototype Application-Specific Integrated Circuit (ASIC) has configurable time resolution from 15 ps to 140 ps, which gives the total possible time measure range from ±9.5 ns to ±70 ns. In this paper the architecture of the developed TDC is described, comprising the implementation of the Time-to-Analog Converter (TAC) and 10-bit ADC. The measurements of the prototype 8 channel TDC ASIC, showing its linearity and timing resolution are also shown.

Keywords: Analogue electronic circuits; Digital electronic circuits; Front-end electronics for detector readout; VLSI circuits

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1 Introduction

Today, in the field of detectors for High Energy Physics (HEP) experiments, in addition to information about the particle's passage and its energy deposited in the sensor, precise time information is often required [2]. Modern complex multi-channel readout Application-Specific Integrated Circuits (ASICs) usually provide both desired quantities. Typically, energy is measured as the signal amplitude by an Analog-to-Digital Converter (ADC), while time information is delivered by a Time-to-Digital Converter (TDC).

Many different architectures of TDC were proposed [3], but for the aforementioned requirements the TDC based on Time-to-Analog Converter (TAC) with ADC for digitisation seems to be a natural choice, since the ADC design can be shared between time and amplitude paths.

This work presents the development of the TDC based on the already existing fast 10-bit ADC [1], which is one of the most requested and used blocks in the readout of various detector systems [4–6]. These and other readout ASICs for LHC and other experiments have been developed in the 130 nm CMOS process, which has been studied in the past and selected for use in HEP experiments many years ago due to its very good performance and good radiation tolerance [7].

The aim of this work is to develop a TDC in CMOS 130 nm, ready for integration into a multi-channel readout ASICs for future experiments. The main goals for TDC are: digitally configured time resolution, ADC based architecture with 10-bit resolution, low power consumption, small pitch per channel below 100 µm, and easy implementation in a multi-channel readout ASIC.

2 TDC design

A simplified block diagram of the TDC is shown in figure 1, consisting of two main parts: the TAC and a fully differential 10-bit Successive Approximation Register (SAR) ADC. The TAC consists of Phase and Frequency Detector (PFD), Charge Pump (CP), VCM Reset block, and logic that control the conversion and communicates with ADC. The PFD detects the time difference between InU and InD (start and stop signals), enabling or disabling two current mirror branches in CP. It also starts (via Control logic) the ADC conversion which is then automatically finished by the ADC itself and signalled back to the Control logic. The VCM Reset circuit maintains the proper voltage on the ADC inputs during the reset state, preparing TDC for the next measurement cycle. The symmetric architecture of the PFD and the fully differential design of CP enable the measurement of positive and negative time values. The time resolution can be digitally configured from 15 ps to 140 ps thanks to internal configurable current DACs.

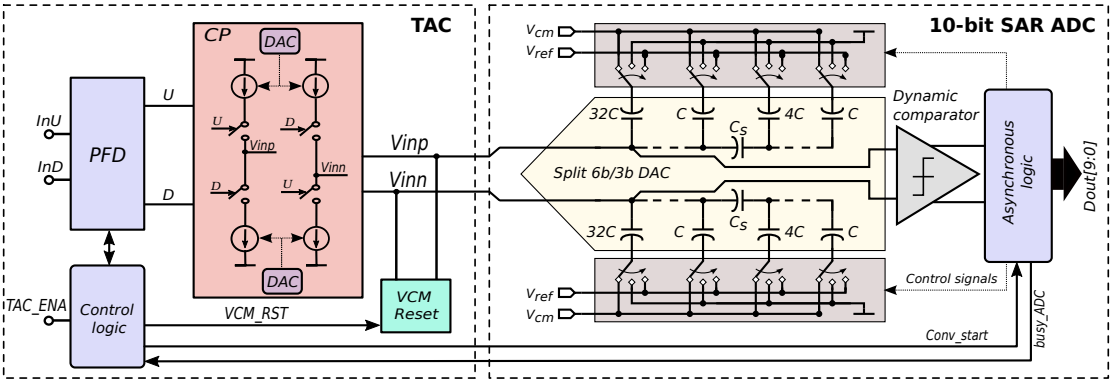

Figure 1. Simplified block diagram of the TDC.

The second part of the TDC is an ADC with a fully differential architecture, comprising a differential capacitive Digital-to-Analog Converter (DAC), a dynamic comparator, and asynchronous control logic [8]. The control logic is implemented as dynamic to increase the speed of the ADC and to reduce power consumption. Due to technological limitations in the minimum capacitance available in the Process Design Kit (PDK), a split DAC architecture with a split capacitor C_s is used to reduce the DAC input capacitance. As a result, the effective unit capacitance is much lower than the minimum physical capacitance used in the DAC design.

Asynchronous and fully dynamic logic, implemented in PFD and ADC, is used to eliminate static power consumption and significantly improve the power budget. It is especially important for the ADC to avoid fast bit-cycling clock distribution during conversion.

Figure 2 shows the timing diagram of the TDC operation. The circuit is fully symmetric and can measure the time difference ΔT between the rising edges of the InU and InD signals, regardless of which one is first received. The measured time value will be negative when InD rises first. The TDC is enabled when the external input TAC_ENA is in high state.

Due to the symmetrical nature of the circuit, there is no need for dedicated start and stop signals, which define the beginning and end of measured time. In case of a situation where one of the InU or InD signals is missing, the TDC will constantly generate erroneous values trying to measure time difference beyond the available range. Disabling the circuit by the TAC_ENA and enabling it again recover the TDC to the proper operating condition.

The U and D signals are generated by the PFD based on the incoming rising edge of InU (or InD) inputs, as shown in figure 2. The extra delay Ton was added here to remove the "dead zone" effect for very short ΔT values. The internal signals U and D turn on/off the current sources in CP, which charge or discharge the internal ADC capacitance (DAC capacitance). As a result, immediately after U (or D) goes high, ADC starts being charged (or discharged) until the rising edge appears at the input InD (or InU). In the end, the voltage on the ADC internal DAC (Vinp and Vinn — differential architecture) will be proportional to the time difference ΔT and ready for conversion. After the ADC conversion, the circuit goes to the reset state and after a short time is ready for the next time measurements.

The layout of TDC, shown in figure 3, was drawn in 100 um pitch, the length is around 740 um. It was done for future implementation of TDC in a multi-channel readout ASIC.

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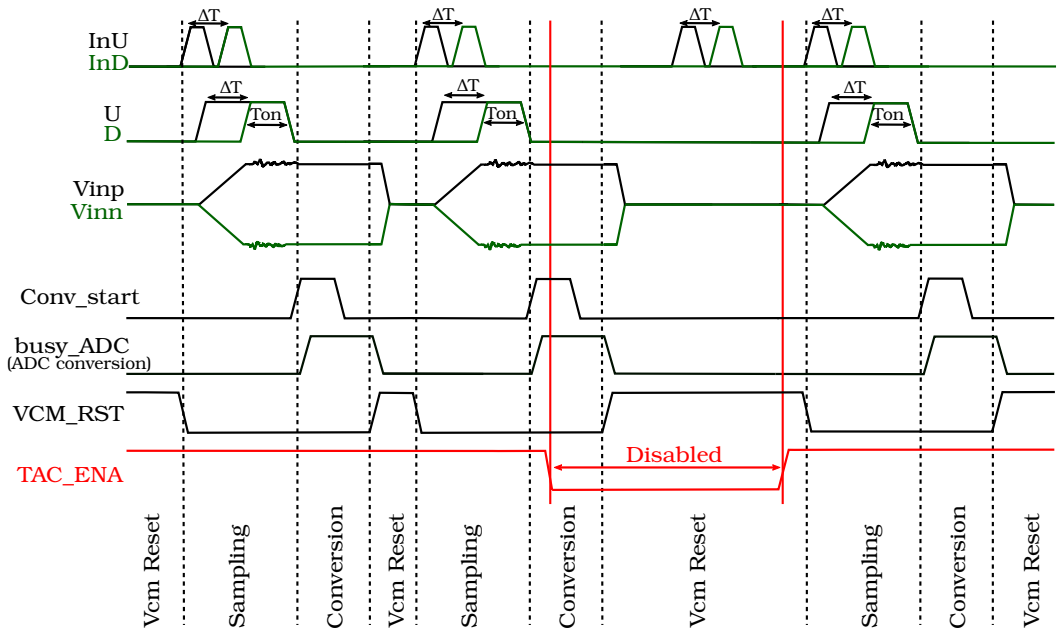

Figure 2. The timing diagram of the TDC operation.

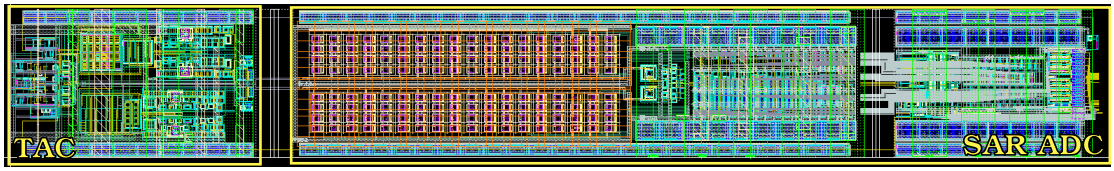

Figure 3. The layout of the TDC — one channel.

3 TDC measurements

The prototype TDC was fabricated in CMOS 130 nm technology. Due to the complexity of the ASIC and its internal configuration, a dedicated setup (shown in figure 4) was developed to measure the important parameters. The measurement setup consists of: a dedicated Printed Circuit Board (PCB) for the TDC ASIC, a digitally controlled uASIC module (custom) for bias voltages and bias current generation, a Field Programmable Gate Array (FPGA) based DAQ supported by a dedicated Gutsy Ferret interconnect board (custom), a signal generator, and a PC for data acquisition and analysis.

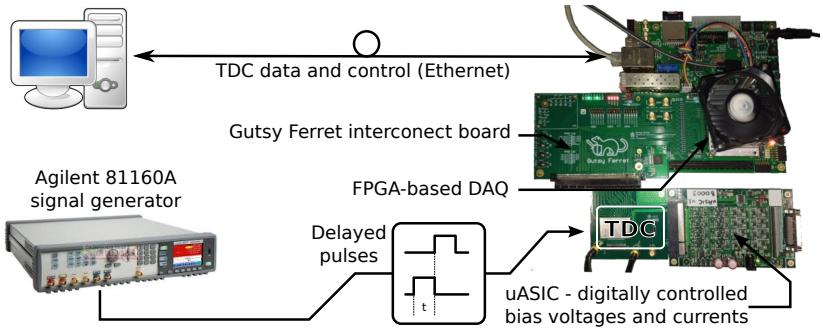

Figure 4. Block diagram of the TDC measurement setup.

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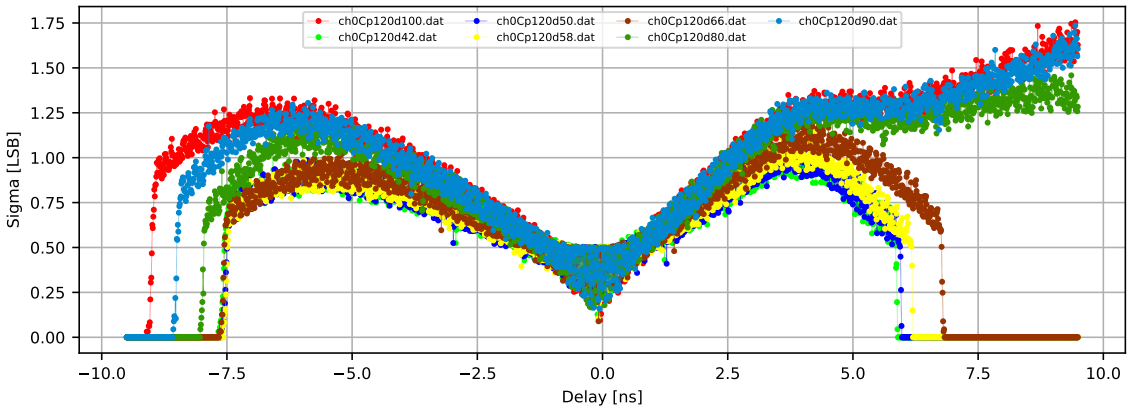

Figure 5. The jitter at the highest resolution (15 ps) as a function of the measured delay.

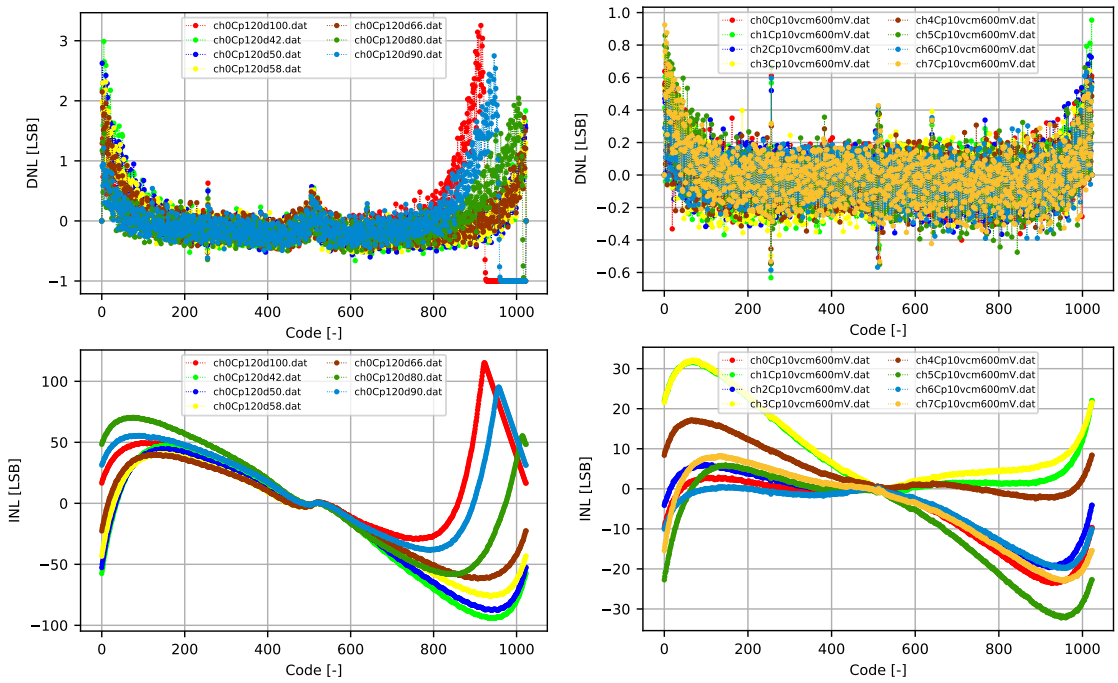

Figure 6. Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) at channel 0 for different CP configurations (left) and for different channels for default configuration (right).

Figure 5 shows the jitter (sigma) at the highest resolution (15 ps) as a function of the measured delay. It is around 1 LSB and depends on the measured time and the internal TDC configuration. The different colors show the different optimization settings for the current sources in CP.

The DNL and INL metrics are shown in figure 6. The two plots on the left are done for ASIC channel 0, working at the highest resolution and for different configurations of CP currents. The results show that TDC achieves a good DNL of about 1 LSB, while INL is significantly worse than simulated of the order of 50 LSB. The measurement results shown in figure 6 (right) are obtained for the lower resolution at the typical TDC configuration, but for all 8 channels available in the prototype ASIC. DNL shows much better performance, about 0.5 LSB, over the most of the operating range

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for all channels. INL is better, but still significantly worse (15 LSB for the best channel) than the simulated and shows different behaviour depending on the channel.

Power consumption was not measured precisely due to technical limitations in the measurement setup, but the post-layout simulations showed the power consumption around 1.2 mW at 20 MHz. The TDC maximum operating frequency is at least 20 MHz at the highest resolution (15 ps LSB).

4 Conclusion

The architecture and measurements results of the prototype TDC, comprising a TAC and 10-bit ADC, are shown. The performed tests confirm the expected TDC functionality. The circuit has a configurable time resolution from 15 ps to 140 ps giving the total possible time measure range from ±9.5 ns to ±70 ns. The symmetrical architecture of the current sources and the fully differential ADC enable positive and negative (before trigger) time measurements. The jitter is slightly dependent on the measured time, but in most of the range is below 1 LSB.

The results show that TDC achieves a good DNL of about 1 LSB at the highest resolution and significantly better at lower resolution. The same behaviour is observed for all channels in the ASIC prototype. INL is significantly worse than simulated and also shows different values for different channels. Detailed circuit tests and analysis show that most of these non-linearities come from current sources in the CP design. In particular, detailed simulations show the effect of the current drop with decreasing voltage on the current source, and in addition large current fluctuations are visible in Monte Carlo and corner simulations. Most likely, in addition to optimizing the current sources (including matching improvement), the range of configurable currents (and therefore the range of configurable time resolution) will have to be reduced, to make TDC ready for implementation in a multi-channel ASICs readout system.

Acknowledgments

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