A sub-5 ps jitter Time-to-Digital Converter ASIC with Back-Gate Delay Tuning in 22 nm CMOS

FERMILAB-PUB-25-0014-ETD

DOI: 10.1016/j.nima.2025.170784

Accepted Manuscript

A sub-5 ps jitter Time-to-Digital Converter ASIC with Back-Gate Delay Tuning in 22 nm CMOS

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Abstract

We present the design of a Time-to-Digital Converter (TDC) ASIC together with performance characterization results at cryogenic temperature (6-8 K), and at room temperature using emulated Low-Gain Avalanche Detector (LGAD) signals. The TDC design uses a two-step architecture with a ring-oscillator based counter and a Vernier delay line fine TDC. The TDC is implemented in an FD-SOI process, and back-gate tuning is used not only to correct threshold variation due to cryogenic operation, but also as a novel way to tune TDC delay elements with very little overhead. Using this technique, we demonstrate a design with very low power (0.5 mW) and area ($0.003\,\mathrm{mm}^2$). We present test results using the Fermilab Constant Fraction Discriminator (FCFD) ASIC to produce discriminated signals from an internal charge injection mechanism that mimics the waveform and signal amplitude of minimum ionizing particles impinging on LGAD sensors. We characterize the time precision of the full system and verify that the TDC ASIC contributes a negligible amount to the total system time precision, fully consistent with the expected jitter contribution of less than 5 ps. The results presented here demonstrate the utility of our TDC for applications in physics and quantum communications.

Keywords: Solid state detectors, Timing detectors, Particle tracking detectors (Solid-state detectors), Time-to-digital Converter, TDC, cryo-CMOS, SNSPD, LGAD

1. Introduction

Precise timing information plays a critical role in many detector systems used for fundamental science ranging from applications as diverse as single photon detectors for quantum communications [1] to tracking detectors for future particle colliders [2]. For the former, exploiting and preserving the exquisite temporal resolution of fast timing detectors such as superconducting nanowire single photon detectors (SNSPDs), which have demonstrated sub-3 ps precision [3], requires close integration with high-performance front-end readout and time-tagging circuits capable of operating at cryogenic temperature (4-20 K) at low power [4].

In the field of high energy particle physics, tracking detectors capable of achieving 5–25 ps timing resolution with pixel sizes as small as 25×25 μm^2 are necessary for many proposed future particle colliders including the Muon Collider [5], the FCC-hh [6, 7], and the Electron–Ion Collider (EIC) [8]. Extracting precision timing information from low gain avalanche detectors (LGADs) in particular is currently a key focus for particle physics instrumentation [9, 10], as LGADs have been demonstrated to achieve 20–30 ps time resolution, making them a leading candidate detector technology for precision timing tracking detector systems [11, 12, 13, 14, 15]. TDC power is expected to become among the dominant contributions to the total power budget of these systems, as the TDC (unlike the front-end amplifier) will not benefit from the reduction in input capacitance associated with smaller pixels.

As such, the design and implementation of low-power front-end electronics capable of extracting precision timing information from LGAD sensors represents a key technical milestone. Initial work has targeted TDC architectures for the endcap timing layer of the CMS experiment at the Large Hadron Collider [16] and general high-energy physics applications [17], but work remains to simultaneously meet the challenging power, area, and performance requirements of future detectors. Our two-step time-to-digital-converter is designed to minimize power and area consumption while providing picosecond resolution. Our design leverages back-gate biasing in the GlobalFoundries 22FDX silicon-on-insulator node as a novel tuning mechanism for delay stages, as well as a compensation strategy to enable operation from 4 Kelvin to room temperature.

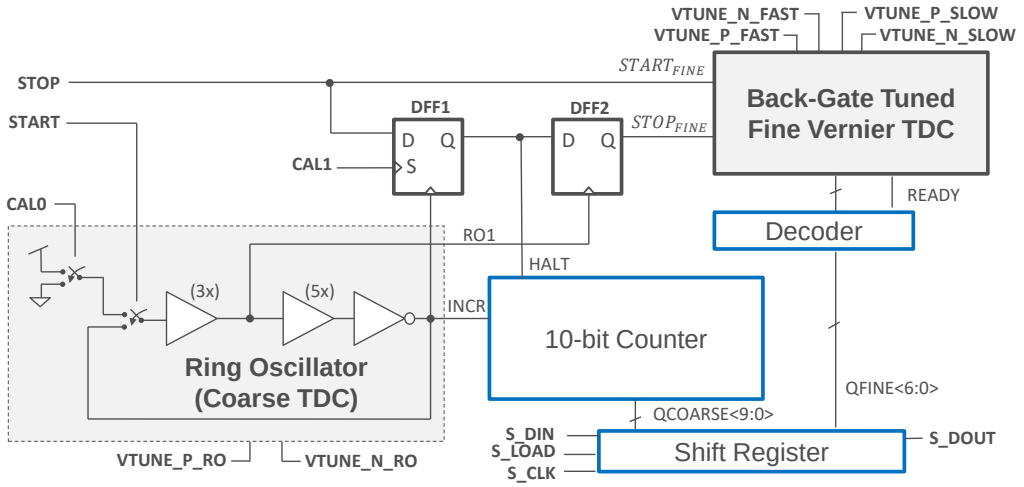

Figure 1: A block diagram of the TDC ASIC design, showing the coarse ring oscillator, DFF interlock, fine Vernier TDC, and serial readout. Bolded signals are inputs or outputs of the test ASIC.

In this paper, we present the design and performance characterization of our Time-to-Digital Converter (TDC) ASIC. We first describe the overall structure of the TDC in Section II, then focus on the implementation of the novel back-gate delay tuning technique in Section III. In Section IV, we present test results. Following the conventions in [18], we report the TDC's timing resolution (i.e. bin size) as a function of the back-gate tuning voltage and precision or jitter (i.e. root-mean-square (rms) error) as a function of the measured time interval T_{in}. Finally, the jitter performance of the TDC is measured using the discriminator output signals from the Fermilab Constant Fraction Discriminator (FCFD) ASIC, presented in [19], which converts signal pulses into discriminated waveforms robust against amplitude-induced time-walk, mimicking the output signal of an LGAD detector.

2. TDC Design and Readout

Compact, low-power TDCs are highly desirable for quantum communication applications in order to be closely integrated with cryogenic control and readout electronics, as well as for particle tracking applications where a large number of channels must be integrated to disambiguate particle tracks. However, timing performance, which encompasses both a fine time resolution

(small bin size) and high precision (low jitter), cannot be sacrificed in either application, and sufficient dynamic range is necessary to allow synchronization with a distributed system reference clock.

The TDC we present is designed with a two-step architecture consisting of a ring-oscillator coarse TDC and a linear Vernier delay line fine TDC. Both stages make use of the back-gate biasing capabilities of the GlobalFoundries 22FDX node to provide fine-tuning. A single-channel prototype TDC is implemented with simple, low-speed readout capabilities, laying the groundwork for a second ASIC integrating many channels with readout and synchronization logic.

2.1. Time-to-Digital Converter Design

A generalized Time-to-Digital Converter produces a digital code which represents the time interval T_{in} between the rising edges of two signals, generally termed *start* and *stop*. A two-step TDC like the design we present consists of two components: a "coarse" TDC which produces an output digital code Q_{coarse} such that $T_{in} \approx T_{lsb(coarse)} Q_{coarse}$, and a "fine" TDC which measures the error between the coarse prediction and the actual time interval, producing an output Q_{fine} such that $T_{in} = T_{lsb(coarse)} Q_{coarse} + T_{lsb(fine)} Q_{fine}$.

Two-step TDCs can typically outperform single-step TDCs in terms of the combination of dynamic range and resolution, since the circuits which allow a fine TDC to achieve fine resolution typically scale poorly for large values of T_{in}. However, a critical concern for two-step TDCs is the method of coupling signals between the two stages, which must not introduce undue jitter or nonlinearity.

The two-step architecture of our TDC (see Fig. 1) follows closely from the design reported by Enomoto et al. [20], which uses a two-DFF interlock to couple signals between a coarse ring oscillator and a fine Vernier TDC. The basic operation of the TDC is as follows:

1. When the *start* signal arrives, the ring oscillator begins to oscillate, and the coarse TDC begins to count.
2. When the *stop* signal arrives, it immediately asserts the start input to the fine TDC ($start_{fine}$).
3. On the next assertion of the clock input to DFF1, *HALT* is asserted, and the coarse TDC count is frozen.
4. On the next assertion of the clock input to DFF2, the stop input to the fine TDC is asserted ($stop_{fine}$).

The use of two sequential flip-flops ensures that there is always a fixed delay T_{gd} between the halting of the coarse TDC and the assertion of $stop_{fine}$. So long as the dynamic range of the fine TDC is greater than $T_{lsb(coarse)}$, this ensures a highly linear TDC transfer function: the ring oscillator contributes no nonlinearity as the load capacitance for every cycle is identical, and the fine TDC, like all thermometer-coded TDCs, exhibits differential non-linearity (DNL) less than 1 LSB. DFF2 also suppresses any metastability that results from the clock and data inputs of DFF1 changing simultaneously before that metastability can propagate to the fine TDC.

The relationship between T_{in} and the TDC digital codes may be derived as follows, starting from the definition:

$$T_{in} = T(stop) - T(start) \tag{1}$$

Letting $T(start) = 0$ and noting that the *stop* signal directly triggers $start_{fine}$ we have:

$$T_{in} = T(start_{fine}) \tag{2}$$

The characteristic equation of the fine TDC is: $T_{lsb(fine)}Q_{fine} = T(stop_{fine}) - T(start_{fine})$. Substituting (2) yields:

$$T_{in} = -T_{lsb(fine)}Q_{fine} + T(stop_{fine}) \tag{3}$$

Finally, due to the fixed propagation delay from DFF1 through DFF2, we note that: $T(stop_{fine}) = T_{lsb(coarse)}Q_{coarse} + T_{gd}$, so we have:

$$T_{in} = -T_{lsb(fine)}Q_{fine} + T_{lsb(coarse)}Q_{coarse} + T_{gd} \tag{4}$$

The three calibration parameters $T_{lsb(fine)}$, $T_{lsb(coarse)}$, and T_{gd} may be calculated by applying pulses of known length to the input of the TDC. After establishing these values, T_{in} may be calculated from Q_{coarse} and Q_{fine}.

It should be noted that some fixed offset T_{off} is practically present in any TDC due to wire delays and fixed mismatches, which must be calibrated for. In our TDC, this is absorbed into T_{gd}. Thus the use of the fixed flip-flop interlock does not introduce a new calibration parameter.

The coarse and fine TDC are both constructed of inverter-based delay cells. The coarse TDC is a ring oscillator composed of a loop of delay cells whose total delay determines $T_{lsb(coarse)}$. The fine TDC is a Vernier TDC (Fig. 2), a structure which uses two delay lines with slightly different delays to achieve sub-gate-delay timing resolution. The delay per stage of the delay

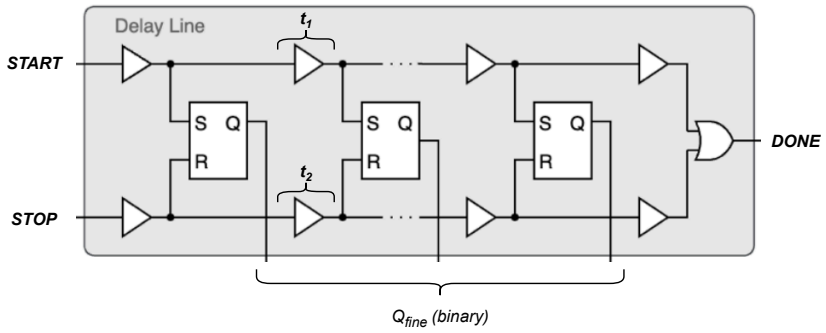

Figure 2: A diagram of a Vernier Delay Line based fine TDC. The TDC is tuned such that $t_1 - t_2 = T_{lsb(fine)} > 0$

lines attached to *start* and *stop* are t_1 and t_2 respectively, with $t_1 > t_2$ such that the rising edge of *stop* eventually catches up to the rising edge of *start*. At each stage, the delay between *start* and *stop* should shrink by $t_1 - t_2 = T_{lsb(fine)}$.A latch (in the case of our TDC, a simple SR latch) compares which signal arrived first. The number of stages after which the *start* signal no longer arrives before the *stop* signal yields Q_{fine}.

2.2. Test ASIC

We implemented, manufactured, and tested a single-channel prototype of this TDC in GlobalFoundries 22FDX (Fig. 3). The TDC core described above was integrated with simple interfaces and a serial readout to enable testing and debugging, which are described in this section. In some cases, these interfaces limit the performance of the TDC.

A second version of this TDC has also been designed, which is currently under test. This future TDC version incorporates thirty-two channels which are synchronized to a shared reference clock using an on-ASIC PLL. Additionally, this version uses a sophisticated asynchronous readout architecture which is designed to allow all channels to be read out at full rate using 1 Gbps links.

In the test ASIC, all digital I/O signals including *start* and *stop* are 1.8 V non-return-to-zero (NRZ) CMOS signals, driven by dedicated I/O cells. In an optimized system, the high-speed interfaces would be co-designed with the intended sensor. In the test ASIC, all six TDC core tuning voltages are exposed as I/Os for manual tuning, along with two additional tuning

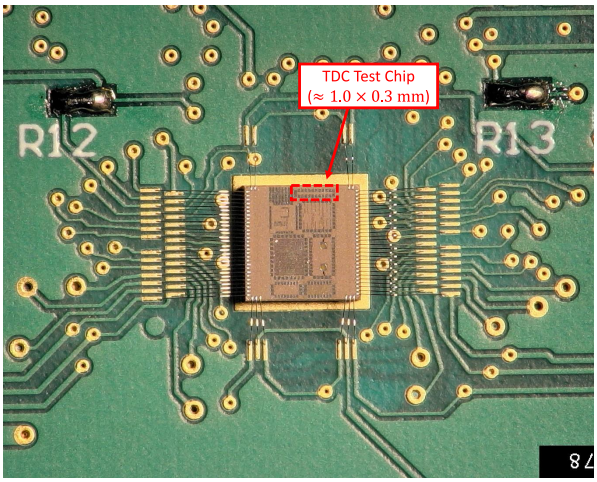

Figure 3: A die photograph of the TDC.

voltages which control the back-gate bias voltage applied to digital circuits, primarily for the purpose of compensating for cryogenic threshold voltage shift. Finally, the use of a local ring oscillator to drive the coarse TDC is not intended to be scalable due to the limits of accumulated jitter and variability between channels; a single-ended ring oscillator like the one in this design will also suffer from inherently very limited supply rejection [21], which we did not measure. Future versions of this TDC will retain the architecture and core circuitry of this design, but the coarse clock will be provided by a separate on-ASIC PLL.

In this prototype ASIC, programming configuration bits and reading out Q_{coarse} and Q_{fine} are both accomplished using a simple shift register. Each TDC count must be read from the shift register by an external controller before another count can be taken, which is the primary limit on readout speed in our tests reported below. The TDC architecture is designed to operate at 100 Mcounts/s; it is limited by the time taken for the Vernier delay line to converge on a value of Q_{coarse}.

The prototype TDC is implemented as a stand-alone sub-block in a larger 3.0 mm × 3.0 mm ASIC (Fig. 3). The block dimensions of 0.3 mm × 1.0 mm are dominated by the pad ring, while the TDC channel itself is 20 µm × 150 µm.

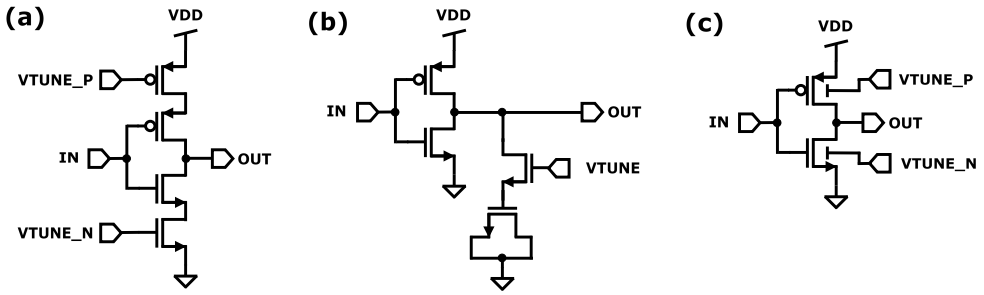

Figure 4: Three methods for tuning the delay of a single Vernier TDC delay cell: (a) current-starving, (b) load capacitance tuning, (c) back-gate delay tuning, the novel method reported in this paper.

3. Back-Gate Delay Tuning Technique

In any Vernier delay line TDC, a method of fine-tuning the delay of TDC delay cells on a sub-gate-delay level is necessary, and the delay tuning technique has a direct impact on the TDC's resolution via the relationship $t_1 - t_2 = T_{lsb(fine)}$, where t_2 and t_1 are the (tuned) delays of individual cells in the fast and slow delay chains respectively.

For a rising (falling) edge, the propagation delay of a CMOS inverter stage is set by the time it takes for current through the drain of the PMOS (NMOS) I_D to charge (discharge) the capacitance of the output node C_Z sufficiently that the voltage at Z crosses the threshold voltage of the next stage [22]. This leads to the two conventional strategies for tuning the delay of a CMOS inverter: current-starving, which limits I_D, and load capacitance tuning, which increases C_Z [23]. Conventionally, current-starving is implemented by placing additional transistors in series with the PMOS and NMOS gates of the inverter to limit current draw from the supply. In our TDC, however, we leverage the back-gate bias capabilites of the GlobalFoundries 22FDX fully-depleted silicon-on-insulator (FDSOI) process to directly control the conductivity of the delay cell NMOS and PMOS, setting I_D and thus the delay of each cell. While the use of FDSOI technology to trade digital performance versus power, and to mitigate the effects of cryogenic operation, are widely reported [24], this is to our knowledge the first reported use of this technology to calibrate the resolution of a Vernier TDC.

Schematic implementations of the three approaches, including our own, are shown in Fig 4. The most striking advantage of our approach is the compactness of the layout. Both conventional approaches require adding several

additional transistors to the unit delay cell, while ours does not. Because these additional transistors are responsible for providing currents or capacitance that is robust against process variation, they may dwarf the size of the delay element (the inverter) itself. The jitter of a CMOS ring oscillator is dominated by white noise and flicker noise from two-level fluctuations in transistor channels [25], so these additional transistors also contribute potential noise. Finally, the additional capacitance increases the power consumption of the fine TDC.

The substrate taps required to bias the NMOS and PMOS transistors in our process do require some layout area, but these taps need not be extremely close to the delay elements, and can be shared between multiple delay elements. In total, we expose six tuning voltage, which are all externally controllable in our test chip: separate NMOS and PMOS back-gate bias voltages for the ring oscillator, and for the slow and fast delay lines of the fine TDC. For convenience in testing, we chose to make the bias voltages for both NMOS and PMOS greater than zero, which required using different threshold voltage flavors for PMOS (regular Vt) and NMOS (super-low Vt) in the GF22FDX process. Without this constraint, slightly higher performance and a more compact layout could be achieved.

Crucially, the same back-gate bias voltages can also be used to negate the characteristic threshold voltage increase observed at cryogenic temperatures [26], maintaining the same TDC resolution across temperature.

4. Experimental Results

We characterize the TDC ASIC by measuring the TDC resolution as a function of the back-gate tuning voltage, the TDC jitter as a function of the delay between the start and stop signals (T_{in}), and the TDC power as a function of the count rate.

4.1. Test Chip Readout

In our experiment, a microcontroller (Arduino Portenta) is used for digital control and readout of the ASIC, as shown in Figure 5. The microcontroller interfaces with the ASIC through a simple serial interface (S_CLK, S_DIN, S_DOUT). In order to prevent shift register action from affecting the internal state of the TDC, two additional signals gate the transfer of data between the shift register and the TDC's internal shadow registers: S_PASS is asserted to pass control bits from the shift register into the shadow registers, and

S_LOAD is asserted to retrieve data (i.e. Q_{coarse} and Q_{fine}) from the shadow registers and place that data in the scan chain.

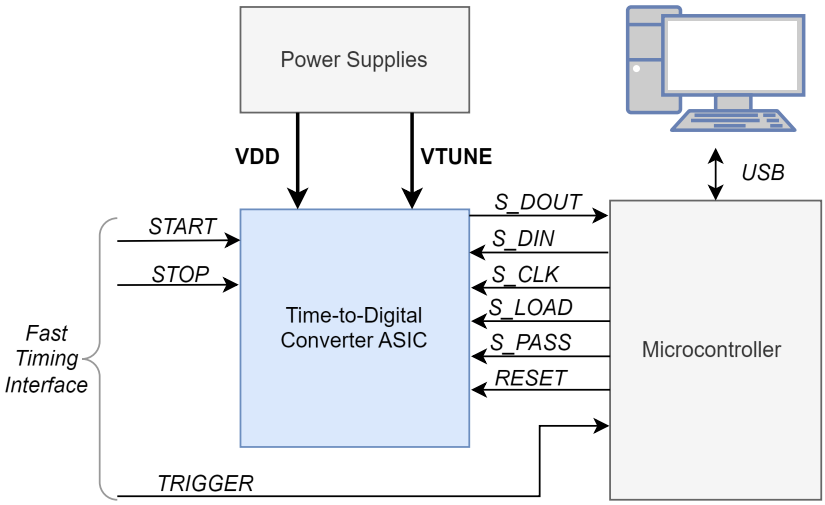

Figure 5: A block diagram illustrating the interfaces between our TDC ASIC and our test setup, including power, digital readout / control, and fast timing interfaces.

A trigger signal is supplied directly from the timing source to the microcontroller, which tells the microcontroller when to retrieve a new measurement from the ASIC. The precise timing of the trigger signal is unimportant: Q_{coarse} and Q_{fine} are determined exclusively by $T_{in} = T(stop) - T(start)$. However, one trigger pulse must be sent for each START/STOP pair to ensure the microcontroller retrieves the current count before it is overwritten by the next count.

4.2. ASIC Characterization Using Pulse Generator

For independent characterization of our TDC we used a Berkley Nucleonics Model 745-OEM Digital Delay Generator to supply the START/STOP and trigger signals. The 745-OEM instrument has a delay resolution of 1 ps and specified RMS jitter of better than $T_{j,rms}$ = 5 ps + delay x 10^{-8}, or approximately 5 ps for signals in the range of interest. The jitter of our specific instrument was measured to be 3.5 ps using a 20 GHz oscilloscope at 2 ns delay.

To calibrate the TDC for each test condition, we performed measurements of three fixed input time differentials (0ps, 100ps, and 10ns) supplied by the

745-OEM and averaged the TDC response for each over a large number of cycles to mitigate jitter. This yielded a system of three equations which can be solved for the calibration constants $T_{lsb(fine)}$, $T_{lsb(coarse)}$, and T_{gd} (see Sec 2).

4.2.1. TDC Resolution vs Tuning Voltage

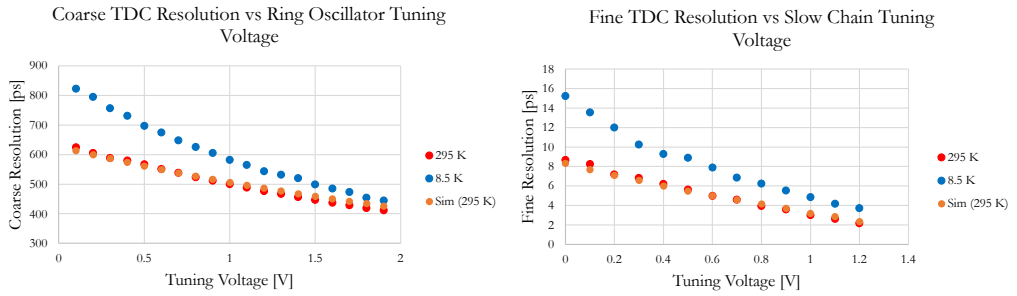

Figure 6: Resolution of the coarse and fine TDCs as a function of back-gate tuning voltage.

In order to assess the tunability of the ASIC, we define two tuning parameters $V_{tune(coarse)}$ and $V_{tune(fine)}$. The actual tuning voltages for the ASIC are derived from these parameters as shown in Table 1. The expressions are defined such that an increase in $V_{tune(coarse)}$ decreases the coarse TDC resolution, and an increase in $V_{tune(fine)}$ decreases the fine TDC resolution, while keeping NMOS and PMOS drive strengths roughly balanced. Nominal values are $V_{tune(coarse)} = 1V$ and $V_{tune(fine)} = 0.55V$.

ASIC Tuning Voltage	**Expression from Tuning Parameters**
VTUNE_N_RO	$V_{tune(coarse)}$
VTUNE_P_RO	$2 - V_{tune(coarse)}$
VTUNE_N_FAST	1.9 V (fixed)
VTUNE_P_FAST	0.1 V (fixed)
VTUNE_N_SLOW	$V_{tune(fine)}$
VTUNE_P_SLOW	$2 - V_{tune(fine)}$

Table 1: Expressions for ASIC tuning voltages as a function of tuning parameters.

To generate each of the two plots in Figure 6 we swept one tuning parameter while keeping the other constant. For each tuning voltage value, we

took three measurements of known-length pulses and recorded the output code from the TDC, then solved this system of three equations as described in 2.1 to find the coarse and fine TDC resolution $t_{R(coarse)}$ and $t_{R(fine)}$, which are plotted for two measurement temperatures (295 and 8.5 Kelvin). We also present simulation results using foundry PDK models and extracted parasitics, which closely agree with the measured results at room temperature. Calibrated cryogenic transistor models were not available at the time of publication.

When the tuning voltage is held constant, we observe that a larger resolution is measured at cryogenic (8.5 K) temperature versus room temperature. This effect primarily results from the well-known threshold shift of CMOS devices at cryogenic temperature [27], which increases the propagation delay of both ring oscillator stages and Vernier delay line stages [28]. This effect can be mitigated in some cases by choosing a different tuning voltage to compensate for threshold voltage shift. Due to larger overall delays, the tuning slope is also approximately twice as large at cryogenic temperatures: we measured 216 ps/V (coarse) and 9.59 ps/V (fine) at 8.5K, versus 118 ps/V (coarse) and 5.40 ps/V (fine) at room temperature. Differential nonlinearity is not characterized, but expected to be ¡ $T_{lsb(fine)}$ due to the TDC architecture as described previously.

4.2.2. TDC Jitter

We assessed the jitter of our TDC in isolation by fixing the START/STOP delay (T_{in}) and taking a large number of samples to build a code distribution. Results as a function of T_{in} are shown in Fig 7. For small values of T_{in}, the core TDC circuits demonstrate jitter below the measurement floor of the 745-OEM instrument, resulting in an approximately flat measured jitter value in the range of a few picoseconds. For larger values of T_{in}, accumulated flicker noise around the test chip ring oscillator is the dominant noise source, resulting in a roughly linear correlation between jitter and T_{in} ($\sigma(T_{in}) \approx 0.001 T_{in}$). Future ASICs which incorporate an on-chip PLL will not exhibit this artifact, which should extend the range over which our TDC exhibits picosecond jitter. Even if limited to the regime in which it achieves few-picosecond jitter, our TDC can still provide adequate coverage for many important particle physics applications, such as timing readout for detectors at the LHC. For example, several readout chips designed for LHC precision timing detectors incorporate TDCs with dynamic range at or below 10 ns, such as ETROC [29] for the CMS MIP Timing Detector and ALTIROC [30]

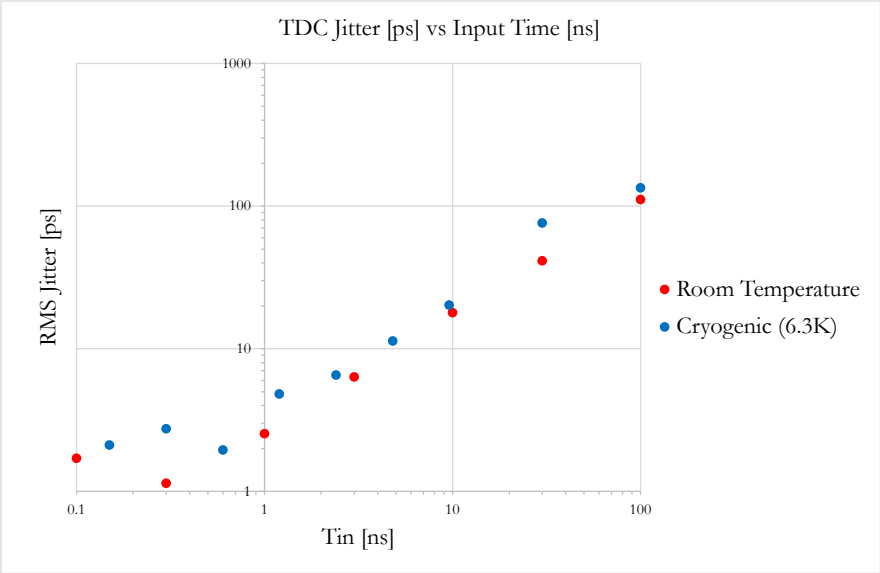

Figure 7: TDC jitter results as a factor of $T_{in} = T(stop) - T(start)$. See note below on temperature.

for the ATLAS High-Granularity Timing Detector. Other applications such as time-domain multiplexing of megapixel arrays [31] for time-resolved imaging in astronomy are also competitive at jitter below 20 ps.

We measured the performance of the TDC at both room temperature and cryogenic temperature (6.3 degrees Kelvin). The measurement temperature differs from the previous experiment (8.5K) because different instrumentation of our closed-cycle cryostat results in a different heat load and thus a different minimum achievable temperature.

Because the contribution of thermal noise is already small (<1 ps rms, from simulation) and flicker noise is not reduced by low temperature [32], no significant advantage is obtained from cryogenic operation. In fact, because the tuning voltage is identical, the cryogenic TDC bin size is slightly larger, resulting in slightly higher jitter.

4.2.3. TDC Power

Our TDC operates in an asynchronous, event-driven fashion, which means that its power consumption is highly dependent on the rate of counts, as well as the average time (t_{RO}) that the ring oscillator must be active in order to resolve each count, which is dependent on the length of START and STOP

pulses. For test purposes, we can control the value of t_{RO} arbitrarily by setting the length of these pulses. Figure 8 illustrates power consumption at cryogenic and room temperature up to 1 Mcps, the limit of our test stand, for t_{RO} values of 100 and 200 nanoseconds. We observe that both quiescent and dynamic power consumption are reduced at cryogenic temperature, due to lower leakage current and slower operation of the TDC at nominal tuning levels.

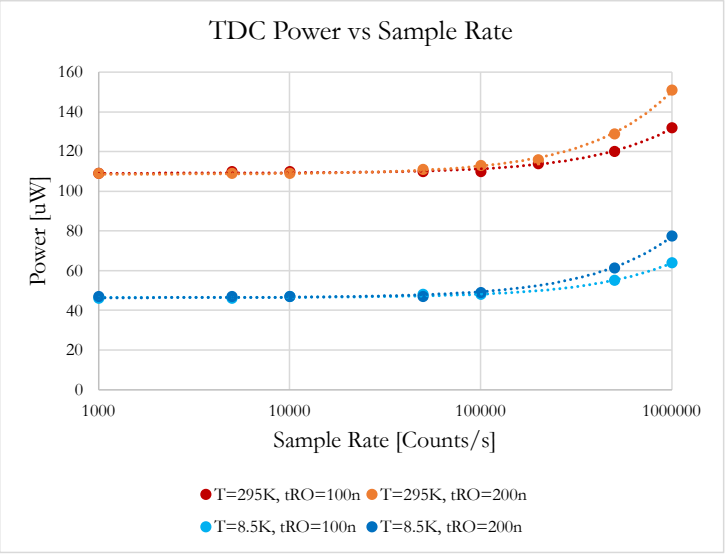

Figure 8: Measured TDC power as a factor of temperature, count rate, and average ring oscillator run time per count (t_{RO}) for count rates up to 1 M counts per second, the limit of our test stand.

Figure of Merit	**295 K**	**8.5 K**
Quiescent Power ($P_{Quiescent}$, µW)	109	46.6
Energy per fine ADC Conversion (E_{fine}, pJ)	3.30	3.03
Ring Oscillator Power (P_{RO}, µW)	193	142
Estimated Channel Power at 100 kcps (µW)	110	47
Estimated Channel Power at 100 Mcps (µW)	632	492

Table 2: TDC channel power for count rates of 100 kcps and 100 Mcps, assuming $t_{RO} = 10ns$

Although our test stand is only capable of driving pulses up to 1 Mcps, the TDC is capable of operating with input count rates of at least 100 Mcps.

Using the data from Figure 8, we can estimate the breakdown of power consumption per block, and use these numbers to estimate power at 100 Mcps as $P(f_{samp}) = P_{RO}t_{RO}f_{samp} + E_{fine}f_{samp} + P_{Quiescent}$. To calculate the power figures of merit in Table 2, we assume $t_{RO} = 10ns$, which means that at an input count rate of 100 Mcps, the ring oscillator is constantly running, which is a conservative estimate.

4.2.4. Summary of Figures of Merit

Reference	Dutton 2015 (ISSCC)	Roy 2017 (TRPMS)	Zhang 2019 (JSSC)	Nolet 2020 (IET)	Talala 2023 (JSSC)	Pass 2023 (ICEE)	This Work	
Technology (nm)	130	65	180	65	110	65	22 FDSOI	
# of Channels	1	4	144 x 6 x 2	1	256	Sim	1	
Cryogenic Results	None	None	None	None	None	None	8.5 K	
Resolution (ps)	71	6.9	48.8	5.5	25.4	20	295K	8.5K
							6.20	8.52
TDC Area (mm^2)	0.03	0.00125	0.025	0.00151	0.024	0.002704	0.003	
TDC Power (mW)	14.1	0.16	2.9	0.02	0.11	0.32	295K	8.5K
							0.63	0.49
Range (ns)	18.8	3	200	4	3.25	168	**	
Conversion Rate (MS/s)	14000	5	666	1	0.28	5	100	
Figure of Merit (Rate/Res.×Pow. ×Area)	466	3620	188	5470	4.2	289	295K	8.5K
							8530	7980

Figure 9: Summary of figures of merit compared to selected recent TDC designs. References in order of appearance: [33] [34] [35] [36] [37][38]

The figures of merit of the TDC design are presented in Figure 9. The figures in the table are calculated by setting the TDC tuning voltages to their nominal settings, and conservatively assuming an input count rate of 100 Mcps and $t_{RO} = 10ns$. In reality, the TDC's power and resolution are highly dependent on count rate and tuning voltages as detailed in the pervious sections. The range of our TDC is practically limited by the accumulation of jitter on the ring oscillator; given a maximum jitter specification for the TDC, the maximum allowable range is the T_{in} value which corresponds to that level of jitter in Figure 7. To avoid making an arbitrary assumption about required jitter, we do not report a single range value in this table.

4.3. ASIC Characterization Using Emulated LGAD Signals

To characterize the performance of our TDC with realistic emulated LGAD signals, we use the FCFD front-end readout ASIC [19]. As shown

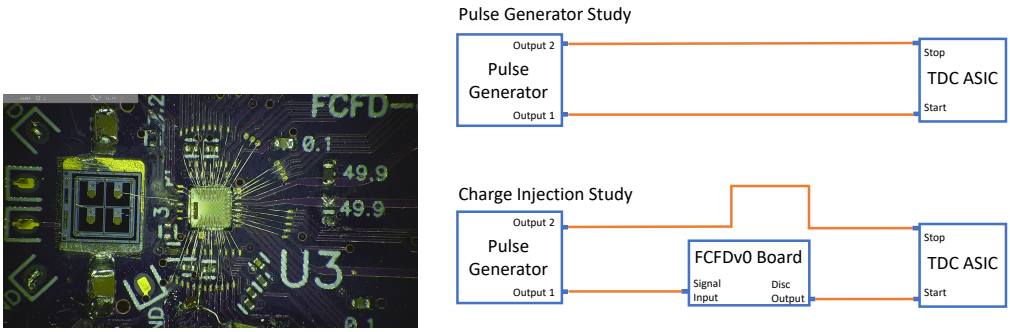

Figure 10: Left: A photograph of the FCFD characterization board showing the FCFD ASIC wire-bonded to an LGAD sensor. Right: schematic diagrams of the pulse generator test measurement (top) and the FCFD charge injection test measurement (bottom).

in Figure 10, we insert the FCFD ASIC into the signal path between the 745-OEM pulse generator and the TDC. The FCFD output is used as the TDC start signal, while the second output of the pulse generator is used as the stop signal. When triggered by the pulse generator, the FCFD generates discriminated LGAD signal pulses using an internal pulse injection circuit, achieving overall jitter better than 9 ps. In order to ensure that the stop signal from the pulse generator arrives later than the start signal from the FCFD output, we introduce a physical delay using longer cables for the pulse generator output. Characteristic waveforms for both setups are shown in Figure 11.

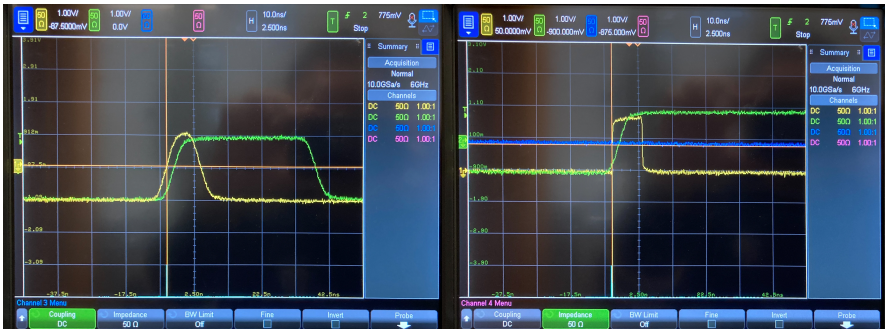

Figure 11: Waveforms of the signals tested acquired by oscilloscope. Left: waveforms for two pulse generator signals to represent the start and stop signals. Right: waveforms for the charge injection trigger (green) and FCFD response (yellow).

The Arduino-based readout system described above is used to capture

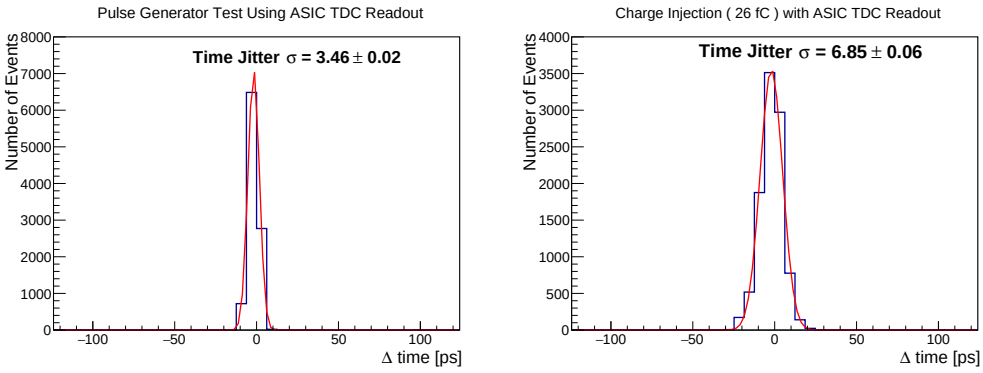

Figure 12: Histograms of the measured time difference between the start and stop signals using our TDC readout for the pulse generator test (left) and one of the charge injection measurements (right).

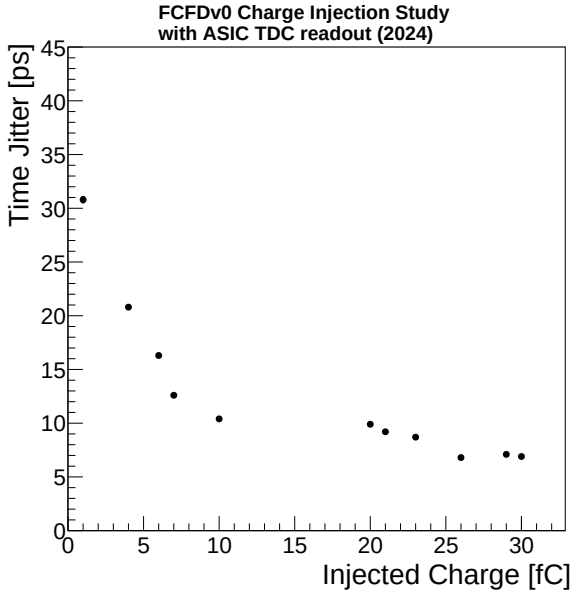

Figure 13: The measured time precision is shown as a function of the injected charge. The internal charge injection mechanism of the FCFD ASIC is used to produce signals and the TDC ASIC is used to read out and digitize the time stamps.

the elapsed time (Δt) between the start and stop signals reported by the TDC. To characterize jitter, we capture a large number of samples of Δt and fit the resulting distribution to a Gaussian function, where σ corresponds to

timing precision, or jitter.

Using the built-in switches, the FCFD ASIC can generate charge injection waveforms from various datasets corresponding to signals with injected charge ranging from 1–30 fC. In Figure 12, we show histograms of the Δt distribution with only the pulse generator (left) compared to the FCFD ASIC with emulated charge injection of 26 fC (right). We measure a TDC precision of 3.5 ps, which is a fraction of the intrinsic jitter of the charge injection mechanism. In Figure 13 we show measured time precision as a function of the injected charge. The results are consistent with previously reported measurements using an oscilloscope readout [19]. These measurements confirm that the contribution of the TDC to the time precision of the full system is below 4 ps, achieving the original design parameters.

5. Conclusions and Outlook

Development of low-power, high-resolution TDCs for applications in high precision timing is one of the key challenges towards implementation of large-scale 4D-tracking detectors. Similarly, applications with novel quantum sensors require very high precision TDCs that are capable of operating in ultra-cold environments.

In this paper we presented a novel TDC design architecture, and the characterization results of the test ASIC in various configurations, at both room and cryogenic temperature. The design makes use of the back-gate biasing capabilities of the GlobalFoundries 22FDX node to provide fine-tuning for the coarse and fine TDC stages. Using the GF 22FDX node allowed us to design a low complexity, small footprint TDC with no noise contribution from bias circuits and separate tuning voltages. Our measurements using both a pulse generator and a dedicated LGAD front-end readout ASIC demonstrate that the compact TDC design achieves better than 4 ps timing resolution, with a power consumption below 630 and 110 μW at 100 and 0.1 Mcounts/second respectively.

Acknowledgments

This document was prepared using the resources of the Fermi National Accelerator Laboratory (Fermilab), a U.S. Department of Energy, Office of Science, Office of High Energy Physics HEP User Facility. Fermilab is managed by Fermi Forward Discovery Group, LLC, acting under Contract

No. 89243024CSC000002. This work was funded by the U.S. DOE Office of Science Research Program for Microelectronics Codesign through the HYDRA project "Hybrid Cryogenic Detector Architectures for Sensing and Edge Computing enabled by new Fabrication Processes" (LAB 21-2491). This work has also been supported by funding from the California Institute of Technology High Energy Physics under Contract DE-SC0011925 with the U.S. Department of Energy.

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