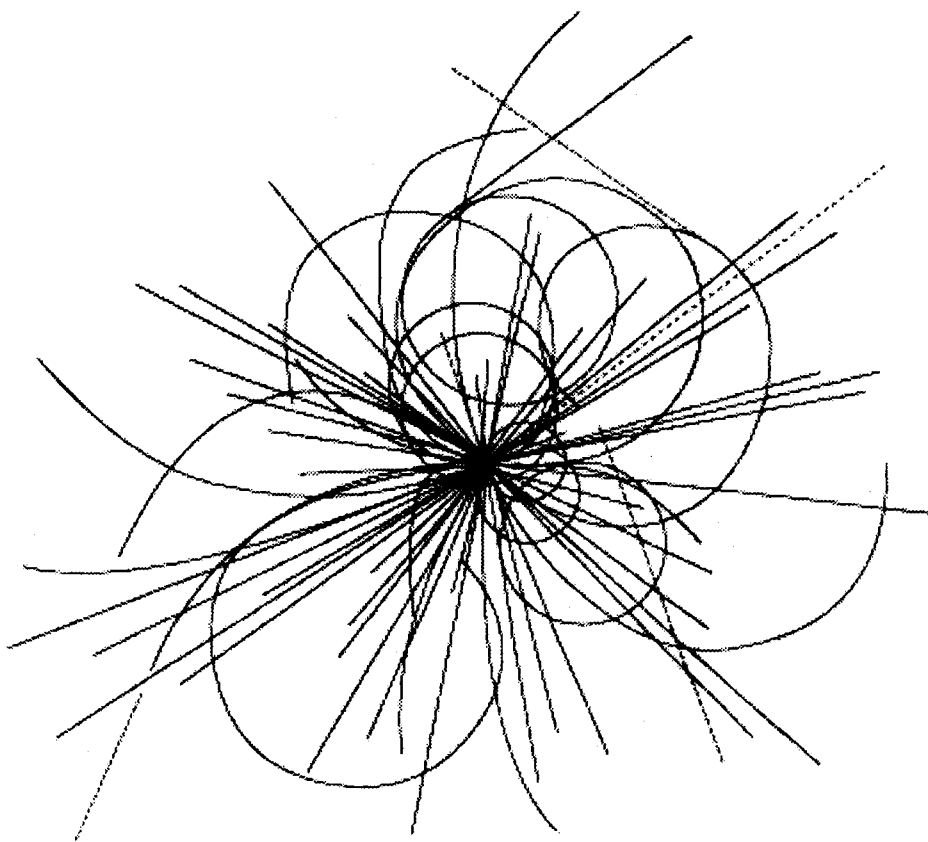


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Superconducting Super Collider
Laboratory

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A QUENCH DETECTION/LOGGING SYSTEM FOR THE SSCL MAGNET TEST LABORATORY

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INTRODUCTION

The quench in a magnet describes a process which occurs while the superconductivity state goes to the normal resistive state. The consequence of a quench is the conversion of the stored electromagnetic energy into heat. During this process the initiating point will reach a high temperature, which will char the insulation or melt the conductor and thereby destroy the magnet. To prevent the magnet from being lost, it is standard practice to observe several resistance and/or inductance voltages across the magnet as quench signatures — Detection. When a quench symptom is detected, protection operations are initiated: proper shutdown of the magnet excitation systems and treatment to dilute the heat energy at a spot — Protection. The temperature rise is diluted by firing heaters along the length of the magnet to insure that the dissipated energy is spread. It is interesting that there is not a significant amount of published research on detection. One reason is that the detection procedure is believed to be a transparent operation based on properly balanced voltage tap signals. Another reason is that there are working detection systems at other laboratory test facilities, which perform fine. Subsequently, for a new test facility, it is customary to adopt an existing system with minor modifications to retain the working experience of the existing system. In reality, the noise environment varies, facility to facility, and it is necessary to understand the existing systems quite well for the specific modification. For example, digitally controlled power supply systems, adopted for the precise control of the excitation current, can produce strong spike noises and consequently increase the false quench detection rate. The addition of simple low pass filters can sometimes reduce the spike heights, but at the expense of a broadened plateau. Power line noise (60 Hz) and its harmonics, communications interference and ground noises can also vary at new installations. To afford a more reliable quench detection system, two distinct approaches have been tried in the past: i) Understanding of the Noise Mechanism [ZhEt92] and Sub-system Optimization [ShEt85], and ii) Escaping from the Known Electromagnetic Noises by Observing Optical Waves [TsEt87] or Acoustic Waves [Dres88]. The MTL of SSCL confronts a mass-measurement of about 10,000 production magnets [Cole92]. To meet the testing schedule, the false quench detection rate needs to be further optimized while the true quench detection rate remains secure for the magnet measurement safety. To meet these requirements, we followed an iterative top-down approach. First we defined the signal and noise characteristics of the quench phenomena by using existing software tools to build a rapid prototype system incorporating all proven functionality of the existing system. Then we further optimize the system through iterative upgrading based on our signal and noise character findings.

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OVERALL ARCHITECTURE

The general design goal of the new system is four-fold: i) reliability, the system will be equipped with more powerful tools such as digital signal processing techniques, ii) flexibility, the system will be modularized for further expansion and external operator interfacing will be enhanced to control the operation of the system, iii) ruggedness, the system will depend on the well-proven standard protocol and unit-tested off-the-shelf sub-systems with minimum re-invention, and iv) adaptivity, each quench event will record the detection history and enable us to later evaluate the algorithms and parameters for future upgrading.

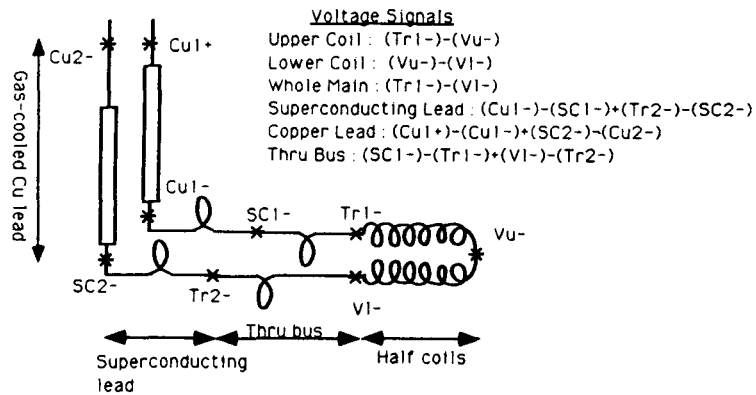


Figure 1. Voltage tap convention.

Hardware: For the SSCL magnet test facility, the overall instrumentation system is modularized with the quench detection system being one module [LaEt92]. The VME readout instrumentation system for the quench detection system is an Analog-to-Digital Converter (ADC), which takes voltage inputs from the isolation amplifiers directly tapping the voltages inside the measurement magnet, the cryostat feed-can interconnection, the transducer signal measuring the power bus current, and the TTL-compatible triggering signal from the backup card. Figure 1 depicts voltage taps from the magnet and the feed can. Isolation amplifiers for the quench detection system have fixed gains to swing the signal of interest within 10% of the full scale of the ADC. Traditionally, the most reliable input voltages are across the magnet coil. To use the prevailing concept of the simple bridge comparison, the whole magnet coil voltage is bisected into half cell voltages of the upper and lower half coil. The well-balanced bridge comparator cancels the inductive voltages of the half coils, and any output of the bridge is attributed to the normal resistive component in one of the coils. To minimize the number of channels for the sampling, symmetric tapped voltages of the positive and negative power buses are added. The power bus-related inputs are the Cu power bus voltage drop, the superconducting (SC) power-lead voltage and the SC through-bus voltage. The isolation amplifiers use Analog Devices AD210 amplifiers, which isolate input, output and power via the transformer couplings which are internal to the modules. The ADC is a DVX-2502 from Analogic accepting 8 differential inputs within ± 10 -V range. A digital output module VMIC/VME2170 is used to output the TTL compatible levels to control the protection system. For the fail-safe operation, an Uninterrupted Power Supply (UPS) backs up all critical electronics, including the quench detection crate and isolation amplifier cards. Another fail-safe card is the backup card, whose main function is to compare the voltage drops across the leads against a fixed threshold, the resistive voltage across the coil against a threshold, and the half-coils voltage difference against a threshold. In the event that the VME crate malfunctions, (for example, due to an unexpected software hangup or a broken hardware card) the analog quench detection system on the backup system will trigger the relevant quench protection systems. The backup card has redundant circuits with separate power supplies. Isolation amplifiers for the voltage taps and the quench detection system are all on the backup card, hence the backup card was designed with the high voltage failures consideration. Also, an analog differentiator is implemented on the backup card, which differentiates the input up to 3 Hz and has a -20 dB/dec roll-off sufficient enough to remove the high frequency noise.

Application Software: The application software has been divided into a set of 3 concurrent modules: i) acquisition, ii) processing and iii) action modules. The acquisition module handles tasks

related to the ADC H/W, and continuously manages several sets of ring buffers. The ring buffer size can be set either short or long. The short size is limited to 20 words, in which the worst system latency is less than the stacking time of the buffer (about 20 ms) for detection and protection. The long size is 1000 words to record the quench signature signals for about 1 second both before and after processing. The processing module implements the core algorithm of the application, to enhance the received signal and test the object measurement quantities. The action module is to interface to the surrounding systems including power supply controller, cryogenic controller, quench protection system and operator interfacing, to broadcast the processing results and gather necessary information. The main processing module is composed of 4 stages:

1. **DATA ACQUISITION:** The data acquisition is the highest priority task except for the system tasks, and affords a uniform sampling timing. Every millisecond the ADC is triggered at the maximum sampling rate of 200 Hz. The first set of 8-channel data is captured and transferred via Direct Memory Access (DMA) to a corresponding ring buffer on MVME147, which results in about 5 ns delay between adjacent samples. Once a quench the event is detected, the contents of the ring buffers are written on the SUN side, via NFS. The data acquisition works like a logger for the quench characterization. With the normal configuration, a dump-out data file keeps the history of 7 buffers of sampled values of the raw signals, 9 buffers of processed signals, and 6 buffers of the quench signature signals.

2. **FILTERING PROCESSING:** Some typical examples of quench induced signals show very strong spike noises over the half cell voltages and the significant 60 Hz component. Several filtering methods used to control these noises include i) the nonlinear spike filtering, ii) linear low pass filtering, iii) differentiation filtering, and iv) 60 Hz harmonics filtering. Since a spike interval is much longer than a single sampling time, the 3-input median filter provides a sufficient spike rejection. Some remaining spikes and resultant false decision will be taken care of by the 2-stage variable threshold decision. A linear low pass filter is implemented by a simple moving average, which is especially useful for low level signature processing with differentiation. Differentiation filtering, giving a 90 degree phase shift while keeping the same magnitude of the input, is implemented in a bi-quad rational form covering all the frequency range up to one half of the sampling frequency [SpBe79].

3. **BALANCING:** Practical data from the DCA 300 series SSC collider dipoles show that the offset level is about 10–30 mV and it becomes a harmful bias to the QDC1 decision threshold when combined with the 100-mV level noise fluctuation. The signature signal offsets are adjusted by initially applying a known signal, such as a periodic saw-tooth, and numerically adjusting the multiplying coefficients.

4. **THRESHOLDING:** To decrease the false decision rate, most probably due to residual spike components, we confirm that the quench decision remains valid through an additional fixed interval. Once a quench signature is detected, the next 10 consecutive samples are tested, and all must exceed the threshold before a quench is declared. If the detected signature value is much bigger than the threshold values, the decision will be shortened proportionally.

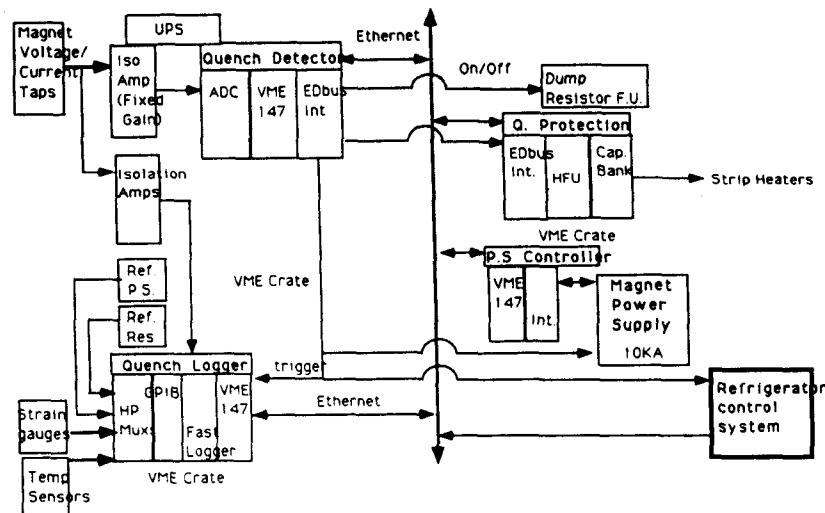


Figure 2. Quench detection system and neighbors.

INTERFACING AND TESTING SETUP

Some of the interacting systems around the quench detection system include the power supply controller, refrigerator control system, and quench protection systems as depicted in Figure 2. The quench detection interface to the power supply puts it into the bypass (short circuit) mode of operation. Interfacing to the quench protection system includes a system to discharge capacitors into heater strips built into the magnet in order to induce quenching over the entire length of the magnet, and de-energization of the magnet through switching in an external dump resistor system. There is additional interfacing to the host for the purpose of operation. Three X-windows are assigned: System-monitor, Quench-monitor and Interactive input. After completing the extensive test of functionality based on the simulation inputs, field experiments were performed at the Fermi National Accelerator Laboratory (FNAL) magnet test facility (MTF), while they were testing superconducting dipole magnets designed for SSC (series number DCA 321, DCA 322 and DCA 323). The quench detection system implemented originally for MTF has run simultaneously with the SSC design. The trip signal from the MTF quench detection system was also recorded and compared to the buffered values of the SSC system. One sample of the results is displayed in Figure 3, where the decision delay between the FNAL and SSC systems is about 6 ms including the software and hardware delays, as expected in the simulations.

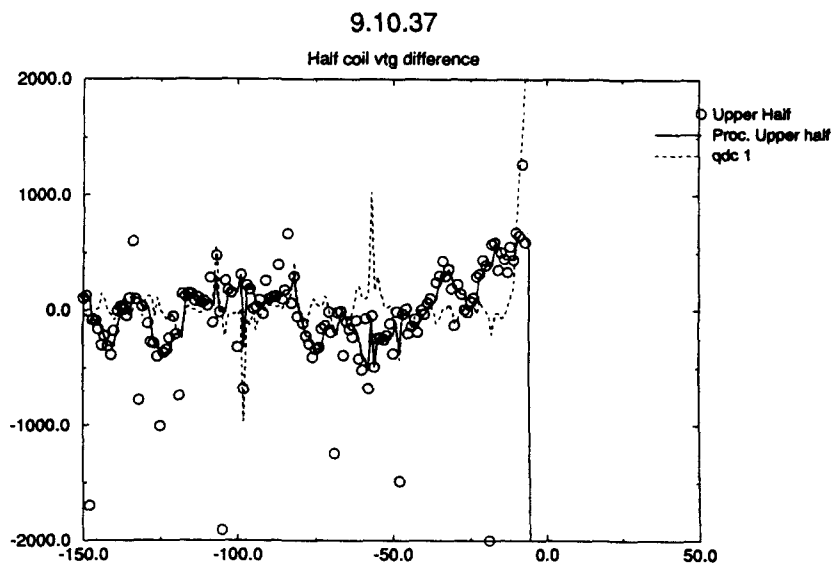


Figure 3. A typical test result: the time scale for the x-axis is 1 ms per tick and the instant $t = 0$ corresponds to the time at which a quench was declared by the SSC system, and shows about 6 ms latency after the time tripped by the FNAL (see the abrupt change at $t = -6$ ms), including the software processing part and the overall hardware.

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