The Quantum Interface Controller: A Full-Stack, Modular, and Scalable System for Qubit Readout and Manipulation

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***Abstract*—Quantum computing has the potential to revolutionize computation by solving complex problems in a way that classical computers cannot. However, robust and scalable qubit manipulation and control electronics are needed to exploit this potential. Academic efforts in this area are sparse, especially in terms of scalability to hundreds or thousands of qubits. The modular and scalable Quantum Interface Controller (QiController), a room-temperature qubit control architecture, addresses this gap. It is implemented using the Advanced Telecommunications Computing Architecture (ATCA) and its dual-dual star topology. The system has two boards: a "Hub" with an AMD Xilinx RFSoC and a "Node" with peripheral FPGAs and DACs for low-latency flux control. This paper describes the system architecture and firmware developments for multi-board synchronization.**

***Index Terms*—Quantum Computing, Qubit, Quantum-Classical Interface, Radio Frequency System-on-Chip (RFSoC), Field Programmable Gate Array (FPGA), Advanced Telecommunications Computing Architecture (ATCA)**

I. Introduction

Quantum computing represents a paradigm shift in computational capabilities, with the potential to solve complex problems that are currently beyond the scope of traditional computers. At the heart of quantum computing is the manipulation and control of qubits, the fundamental units of quantum information.

While there have been significant advances in quantum device fabrication [1], the development of scalable qubit manipulation and control electronics continues to lag behind. Academic efforts in this domain are sparse, especially related to scalability for hundreds or thousands of qubits. Existing architectures based on evaluation boards [2]–[4] frequently lack the modularity and scalability necessary to handle the complexities of mid- and large-scale quantum systems.

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To fill this critical gap, this paper presents the multi-device Quantum Interface Controller (QiController), a novel room-temperature architecture designed to leverage the power of the AMD Xilinx Radio Frequency System-on-Chip (RFSoC) device and utilize the versatility of the Advanced Telecommunications Computing Architecture (ATCA). The multi-device QiController provides a comprehensive solution for managing with a single crate up to 40 superconducting qubits, depending on the specific qubit architecture. Multiple crates can be interconnected for scaling beyond this number.

II. System Architecture

The multi-device QiController architecture depicted in Figure 1 represents an evolution from the previous single-board QiController [5] based on the AMD Xilinx evaluation card ZCU216. While this platform has been instrumental in the characterization and measurement of a single to a handful of qubits, the multi-device QiController is designed to address the scalability and modularity requirements for large-scale qubit manipulation and control systems. The system is comprised of two main components: the "Hub" board and the "Node" board, both designed following the ATCA standard.

A. Description of the ATCA Architecture

The ATCA provides a standardized framework for building modular and scalable systems. Originally developed for telecommunications applications, ATCA-based data acquisition systems have found widespread adoption in scientific research instrumentation, including high-energy physics experiments where 100s of thousands of individual detectors are managed [6]. The high-speed interconnects of ATCA enable efficient data processing and handling within the stringent latency requirements of these experiments.

The multi-device QiController architecture is drafted following the dual-dual star backplane design of ATCA. The crate is able to host up to 4 Hubs and 10 Nodes, equating

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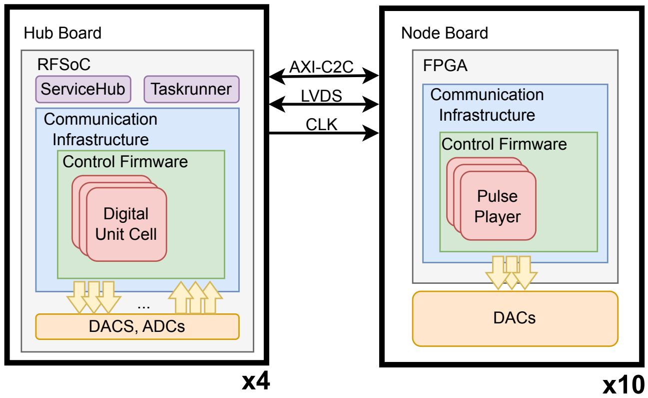

Fig. 1. Modular and scalable multi-device QiController architecture. An ATCA crate hosts 4 Hubs and 10 Node boards.

to a potential total number of 64 high-frequency outputs (filter-selectable from 100 MHz to 8 GHz), 64 high-frequency inputs (filter-selectable from 1 to 7 GHz), and 320 outputs (DC to 1 GHz). The system can expand its capabilities by connecting multiple crates. The crate system ensures low-latency and high-bandwidth data transfer between all boards, essential for real-time qubit control operations.

B. The Hub Board

The Hub board serves as the central processing unit of the multi-device QiController. It coordinates the manipulation and control of qubits and talks to the higher-level software computing stacks using the open-source Python-based qclib library [7] and the two custom software programs running on the processor, the ServiceHub and the Taskrunner [8]. Key components of the Hub board include the AMD Xilinx RFSoC, the analog filters, the clock-distributing network, and both low-latency and high-speed communication interfaces.

The AMD Xilinx RFSoC is a highly versatile platform that integrates hardened processors, Field-Programmable Gate Array (FPGA) fabric, and high-speed Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs), making it well-suited for real-time signal processing tasks. Its programmability and high-performance computing capabilities make it an ideal choice for qubit manipulation and control applications, as demonstrated by the current version of the QiController [5]. Implemented in the programmable logic are the communication infrastructure, the control firmware, our custom real-time scheduler, and the Digital Unit Cell (DUC). The DUC stores and handles all parameters of each physical qubit in the device.

C. The Node Board

The Node board complements the Hub board by providing peripheral FPGA resources and DACs for low-latency flux control. This enables precise and real-time adjustments to qubit coupling, which is essential for implementing complex quantum algorithms and protocols on capable quantum devices. As seen in Figure 1, the programmable logic includes, in addition to the infrastructure firmware, a sub-set of the DUC with only the pulse player features. More information about the firmware blocks can be found in [5].

D. Interconnection Between Boards

The interconnection between boards is facilitated by the dual-dual star backplane where four ports are available between each Node and each Hub in the crate. High-speed serial links (AXI-C2C) enable high-bandwidth data transfers. LVDS serial links are used for low-latency trigger execution and for phase alignment between boards. The backplane also provides the clock distribution network to synchronize all boards with the main clock source, which is by default an external GPS-disciplined PLL connected to the main Hub board.

III. Hardware Demonstrator

The architecture of the multi-device QiController was implemented on commercial off-the-shelf boards consisting of an AMD Xilinx RFSoC ZCU216 board, an AMD Xilinx FPGA VCU118 board, a Skyworks Si5344 clock board, a custom analog front-end board, and a custom-designed adapter board used to interconnect them using the same backplane-defined signals. This was done to develop and validate all relevant interfaces during the design and manufacturing of the ATCA-sized boards.

IV. Conclusion

The multi-device QiController architecture was presented; it leverages the RFSoC device and the ATCA standard to create a modular and scalable qubit control platform. It provides sufficient signals for addressing a 40-qubit device within a single crate while also enabling multi-crate communication. All system interfaces, including timing synchronization, were validated through the construction of a hardware demonstrator using commercial off-the-shelf boards. The innovative architecture of the QiController paves the way for significant advancements in the practical deployment of quantum computing systems, demonstrating a promising path forward for the field.

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