The design of PMT test and analysis system for WFCTA-LHAASO

YINGTAO CHEN[1], MAOMAO GE[1], YONGKANG CHEN[1], JIALI LIU[2], QUNYU YANG[1], JIAHUA WANG[1]
[1]*Department of Physics, Yunnan University, Kunming, China, 650091*
[2]*University of Kunming, Kunming, China, 650214*
chenytao@ynu.edu.cn
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Abstract: A test and analysis system of a prototype photomultiplier tube (PMT) system for wide field of view Cherenkov telescope array (WFCTA) is presented in this paper. This prototype consists of a pre-amplifier stage to invert, amplify, and stretch output signal from PMTs, a dual-gain stage to achieve large dynamic range, and a digital signal processing part to capture and transfer data to host computer by using self-defined algorithm and protocol. A quadra-channel system has been designed and tested and the results show that this design covers a large dynamic scale from 1 pe to 3,500 pe and the maximum data transferring rate reaches 3.5 Mbits/s. These characteristics make it suitable for PMT performance researching and batch testing for WFCTA.

Keywords: photomultiplier tube; test system; Ethernet; WFCTA

1 Introduction

As a light sensor which is superior in response speed and sensitivity, a photomultiplier tube (PMT) is widely used in measuring instruments, medical equipment and high energy physical experiments. In the wide field of view Cherenkov telescope array (WFCTA) of the Large High Altitude Air Shower Observatory (LHAASO) project [1], more than 24,000 PMTs will be used to construct 24 telescopes. As usual, the characteristics of these PMTs will dramatically affect the performance of those telescopes. It means that every single PMT should be researched, tested, and calibrated carefully. And every PMT for this experiment must satisfy given specifications which are used to minimize systematic error and to maximize the lifetime of PMT. For example, the quantum efficiency of these PMTs should be more than 25% around 420 nm and the spectral range could spread from 300 nm to 650 nm to be able to see Cerenkov radiation in air. These PMTs must be operated at a gain of 2.5×10^5 with a high voltage less than 1300 volts. In regard to linearity, we specified that these tubes must be less than $\pm2\%$ non-linearity with up to 30 mA of peak anode current.

In order to achieve this purpose and to fulfill demands of the WFCTA, a PMT test and analysis system, PtAs for short, has been designed, realized, and tested. This system is made up by electronics and peripherals. For batch test, this system is designed to test 37 PMTs maximum at a time in a single run. The High voltages to PMTs can be controlled by host computer as well. And a computer controlled one-dimensional translation stage is used to adjust distance between PMTs and LED to achieve sufficient dynamic range to test linearity of these PMTs. In electronics, a dual-gain amplifier stage has been adopted to increase dynamic range. And it also supports multi-channel for batch test and different acquisition modes for different tests. Captured data will be transferred to host computer through Ethernet by using self-defined protocol. The schema of this test system is showed in figure 1.

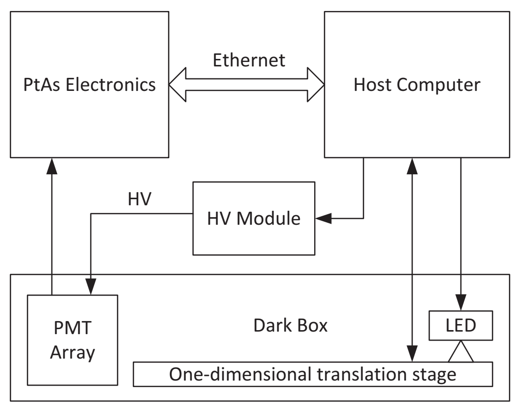

Figure 1: The Schema of PtAs

2 peripherals of the PMT test facility

To satisfy the demands of WFCTA, these characters of every single PMT, such as Gain (vs. high voltage), Single photoelectron response, Linearity of dynamic range, Dark Pulse Rate, Spectral response and Photocathode position response should be tested. We realized a platform to implement these tests. It based on a dark box with a one-dimensional translation stage to alter the distance between PMTs array and LED light source to achieve a large dynamic range for linearity test. The voltages to the PMTs can be controlled by host computer as well as the intensity and frequency of the LED driver. Combined with the electronics of PtAs, 37 PMTs maximum can be tested simultaneously. The signals from PMTs will be sent into host computer after processing by electronic part. To monitor the stability of the system, 5 or 7 permanent standard PMTs located at the center or the corners of the PMTs array. These PMTs are used to monitor the stability of the LED light source, the stability of the electronics and the position response of the PMTs array. We can use them to calibrate our test system.

In the test procedure, we measure the single photoelectron response to calculate the absolute gain of the PMT first. In this step, we turn our light source intensity down until 90% of the time it gives no light and 9% of the time it gives single photon. By using this absolute gain, then we take data at different voltages to measure the function of the gain vs. voltage. It will give us the deviation from linear response when voltage drift. Then setting the PMT's voltage at the gain of 2.5×10^5, we count the number of events per second above single photoelectron to obtain dark pulse rate.

To measure the Linearity of dynamic range, we also designed and implemented a computer-controlled LED driver to generate pulses with a rising and falling time less than 2 ns. We can use one-dimensional translate stage to change the distance between PMTs and LED light source and change the calibre of the Iris diaphragm before the LED light source to alter the intensity of the light. Using these three ways, we can easily cover the needed dynamic range. Measuring data at different position and computing the deviation from the linear response shows us the continuity of the PMT's response with a different amplitude of the signals. Figure 2 show this apparatus and accessories of it which is included LED driver(top-left), PMTs array and translation stage(bottom-left), PtAs electronics(top-right) and PtAs module(bottom-right).

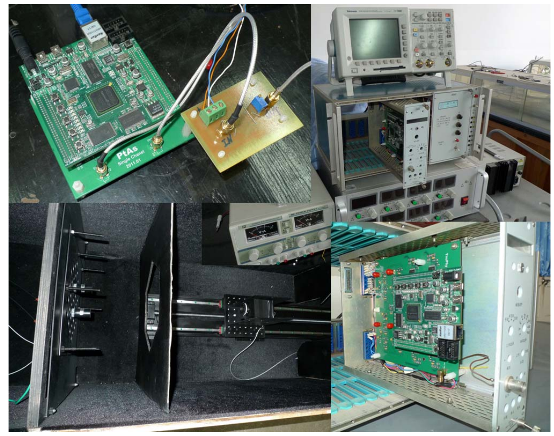

Figure 2: The photo of the apparatus of this system

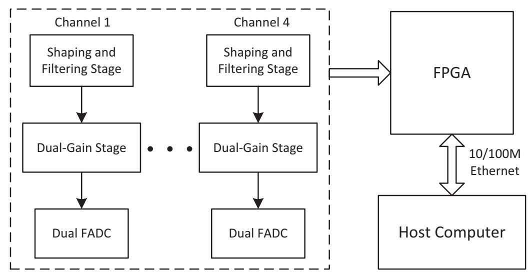

Figure 3: The basic architecture of the electronic part

3 The electronics of PtAs

There are different ways that can be implemented to process PMT signals or to measure the total charge of the pulse [2]. The easiest one is to use a FADC to convert the current or voltage signal to digital directly, but this method depends on the sample rate and the resolution of the FADC. We also can use the time over threshold (TOT) method to handle this signal [3]. But a small offset on input voltage comparator may introduce a large error on an output. Furthermore, considering the cost, convenient to implement and the demands of WFCTA, the architecture based on FADC way has been chosen [4]. In PtAs system, we use two 2nd order Low-pass filters as pre-amplifier stage to shape and filter the signal from PMT. At the output of this stage, the pulse will be shaped and stretched. Figure 3 shows this architecture of PtAs. To achieve about the order of magnitude of 3.5 with proper linearity and the resolution, a dual-gain stage has been included in PtAs. In this stage, an amplifier with a higher gain has been added to circuit in order to increase small signal resolution. With this gain, our system can be used to detect single photoelectron. The other amplifier with unity gain ensures a large dynamic range. This makes us be able to use a FADC with a moderate resolution to handle these signals.

A FPGA can control a maximum of 8 FADCs to implement a quadra-channel system. Digital signal processing part treats PMT data as events and it will be buffered only under specific conditions defined by users. Those data will be transferred to host computer through Ethernet directly by using a 10/100M self-adaptive fast Ethernet MAC controller. Host computer also can send control commands back to FPGA in order to control data acquisition or LED driver pulse generator integrated in it.

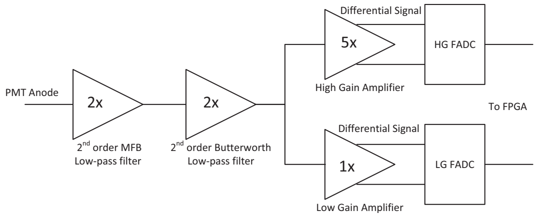

Figure 4: Schema of PMT signal processing

3.1 Analog Signal Processing

As mentioned above, we will use a typical way based on FADC to process the PMT signals. This analog processing stage is composed of a 2nd order multiple feedback (MFB) low-pass filter followed by a 2nd order Butterworth low-pass filter. This gives an output pulse shaped like a Quasi-Gaussian function [5]. Because of the time constant of the shape circuit, every signal that comes from this part will be stretched to about 120 ns. It makes signal large enough be sampled by FADC. Figure 4 shows this procedure. Since this system should cover the order of magnitude of 3.5 of dynamic range, this shape circuit should be followed by a dual-gain amplifier stage. The high gain amplifier has been set at a higher level; about 5X gain, in order to detect single photoelectron and the low gain amplifier with unity gain will make this system enable to spread the dynamic range from 1 pe to 3,500 pe (40 fC to 140 pC @ PMT gain of 2.5×10^5). Without this stage, we will have to increase the resolution of FADC to ensure this range and linearity to cover it. But in this case, two 10-bit FADCs are enough for the application. On the other hand, for the reason to alleviate noise problem and nonlinearity of FADC, the output signals of dual-gain stage will be converted into differential signals. It also can help us to adjust its pedestal (DC level) easily.

3.2 Digital Data Processing

In the PtAs system, we treat PMT signals as events and the time window of an event is 256 bins. An event will store 64 bins before the trigger point and 192 bins after it. This will provide sufficient information about an event. To adapt different types of tests, PtAs also supports multiple acquisition modes, such as threshold value trigger mode, external signal trigger mode, and counting mode for dark noise counting. All channels can be selected separately or altogether for performance researching. If an event has been triggered, all HG and LG channel data will pass through a Ping-Pong buffer to achieve high throughout and avoid data lost. This scheme consumes much more resources than pipeline buffer. But its efficiency is higher than pipeline which makes it usable. Then these buffered data will be read into an off-chip SRAM by using NIOS II CPU [6] with a direct memory access (DMA) mode. By using this controller, we can easily implement Ethernet transferring

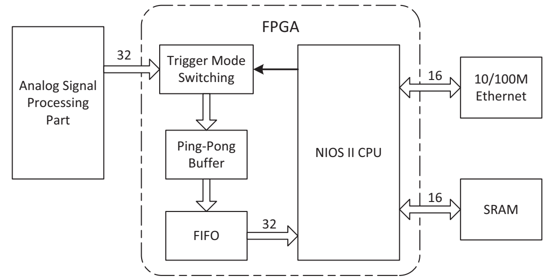

Figure 5: Schema of the digital processing part

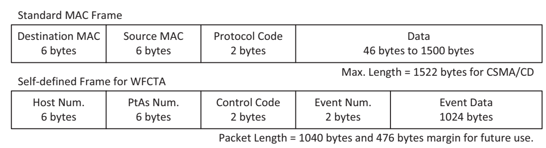

Figure 6: Structure of the standard MAC frame and self-defined frame

and RAM accessing. It can help us to be away from complicated HDL programs. The schema of this part is given in figure 5. As a result of a 32-bit CPU, there are still 6 bit margins (10-bit FADC) when data processing by NIOS II. We use them to distinguish different devices and different channels. For example, if an event has 6 higher bits like "001001", it means that the data come from the 1st PtAs, the 3rd PMT, and the low gain channel. All data will be stored in an off-chip SRAM waiting to transfer.

3.3 Data Transferring and System Control

Our PtAs system is essentially different from typical PMT test system. The later uses standards like VME [7] or PC104 [4] to transferring data and control system, and our system directly uses Ethernet chip to achieve these goals. In this scheme, events will be transferred through Ethernet by using low three levels of OSI stack and a specific frame revised from standard IEEE 802.3 MAC frame [8]. This frame is very similar to standard MAC frame, but we amended it for the WFCTA. We use MAC address to represent different PtAs units and use protocol code to control system. The structure of the standard MAC frame and self-defined frame for the WFCTA can be found in figure 6. But because of using low level protocol, this increases the difficulty of packet capturing. Most operating system cannot deal with those kinds of packets directly. Even in UNIX-like system, OS has to use Berkley Packet Filter (BPF) and Libpcap to complete this job. We designed a data acquisition (DAQ) software based on WinPcap [9], which is call as PtAs Explorer, to capture packets sending from PtAs and send control commands to it. By using it, capturing and analyzing can be finished on-line in real-time easily. In our future works, an analytical function of PtAs explorer will

Feature	Parameters
Channels	1 to 4
Input range	1 pe to 3500 pe
Gain	HG: 20×, LG: 4×
Time resolution	20 ns
FADC reolution	10-bit
FADC voltage scale	0 to 2V
Nonlinearity	$< \pm 2\%$
RMS noise	HG: 0.9LSB, LG: 0.4LSB
Event window	5.12 us
Packet length	1040 bytes
Max. transferring rate	3.5 Mbits/s, 420 events/s

Table 1: Basic Characteristics of PtAs

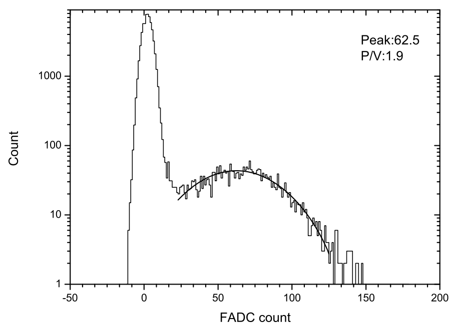

Figure 7: The single photoelectron response

be enhanced and all testing results will be stored in a public database (PDB) for all members of LHAASO project.

4 Characteristics of PtAs

A prototype quadra-channel PtAs has been designed and realized with an Altera Cyclone II FPGA and peripherals. The basic characteristic of this prototype PtAs can be described as Table 1.

This prototype has been tested with Hamamatsu R1924A. As discussed in section 2, the high gain channel has been used to analyzing the single photoelectron response. Figure 7 shows this characteristic. The peak of SPE is located at 62.5 and the P/V ratio is around 1.9. Figure 8 also demonstrates the gain vs. voltage of this tube. the β value of it is about 7.82±0.01 and nonlinearity is less than 0.2%.

5 Conclusion

To achieve the requirements of PMT performance researching and batch testing for the WFCTA of the LHAASO project, a quadra-channel PtAs system is designed and implemented. The system has been used in the research of Hamamatsu R1924A and the results show that it fully satisfied the demands. Its linearity and RMS noise are good enough for detecting single photoelectron response and for a large dynamic testing. By using Ethernet chip, data transferring and system control are direct and convenient.

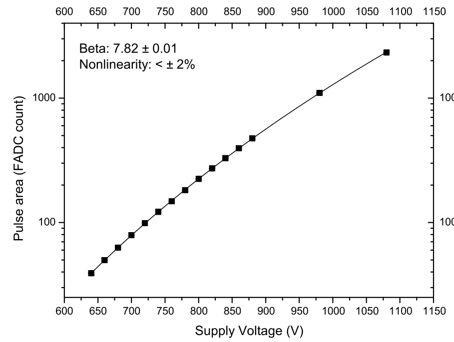

Figure 8: The Gain vs. Voltage curve

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