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SOC BASED TIME-RESOLVED SCALER DAQ AND AMPLIFIER-DISCRIMINATOR UPGRADE FOR LASER SPECTROSCOPY*

S. Kunjir†, E. Bernal, K. Minamisono, D. Morris, S. Zhao
Facility for Rare Isotope Beams, Michigan State University, East Lansing, MI, USA

Abstract

The BEam COoler and LAser spectroscopy (BECOLA) is a collinear laser spectroscopy facility at the Facility for Rare Isotope Beams (FRIB) at Michigan State University. Time resolved laser spectroscopy experiments are performed here to study the nuclear structure of radioactive isotopes. The current data acquisition (DAQ) system being used is based on AMD Spartan 6 field programmable gate array (FPGA) and has a time resolution of 8 ns. There was a need to upgrade existing hardware to meet the requirements for higher time resolution of fast ion detectors. A new DAQ system with AMD Zynq System on Chip (SoC) FPGA based time-resolved scaler was designed, developed and fabricated. It achieves a time resolution of 2 ns. The current amplifier-discriminator has an output pulse resolution of 10 ns. To address this constraint and fully leverage the 2 ns time resolution provided by the new SoC FPGA, a new AD with an output pulse resolution of 1 ns was designed. A brief overview of the upgraded DAQ system will be discussed in this paper, including its features, improvements and future updates.

INTRODUCTION

The Facility for Rare Isotope Beams (FRIB) at Michigan State University conducted the first user scientific experiment in May 2022 [1]. It will make the majority (~80%) of the isotopes predicted to be bound available for experiments. These isotopes will allow researchers to understand atomic nuclei and their role in the Universe. The BEam COoler and LAser spectroscopy (BECOLA) facility [2] at FRIB was designed to accept low-energy beams (< 60/q keV, with q being the ionic charge state) produced at FRIB.

Radioactive isotopes produced in the projectile-fragmentation reactions and subsequent in-flight separation [3] are thermalized in the FRIB gas stopper [4] and extracted at low energy (typically 30 keV). The low-energy beam is then transported to the BECOLA facility. The beam is first injected into the BECOLA Radio Frequency Quadrupole (RFQ) cooler and buncher [5] and then transported to the collinear laser spectroscopy (CLS) beam line. Laser light is overlapped with the ion beam and the resonant fluorescence is detected using a photomultiplier tube as a function of laser frequency and time relative to the beam bunch. The hyperfine structure can be determined from the locations of resonances. Figure 1 shows the BECOLA beamline at FRIB.

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† kunjir@frib.msu.edu.

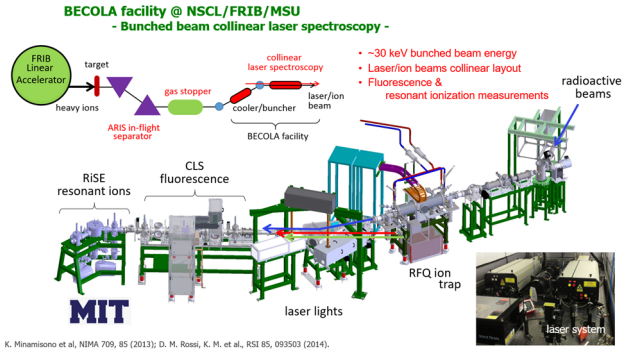

Figure 1: BECOLA beamline.

MOTIVATION

The current data acquisition (DAQ) system in operation at BECOLA was fabricated in 2014 and has a time resolution of 8 ns. This is in part due to the limitation of multiple integrated chip (IC) specifications and design requirements. For example, on the current DAQ, the maximum frequency for sampling input pulses is 125 MHz and the pulse-pair resolution of the amplifier-discriminator (AD) is 10 ns. The motivation was to harness the advancements in FPGA and comparator technology and utilize them to achieve higher time resolution data compared to the existing DAQ.

DAQ

Figure 2 shows the new DAQ chassis and the hardware components. The new DAQ's hardware comprises of (1) FPGA board, (2) DAQ board, (3) switching power supply and (4) solid state drive (SSD). These hardware components reside in a 3U chassis designed to be stand-alone and rack mountable.

The FPGA board is an AMD ZCU102 evaluation board that hosts a Zynq Ultrascale plus Multi-Processor System on Chip (MPSoC), gigabit ethernet interface for networking, serial advanced technology attachment interface for SSD, universal serial bus interface for serial console debugging and high pin count field programmable gate array (FPGA) mezzanine card for interfacing with the DAQ board.

The DAQ board hosts high-speed comparators, radio frequency switches, low noise amplifiers, non-volatile memory for configuration storage, low speed analog-to-digital converter (ADC) and digital-to-analog converter (DAC) for interfacing with external systems, level shifters, low voltage differential signalling (LVDS) buffers and power supply ICs. The switching power supply is 1U fan cooled and supplies power to all hardware components inside the chassis. The SSD hosts root file-system of the

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linux operating system running on one of the processors of the SoC.

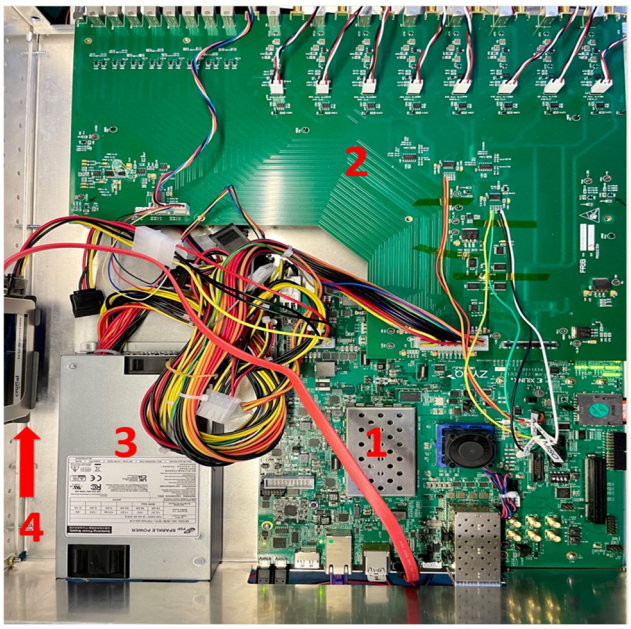

Figure 2: Data flow from PL to PS.

The DAQ features eight input channels, each designed to be compatible with both photomultiplier tubes (PMTs) and ion detectors. One of these input channels can be configured to serve as an external trigger input, enhancing the system's flexibility. Each channel is equipped with a built-in amplifier-discriminator, capable of achieving a pulse-pair resolution of 1 ns, along with a configurable pulse discrimination voltage threshold to accommodate varying signal conditions.

For output, the system provides 16 channels capable of delivering pulse outputs with a fine resolution of as low as 2 ns. Additionally, there is one analog voltage output channel offering a range from -10 V to +10 V, delivered with a high 20-bit resolution for precise voltage adjustments.

Monitoring capabilities include eight amplifier output channels and eight discriminator output channels, allowing for comprehensive observation of the system's operational status. Furthermore, the system is equipped with an output debug port specifically designated for monitoring FPGA signals. Table 1 shows differences between current and new DAQ's component specifications.

Table 1: DAQ Component Comparison

Component	Current	New
AD	LeCroy 821, 10 ns pulse-pair resolution	Custom - 1 ns pulse-pair resolution
DAC	20-bit	20-bit
FPGA	Xilinx Spartan-6	Xilinx Zynq MPSoC
DAQ board	Evaluation kit	Custom - RO4350B, 8 layer

AMPLIFIER-DISCRIMINATOR DESIGN

An amplifier-discriminator circuit with a pulse pair resolution of 1 ns was designed using Gali-74+ amplifier from Mini-Circuits and the TLV3801 comparator from Texas Instruments. The combination of these components allows for precise pulse detection and timing critical for BECOLA application. Attention to the power supply stability and PCB layout was critical (see Fig. 3).

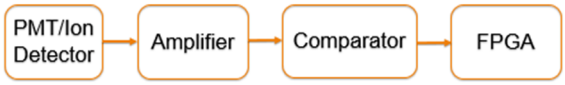

Figure 3: Pulse input chain.

Amplifier

The Gali-74+ amplifier was chosen for its wide operational bandwidth up to 1 GHz [6], which is essential for handling high-frequency signals while maintaining signal integrity. This amplifier provides stable gain, crucial for consistent performance across a wide frequency range. Its low noise figure enhances the signal-to-noise ratio, enabling the effective discrimination of closely spaced pulses.

Discriminator

The TLV3801 comparator was selected for its fast response time with its rise time and fall time of 135 ps and input toggle frequency of 3 GHz [7]. The component's low propagation delay is vital for maintaining the integrity of the pulse timing. The threshold can be adjusted by the user through a resistor pot to optimize sensitivity and specificity in pulse detection, incorporating dynamic adjustments based on preliminary signal observations. The built-in hysteresis of the TLV3801 aids in mitigating noise-related false triggers.

PCB

The PCB utilizes an 8-layer configuration, fabricated using Rogers 4350B material, selected for its low dielectric loss, superior high-frequency performance and robust temperature stability [8]. These attributes are essential for reducing signal attenuation and phase shifts within the GHz frequency range utilized by the circuit. Signal path impedance is precisely calibrated to align with component characteristics and system specifications, ensuring high-fidelity signal integrity and minimizing signal reflections.

FPGA

Firmware

Post-discrimination, the output pulses are conditioned to interface seamlessly with FPGA, preserving the fidelity of the timing information. The FPGA detects and counts pulses and its programmable logic (PL) is optimized to handle the edge detection algorithms required for this task. Once pulses are counted, the data needs to be transferred efficiently to a host linux system for further processing and visualization. To achieve this, the firmware leverages the

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FPGA's direct memory access (DMA) capability to move pulse count data from the PL block random access memory to the shared double data rate memory in processing subsystem (PS) (see Fig. 4).

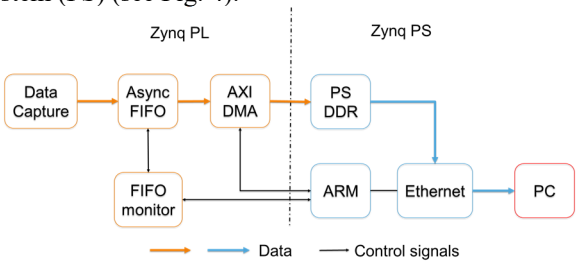

Figure 4: Data flow from PL to PS.

Software

The bare-metal software application is based on embedded systems design approach. It executes high-level tasks for initializing device configuration, controlling fan speed for optimal cooling and serial console debugging.

EPICS IOC

By taking advantage of the new DAQ's FPGA MPSoC, Experimental Physics and Industrial Control System (EPICS) Input/Output Controller (IOC) server was implemented on its A53 quad core processor that hosts Debian root file system and interfaces with Control Systems (CS) Studio Phoebus (see Fig. 5).

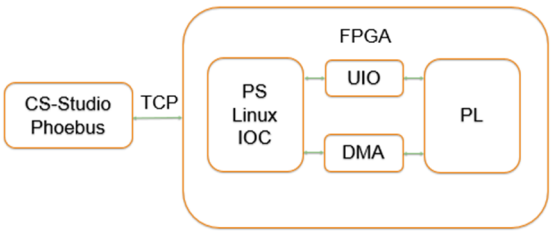

Figure 5: EPICS IOC implementation on DAQ FPGA.

An EPICS driver is deployed on the linux operating system that handles interactions between the user applications and the FPGA's PL registers through the Userspace I/O (UIO) interface. This driver is integral to the system, ensuring seamless integration and robust communication with the FPGA. Additionally, it oversees the DMA transfers through a kernel driver, optimizing the movement of pulse count data from the FPGA directly into system memory at an average throughput of 650 MB/s. This architecture significantly enhances overall system efficiency by alleviating central processing unit workload, thereby facilitating real-time data processing and minimizing latency, which is critical in high-performance operational environments.

FUTURE WORK

Since the DAQ is still under development, it hasn't been used for an experiment yet. Further studies will involve real-world testing to validate the system under various operational conditions.

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