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Surface loss calculations and design of a superconducting transmon qubit with tapered wiring

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Analytical formulas are presented for simplified but useful qubit geometries that predict surface dielectric loss when its thickness is much less than the metal thickness, the limiting case needed for real devices. These formulas can thus be used to precisely predict loss and optimize the qubit layout. Surprisingly, a significant fraction of surface loss comes from the small wire that connects the Josephson junction to the qubit capacitor. Tapering this wire is shown to significantly lower its loss. Also predicted are the size and density of the two-level state (TLS) spectrum from individual surface dissipation sites.

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INTRODUCTION

Quantum computers are made from quantum bits, which have natural sources of noise and dissipation that produce errors in quantum gates. Decreasing these errors increases the size and complexity of quantum algorithms that can be run on a quantum computer. When errors are reduced to about 0.1% per gate operation, then quantum error correction may be used on a large array of qubits in order to lower logical errors and execute vastly more complex quantum algorithms¹. Qubit errors are often limited by the rate of energy decay from loss mechanisms.

Superconducting qubits can be thought of as an inductor-capacitor resonator, with the superconducting Josephson junction giving a non-linear inductance that allows the two lowest energy levels to behave as a qubit. The Josephson junction and the capacitance are designed to be separate physical entities, as illustrated in Fig. 1, and thus can be separately optimized. The size of the Josephson junction is about 100 nm. Its natural capacitance is negligible and junction defects are statistically unlikely because of its small size; the junction can thus typically be modeled as bringing no energy loss. The capacitance is made from superconducting pads with a relatively large millimeter size and about 100 μm spacing, producing a capacitance of about 100 fF for the transmon qubit². When the capacitor is designed properly with control lines weakly coupled to an external circuit, dielectric surface loss from the superconductor and substrate is the dominant mechanism of energy loss. As for any surface loss mechanism, it has been found experimentally that increasing the size of this capacitor lowers the net effect of the surface loss on the qubit device³.

Calculating the surface loss is difficult because of the divergence of the electric fields at the metal edges, which has pushed researchers to solve the problem numerically with finite-element models^{3–7}. More recently, an analytical result was obtained using solutions of conformal mapping, which describes the electric fields of ribbon and coplanar geometries⁸. Unfortunately, this result is only approximate since it assumed the dielectric is thicker than the metal, opposite of the real design. Here, a more practical solution is presented that is valid for a few nanometer lossy dielectric surrounding a much thicker metal layer about 0.1 μm. Changes to the conformal predictions are calculated

using the scaling of corner fields and numerical simulation, and are simple to use and understand.

For planar transmons, ribbon capacitors are typically embedded in a ground plane, and thus the analytical results are not valid. Numerical simulations and fit functions give capacitance and surface loss for this important practical case.

New surface loss predictions are also given for the wires that connect the Josephson junction to the capacitor pads. They typically have a width approximately the size of the junction, about 0.1 μm, and extend in length from the junction to the pads, about 50 μm. They are typically narrow compared to their length and thus have large electric fields at their edges. Conformal and numerical solutions are used to give analytic predictions of surface loss. Their long length produces significant surface loss, which can be reduced by tapering the wires, as illustrated in Fig. 1. I argue that tapering is better than previous stepped designs.

For numerical solutions, meshing is always a concern given the range of size scales, from nanometer thick oxides to millimeter-sized capacitor pads. Meshing is particularly important for 2-D and 3-D numerical solvers where the large grid makes it more difficult to calculate edge fields accurately. In this paper, the assumption of flat substrates (no trenching) allows solutions based on surface charges that are effectively 1-D, so that adaptive meshing at corners to the nanometer scale enables accurate checking of formulas. These formulas are thus a useful standard reference for verifying numerical methods. This is especially needed for experiments where surface loss parameters want to be accurately extracted^{9,10}.

Expressing loss with formulas is also useful since the designer can separate out all the loss mechanisms, instead of modeling the entire device at once using numerical solvers. Optimization is more transparent, for example, trading off the surface loss of the qubit capacitance pads and the junction wires. In order to give useful design formulas for various geometries of the qubit capacitor, the surface loss is analyzed for 3 cases: a parallel plate, a ribbon capacitor where electric fields are between the two electrodes, and a coplanar capacitor where the fields connect through a ground plane. A typical design should be able to be modeled as a combination of these geometries, thus enabling surface loss predictions from formulas derived here.

The initial section introduces the surface loss calculation and shows that the participation ratios have significant contributions

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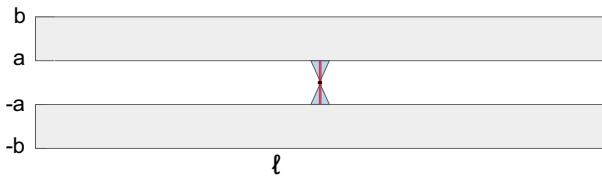


Fig. 1 Qubit design with taper. Drawing of prototypical qubit device, with relative dimensions approximately to scale. The qubit capacitance $C \approx 100 \text{ fF}$ is made from two ribbons (shaded gray) of width $b - a = 100 \mu\text{m}$ and length $\ell = 1300 \mu\text{m}$, separated by distance $2a = 100 \mu\text{m}$. Wires (drawn in red) connect to the sub- μm Josephson junction in a conventional design. Surprisingly, the loss from the small junction wires is about equal to that coming from the large ribbons. This paper proposes tapering these wires (shaded blue) as a near-optimal design.

from dielectric factors. This theory is then applied to the simple case of a parallel plate capacitor, where the surface fields can be calculated readily. The next section considers the case of a coaxial and flat coaxial geometry because the fields can be expressed in simple formulas, thus allowing surface energy to be calculated. Here, important corrections are introduced due to finite thickness of the film. The next three sections give results for the important cases of a ribbon, coplanar and ribbon with ground capacitors. The surface loss from the junction wires are then calculated for both a straight and tapered design, the later showing lower loss. A final section discusses how the splitting spectrum from the two-level-states of the surface loss can be estimated knowing the surface electric fields. The methods section describes how numerical calculations were performed here.

RESULTS AND DISCUSSION

Qubit model and participation ratios

Figure 2 shows an example design of a full differential qubit, include the qubit electrodes and an shielding ground plane (gray). The full design can be broken up into the junction and tapered wires (red), a ribbon capacitor (blue) and a coplanar capacitor (green). The capacitances and losses from the combination of the structures would then be used to optimize the design.

We are interested here in calculating the loss from dielectrics, since the loss from the metallic structures are typically negligible for superconductors. For a crystalline substrate such as silicon or sapphire, the loss is dominated by the thin surface layers of the films⁴: the metal-air (MA), metal-substrate (MS) and substrate-air (SA), typically coming from amorphous oxides.

The total loss tangent for these thin layers is given by $\sum p_i \tan \delta_i$, where surface interface type i has loss tangent $\tan \delta_i$ and participation ratio of the stored energy

$$p_i = \frac{\epsilon_i/2}{W} \int dA t_i |E_i|^2 \quad (1)$$

where the normal volume integral is replaced by a surface integral dA for a thin dielectric layer with thickness t_i , dielectric constant ϵ_i , and a surface electric field E_i . The participation ratio is normalized by the total capacitor energy $W = CV^2/2$, where C is the total capacitance and V the voltage.

When designing the qubit, the qubit capacitance C is usually fixed to a desired parameter. Because the results are more easy to interpret in terms of design distances, it is convenient to describe the qubit capacitance in terms of a length using

$$C \equiv \epsilon_0 L. \quad (2)$$

For $C = 100 \text{ fF}$, a value used for a qubit non-linearity of about 200 MHz, one finds $L = 11.3 \text{ mm}$.



Fig. 2 Example of full transmon design. Example design of a differential transmon qubit that incorporates several of the capacitance structures described here. Red shows the junction and tapered wire, blue is a ribbon capacitor, and green is a coplanar capacitor. The outer ground plane is gray. The capacitances and losses would be added to give a good approximation for the entire design.

For thin films, the electric fields of the top and bottom dielectrics can be considered separately. Thus the electric fields E_0 can be solved for $\epsilon = \epsilon_0$, the free space value, and then the participation ratio is multiplied by 1 for the solution on the air side and ϵ_s for the substrate side. The surface dielectrics can be taken into account with the three participation ratios⁴

$$p_{\text{MA}} = \frac{1}{\epsilon_{\text{MA}} L \epsilon_0/2} \left[\frac{\epsilon_0}{2} \int_{\text{MA}} dA |E_0/V|^2 \right], \quad (3)$$

$$p_{\text{MS}} = \frac{\epsilon_s^2}{\epsilon_{\text{MS}} L \epsilon_0/2} \left[\frac{\epsilon_0}{2} \int_{\text{MS}} dA |E_0/V|^2 \right], \quad (4)$$

$$p_{\text{SA}} = \frac{\epsilon_{\text{SA}}}{\epsilon_{\text{SA}} L \epsilon_0/2} \left[\frac{\epsilon_0}{2} \int_{\text{SA}} dA |E_0/V|^2 \right], \quad (5)$$

where the area integrals correspond to the appropriate surfaces for each type, and the bracketed terms are called surface energies. Tangential fields are only included for the SA formula, as appropriate for thin films⁴. For the above MA and MS surface energies, the electric field is for only one side of the metal. Thus for the total surface energy U calculated in the next sections, the above MA and MS energies in brackets should be $U/2$.

Dielectric constants are for a silicon substrate $\epsilon_s = 11.7$, aluminum oxide $\epsilon_{\text{MA}} = \epsilon_{\text{MS}} = 9.8$, and silicon dioxide $\epsilon_{\text{SA}} = 3.8$; the relative weights of the MA:MS:SA dielectric terms are 0.10:14:3.8.

Differential parallel plate capacitor

The simplest geometry is a parallel plate capacitor, which allows a simple calculation of the surface loss due to constant electric fields. A differential geometry is illustrated in Fig. 3. This contribution is typically needed when transmon qubits are made

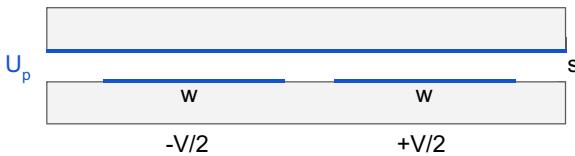


Fig. 3 Differential parallel plate. Side view of a differential parallel-plate capacitor. The parallel plate has width w and length ℓ , using a separation s of a vacuum gap. The differential voltage drive is $\pm V/2$. The surface energy is U_p .

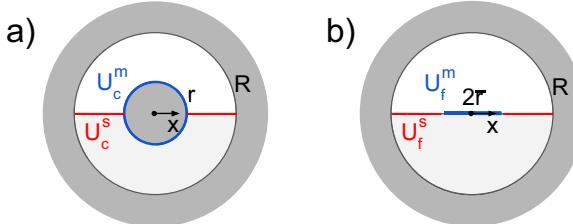


Fig. 4 Coaxial geometries. Drawings of coaxial geometries considered here. **a** Cross section of coax, with inner radius r and outer radius R . **b** Cross section of flat coax, with width $2\bar{r}$ of inner thin film. The surface energies of the metal and substrate are U^m and U^s respectively, with the subscripts referring to the coax (U_c) or flat coax (U_f) cases. The x -direction is horizontal and the shaded regions correspond to the substrate.

using bump-bonded substrates, where the second substrate acts as a ground plane above the qubit metal pads and thus adds capacitance to the qubit. This structure can be treated as parallel plate with each plate having width w and length ℓ and a separation s to the ground plane, with capacitance

$$C_p = (1/2)\epsilon_0\ell w/s, \quad (6)$$

where the $1/2$ factor coming from the differential design of the qubit, where the capacitance of each parallel plate is in series.

The electric field in each differentially driven capacitor is $E_p = V/s$, and the total surface energy is

$$U_p = (\epsilon/2)2(2\ell w)(V/2s)^2, \quad (7)$$

where a factor of 2 comes from the two parallel plates, and another from surface loss at the 2 plates of the capacitor.

The participation ratio for the parallel-plate capacitor is

$$p_{MA}^p = \frac{1}{\epsilon_{MA}} \frac{t_{MA} \ell w}{L s^2}. \quad (8)$$

Participation ratios are written with first the dielectric factor, then the dielectric thickness, and finally the geometric factors for the design.

Thickness correction

The finite thickness of the metal film changes the surface electric fields mostly at the edges of the film. Since the edge fields will be similar for different geometries, their effect will be calculated here for a simple flat coaxial film. The resulting simple correction to the surface energy can then be applied to different geometries.

It is useful to start with a 2-D solution of a coax line, with an inner conductor of radius r and an outer conductor of radius R as illustrated in Fig. 4a. The solution for the radial electric field on the surface of the inner conductor is

$$E_c = \frac{V}{r \ln(R/r)}, \quad (9)$$

with its strength decreasing with radius x as

$$E_c(x) = (r/x)E_c \quad (10)$$

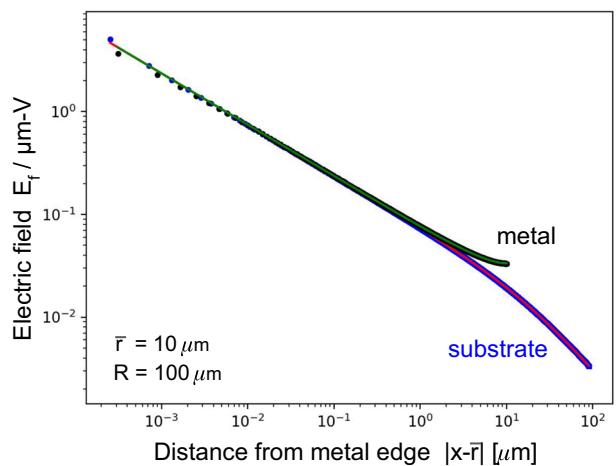


Fig. 5 Electric field of flat coax. Plot of the surface electric field for a flat coax for both the metal surface (black) and substrate (blue), obtained by numerical simulation (dots) for the zero thickness limit. The solid lines (green, red) are predictions from Eqs. (15) and (16) and fit well the numerics. Parameters are $\bar{r} = 10 \mu\text{m}$ and $R = 100 \mu\text{m}$.

The electric field energy $(\epsilon/2)\int E^2 dv$ is calculated from a volume integral dv of the electric field E . Because the interest here is for the surface energy in a 2-D geometry, we compute the surface energy U/ℓ for a line length ℓ so that the full energy will be multiplied by the surface thickness and length ℓ . For the coax geometry, the surface energy of the inner metal at radius r is

$$U_c^m/\ell = (\epsilon/2)2\pi r E_c^2 \quad (11)$$

$$= \epsilon E_c^2 r \pi. \quad (12)$$

The surface energy coming from the substrate, the red line in Fig. 4a, is a cut through the middle of the coax

$$U_c^s/\ell = (\epsilon/2) 2 \int_r^R E_c(x)^2 dx \quad (13)$$

$$= \epsilon E_c^2 r [1 - r/R], \quad (14)$$

where the factor of 2 before the integral comes from the left and right substrate sides.

Figure 4b shows a flat coax, where the circular inner conductor is replaced by a thin film of width $2\bar{r}$. The electric field magnitude along the coordinate x of the thin film is found from numerical solutions for all x to be given by a conformal-mapping solution

$$E_f = \frac{V}{\bar{r} \ln(2R/\bar{r})}, \quad (15)$$

$$E_f(x) = E_f \sqrt{\frac{\bar{r}}{|\bar{r} + x|}} \sqrt{\frac{\bar{r}}{|\bar{r} - x|}}, \quad (16)$$

which fits well for $R > 2\bar{r}$. The electric field is perpendicular to the metal surface but parallel to the substrate surface. The voltage integral checks properly

$$\int_{\bar{r}}^R E_f(x) dx = V[1 + O(\bar{r}^2/R^2)]. \quad (17)$$

Figure 5 shows a comparison between the numerical solution and the formula of Eqs. (15) and (16), showing excellent agreement. The square-root divergence at the metal edge is characteristic of the electric fields of thin metal films.

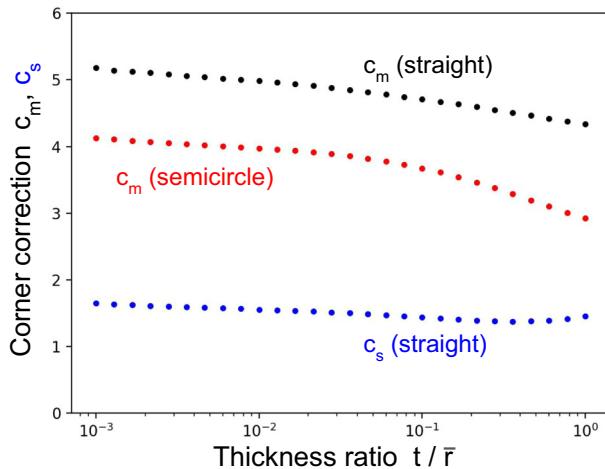


Fig. 6 Corner corrections. Plot of corner corrections obtained by numerical simulation of films with finite thickness t/\bar{r} and a straight vertical edge, for the metal c_m (black) and substrate c_s (blue). Data in red is for a semi-circular edge, showing that sharp corners have a non-negligible but non-dominant effect. The corrections vary slowly with thickness and are taken as $c_m = 5.0$ and $c_s = 1.6$.

The surface energy for the metal surface ($|x| < \bar{r}$) is

$$U_f^{m1}/\ell = (\epsilon/2)E_f^2 4 \int_0^{\bar{r}-t/2} \frac{\bar{r}^2}{\bar{r}^2 - x^2} dx \quad (18)$$

$$\simeq \epsilon E_f^2 \bar{r} \ln(4\bar{r}/t) \quad (19)$$

where the factor of 4 is for the top/bottom and left/right parts of the metal, and the logarithmic divergence in the integral at the edge is cut-off at half the thickness t of the film.

Numerical simulation for a film with a rectangular cross-section of thickness t shows that the electric fields within $t/2$ of the outside corner have a power law behavior with exponent $p = -1/3$, as appropriate for a 90 degree corner^{4,11}. As an initial approximate solution, this power law dependence of the corner field is then matched to the computed field $E_f(\bar{r} - t/2)$ at a distance $t/2$ from the corner. At a distance r_c from the corner, the corner field is

$$E_c = E_f(\bar{r} - t/2) [r_c/(t/2)]^p \quad (20)$$

$$= E_f \sqrt{\bar{r}/t} [2r_c/t]^p. \quad (21)$$

Including all 4 corners, with 2 sides per corner, the line energy for the corner is approximately

$$U_f^{m2}/\ell = (\epsilon/2)E_f^2(\bar{r}/t) 8 \int_0^{t/2} [2r_c/t]^{2p} dr_c. \quad (22)$$

$$= 4\epsilon E_f^2(\bar{r}/t)(t/2)/(1 + 2p) \quad (23)$$

$$= \epsilon E_f^2 \bar{r} [2/(1 + 2p)]. \quad (24)$$

With $1 + 2p = 1/3$, the numerical factor in Eq. (24) is 6 and does not depend on t .

The total surface energy for the metal is the sum of the two energies

$$U_f^m/\ell = \epsilon E_f^2 \bar{r} [\ln(4\bar{r}/t) + c_m], \quad (25)$$

where c_m is the corner correction for the finite thickness of the metal. Figure 6 gives c_m obtained from numerical integration of the surface energy. The corner correction is slowly varying with relative film thickness t/\bar{r} and has a typical value

$$c_m = 5.0 \quad (26)$$

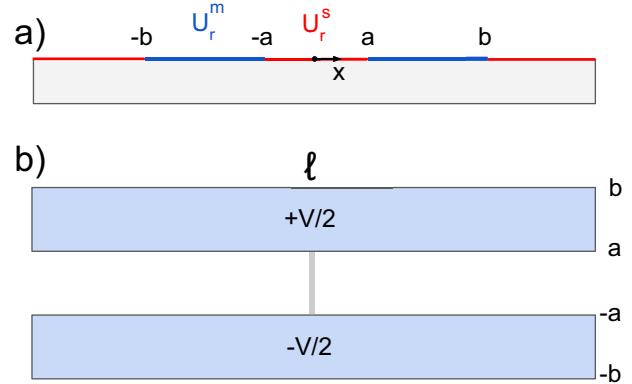


Fig. 7 Differential ribbon. **a** Cross section of a differential ribbon capacitor, with metal conductors from $-b$ to $-a$ and a to b . The surface energies for the metal and substrate are U_r^m and U_r^s , respectively. **b** Top view, showing a capacitor of length ℓ and differentially driven by $\pm V/2$. The gray bar shows typical location of the junction wires. The x -direction is horizontal and the shaded region corresponds to the substrate.

close to the value 6 obtained above by scaling of the corner fields. It is useful that the surface energy is predicted well even for a thick film, with thickness as much as one-half the width. The edges typically contribute about 1/3 of the total surface energy. Also shown is the case of a semicircular edge, which lowers the surface energy a non-negligible but small amount, providing a lower bound for the correction of a rounded edge.

This result shows that a constant term added to the logarithmic cut-off term well represents the corner fields. Note the similarity to Eq. (12). Here, the bracket term in Eq. (25) is slightly larger than the corresponding π constant in Eq. (12), as expected since the flat coax has large edge fields. The correction factor $\ln(4\bar{r}/t) \rightarrow \ln(4\bar{r}/t) + c_m$ will be used in all formulas for the metal edge.

The surface energy for the substrate surface ($\bar{r} < x < R$) is

$$U_f^{s1}/\ell = (\epsilon/2)E_f^2 2 \int_{\bar{r}+t/2}^R \frac{\bar{r}^2}{x^2 - \bar{r}^2} dx \quad (27)$$

$$= \epsilon E_f^2 (\bar{r}/2) \left[\ln(4\bar{r}/t) - \ln \frac{R + \bar{r}}{R - \bar{r}} \right], \quad (28)$$

where the factor of 2 is for the left/right parts of the substrate. Like found for the metal surface, numerical integration for finite thickness gives a corner correction 1.6. Since typically $\bar{r} \ll R$, the total substrate surface energy is

$$U_f^s/\ell = \epsilon E_f^2 (\bar{r}/2) [\ln(4\bar{r}/t) + c_s - 2\bar{r}/R], \quad (29)$$

$$c_s = 1.6. \quad (30)$$

This is smaller than the surface energy for the metal surface since it does not include a sharp edge. The correction factor $\ln(4\bar{r}/t) \rightarrow \ln(4\bar{r}/t) + c_s$ will be used in all formulas for the substrate edge.

Differential ribbon capacitor

Considered next is the capacitance between the two leads of the qubit, modeled as two long and straight ribbons as illustrated in Fig. 7. Each ribbon has metal spanning a distance a to b from the centerline, with length $\ell \gg b$ and a metal thickness t . A conformal-mapping solution from Ref. ⁸ is used for the electric fields. The

ribbon capacitance for a differential voltage V is

$$C_r = [(\epsilon_s + 1)/2] \epsilon_0 \ell / C_K(a/b), \quad (31)$$

$$C_K = K(a/b) / K'(a/b) \quad (32)$$

$$\simeq (1/\pi) \ln[2(1 + \sqrt{a/b})/(1 - \sqrt{a/b})], \quad (33)$$

$$K'(k) = K(\sqrt{1 - k^2}) \quad (34)$$

where $K(k)$ is the complete elliptic integral of the first kind. Equation (33) is an excellent approximation to Eq. (32). The effective dielectric constant has contribution from both the air ($\epsilon_0/2$) and substrate ($\epsilon_s \epsilon_0/2$).

From the conformal-mapping solution Eq. (5) of Ref.⁸, the surface fields are

$$|E_r(x)|^2 = \left(\frac{V/2}{K(a/b)} \right)^2 \frac{b^2}{|(x^2 - a^2)(x^2 - b^2)|}, \quad (35)$$

where the E field is parallel to the surface on the substrate and perpendicular on the metal. The surface integral is evaluated in three sections:

$$\text{inner } 0 < x < a - t/2, \quad (36)$$

$$\text{center } a + t/2 < x < b - t/2, \quad (37)$$

$$\text{outer } b + t/2 < x < \infty, \quad (38)$$

giving

$$S_i = \int_0^{a-t/2} dx \frac{b^2}{|(x^2 - a^2)(x^2 - b^2)|} \quad (39)$$

$$= \frac{1}{a} \ln \frac{a+x}{a-x} + \frac{1}{b} \ln \frac{b-x}{b+x} \Big|_0^{a-t/2} \quad (40)$$

$$\simeq \frac{1}{a} \ln \frac{4a}{t} + \frac{1}{b} \ln \frac{b-a}{b+a}, \quad (41)$$

$$S_c \simeq \frac{\frac{1}{a} (\ln \frac{4a}{t} + \ln \frac{b-a}{b+a}) + \frac{1}{b} (\ln \frac{4b}{t} + \ln \frac{b-a}{b+a})}{2(1 - a^2/b^2)}, \quad (42)$$

$$S_o \simeq \frac{\frac{1}{a} \ln \frac{b-a}{b+a} + \frac{1}{b} \ln \frac{4b}{t}}{2(1 - a^2/b^2)}. \quad (43)$$

Note that $S_c = S_i + S_o$.

The surface energy of the center metal section is

$$U_r^m / \ell = (\epsilon/2) 4 [V/2K(a/b)]^2 S_c \quad (44)$$

$$= \frac{\epsilon V^2}{2 K^2(a/b)} \frac{S_a(c_m)}{a}, \quad (45)$$

$$S_a(c_m) \equiv \frac{(\ln \frac{4a}{t} + c_m + \ln \frac{b-a}{b+a}) + \frac{a}{b} (\ln \frac{4b}{t} + c_m + \ln \frac{b-a}{b+a})}{2(1 - a^2/b^2)} \quad (46)$$

where the factor of 4 comes from the two ribbons and the top/bottom surfaces. The dimensionless surface integral is obtained from $S_a/a = S_c$, along with adding the corner correction c_m for a finite thickness.

The surface energy of the inner and outer substrate sections is

$$U_r^s / \ell = (\epsilon/2) 2 [V/2K(a/b)]^2 (S_i + S_o) \quad (47)$$

$$= \frac{\epsilon V^2}{4 K^2(a/b)} \frac{S_a(c_s)}{a}, \quad (48)$$

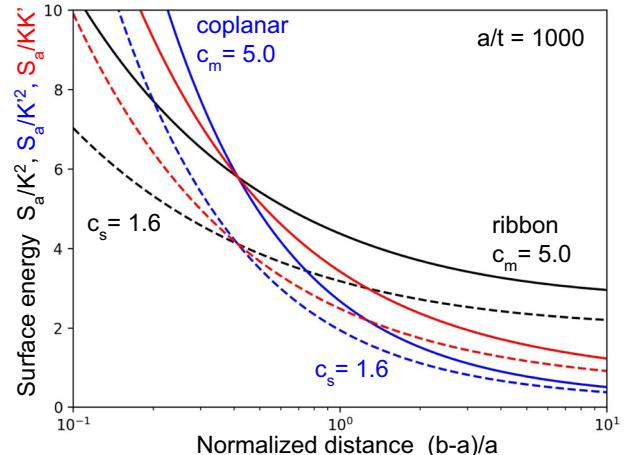


Fig. 8 Surface energies. Plot of the normalized surface energies $S_a(c_m)/K^2$ for ribbon (black) and $S_a(c_s)/K^2$ for coplanar (blue) geometries, versus the normalized distance $(b-a)/a$. The plot uses the normalized thickness $a/t = 1000$. The solid lines are for the metal surface with $c_m = 5.0$, whereas dashes are for the substrate with $c_s = 1.6$. Also plotted in red is S_a/KK for the case of all capacitance coming from the ribbon or coplanar geometry.

where the factor of 2 is from the two sides of the ribbon. The substrate surface energy is smaller than the metal by approximately a factor of 2.

The ribbon capacitor has participation ratios coming from the surface-air, metal-substrate, and substrate-air interfaces, calculated using Eqs. (3)–(5), (45) and (48)

$$p_{MA}^r = \frac{1}{\epsilon_{MA}} \frac{t_{MA}}{L} \frac{\ell}{a} \frac{S_a(c_m)}{2 K^2(a/b)}, \quad (49)$$

$$p_{MS}^r = \frac{\epsilon_s^2}{\epsilon_{MS}} \frac{t_{MS}}{L} \frac{\ell}{a} \frac{S_a(c_m)}{2 K^2(a/b)}, \quad (50)$$

$$p_{SA}^r = \epsilon_{SA} \frac{t_{SA}}{L} \frac{\ell}{a} \frac{S_a(c_s)}{2 K^2(a/b)}. \quad (51)$$

The only difference in the 3 participation ratios is the dielectric factors and the small change from the corner constant.

The black lines in Fig. 8 are a plot of the dimensionless surface energy $S_a(c_m)/K^2$ for the metal (solid) and $S_a(c_s)/K^2$ for the substrate (dashed) as a function of the normalized distance $(b-a)/a$. The metal surface energy is greater because of the higher corner constant $c_m > c_s$. As the distance $b-a$ increases, the surface energy decreases. Typical designs use $(b-a)/a \sim 1$. Note that the surface energy drops by a non-negligible amount with the lower corner constant, showing that the edge fields from the finite thickness are important.

For the case where all of the capacitance comes from the ribbon $C_r = \epsilon_0 L$, the participation for the metal-substrate interface is

$$p_{MS}^r(C_r) = \frac{\epsilon_s^2}{\epsilon_{MS}(\epsilon_s + 1)/2} \frac{t_{MS}}{a} \frac{1}{2} \frac{S_a(c_m)}{K(a/b)K'(a/b)}. \quad (52)$$

The last factor is the geometric mean of the ribbon and coplanar curves of Fig. 8, shown in red.

Differential coplanar capacitor

The qubit can also have capacitance to ground. This can be modeled as a coplanar structure as shown in Fig. 9, where each side of the qubit has a pad with width $2a$ and length $\ell \gg a$, with a ground plane at a distance b from the centerline. As this is the “dual” of the ribbon capacitor, with metal and substrate switched, similar conformal solutions can be used with minor modifications.

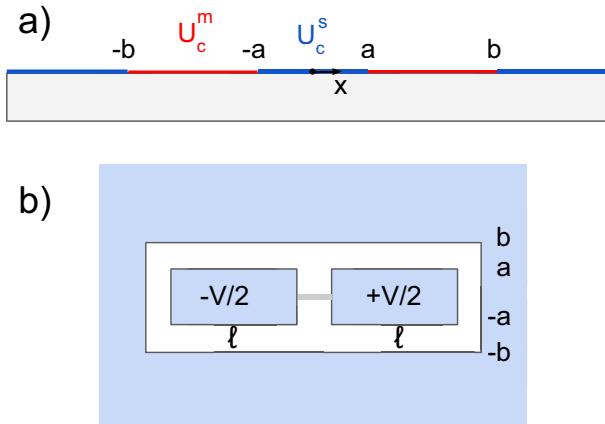


Fig. 9 Differential coplanar. **a** Cross section of a differential coplanar capacitor, with metal conductors from $-\infty$ to $-b$, $-a$ to a , and a to ∞ . The surface energies for the metal and substrate are U_c^m and U_c^s respectively. **b** Top view, showing each differential electrode with length ℓ and driven by $\pm V/2$. The gray bar shows typical location of the junction wires. The x -direction is horizontal and the shaded region corresponds to the substrate.

The differential capacitance is

$$C_c = (1/2)[(\epsilon_s + 1)/2] \epsilon_0 \ell 4C_K(a/b), \quad (53)$$

where C_K is defined in Eq. (32), and the initial factor of 1/2 comes from the two coplanar capacitors in series. From Eq. (25) of Ref. ⁸, the electric field for each coplanar capacitor is

$$|E_c(x)|^2 = \left(\frac{V/2}{K'(a/b)} \right)^2 \frac{b^2}{|(x^2 - a^2)(x^2 - b^2)|}, \quad (54)$$

where now the field is perpendicular to the substrate in the inner and outer sections, and parallel in the center.

The surface energy of the metal sections is similar to the ribbon case except for an extra factor of 2 to account for the series capacitors, as can be seen from Fig. 9 since ℓ only accounts for half of the total length. The metal and substrate surface energies are

$$U_c^m/\ell = \frac{\epsilon V^2}{K'^2(a/b)} \frac{S_a(c_m)}{a}, \quad (55)$$

$$U_c^s/\ell = \frac{\epsilon V^2}{2K'^2(a/b)} \frac{S_a(c_s)}{a}, \quad (56)$$

Note the similarities to the ribbon formulas. The participation ratios are twice as large as the ribbon and with K replaced by K'

$$p_{MA}^c = \frac{1}{\epsilon_{MA}} \frac{t_{MA}}{L} \frac{2\ell}{a} \frac{S_a(c_m)}{2K'^2(a/b)}, \quad (57)$$

$$p_{MS}^c = \frac{\epsilon_s^2}{\epsilon_{MS}} \frac{t_{MS}}{L} \frac{2\ell}{a} \frac{S_a(c_m)}{2K'^2(a/b)}, \quad (58)$$

$$p_{SA}^c = \epsilon_{SA} \frac{t_{SA}}{L} \frac{2\ell}{a} \frac{S_a(c_s)}{2K'^2(a/b)}. \quad (59)$$

For the case where all the capacitance comes from the coplanar structure, the participation is the same as the ribbon design, for example

$$p_{MS}^c(C_c) = p_{MS}^r(C_r). \quad (60)$$

A single-ended coplanar design is used to test resonators. In this case, the coplanar capacitance of Eq. (53) does not have the initial 1/2 term. The surface energy U and participation ratios are a factor

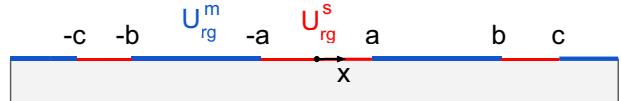


Fig. 10 Differential ribbon with ground. **a** Cross section of a differential ribbon capacitor with ground conductors added from $-\infty$ to $-c$ and c to ∞ . The surface energies for the metal and substrate are U_{rg}^m and U_{rg}^s respectively.

of 2 larger. The participation $p_{MS}^r(C_c)$ includes these two factors, so Eq. (60) is unchanged for the single-ended design.

Differential ribbon capacitor with ground

Planar transmons are typically designed to have a ground plane surrounding the qubit capacitor, as shown in Fig. 2. For the ribbon capacitor considered previously, a ground plane is added here from minus infinity to $-c$ and c to infinity, where $c > b$, as shown in Fig. 10. The capacitance and surface loss is computed numerically and then fit to functions based on the previous ribbon formulas.

The surface electric field is well described a simple modification to the ribbon case of Eq. (35)

$$|E_{rg}(x)|^2 = |E_r(x)|^2 \frac{c^2}{|x^2 - c^2|}. \quad (61)$$

Integration of surface charge from the numerical solutions gives a simple modification to the ribbon differential capacitance of Eq. (31)

$$C_{rg} \simeq C_r / [1 - (x_e/c)^2]^{0.23}, \quad (62)$$

$$x_e = b - 0.15(b - 1.2a). \quad (63)$$

Figure 11 shows the numerical results (points) and the fit function (line) versus ground plane separation $(c - b)/b$ for three values of a , representative of a/b ratios that would commonly be used. The fit function represents the numerical results well.

For the surface loss of the metal, the fit function for the numerical results are

$$U_{rg}^m/\ell = \epsilon V^2 \left[\frac{0.98}{2K'^2(a/b)} \frac{S_a(a, b, t, c_m)}{a} \right] \quad (64)$$

$$+ \frac{1.70}{2K'^2(b/c)} \frac{S_{ao}(b, c, t, c_m)}{b}, \quad (65)$$

where the contribution of S_{ao} corresponds to the outer metal of a coplanar capacitor between b and c

$$S_{ao}(b, c, t, c_m) = \frac{\ln \frac{c-b}{c+b} + \frac{b}{c} (\ln \frac{4c}{t} + c_m)}{2(1 - b^2/c^2)}. \quad (66)$$

The surface loss for both the inner and outer substrate gaps gives the fit function

$$U_{rg}^s/\ell = \epsilon V^2 \left[\frac{0.95}{4K'^2(a/b)} \frac{S_a(a, b, t, c_s)}{a} \right] \quad (67)$$

$$+ \frac{0.80}{4K'^2(b/c)} \frac{S_a(b, c, t, c_s)}{b}, \quad (68)$$

where the second contribution of S_a corresponds to the substrate of a coplanar capacitor between b and c . Figure 11 shows the numerical results are well represented by the fit functions.

Differential junction wires

The connections between the Josephson junction and the capacitor electrodes are made through two junction wires of total length $2d$, as shown in Fig. 12. Starting with the simple case

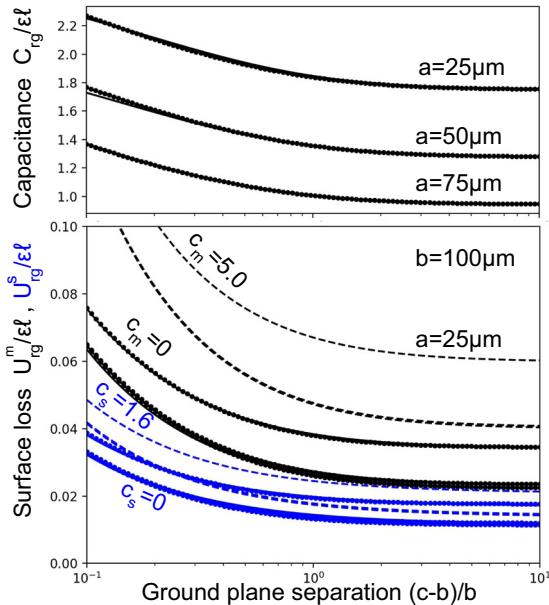


Fig. 11 Capacitance and loss numerics. Plot of the capacitance (top panel) and surface loss (bottom panel) versus the ground plane separation $(c-b)/b$, for $a = (25, 50, 70) \mu\text{m}$ (top to bottom) and $b = 100 \mu\text{m}$. Points are numerical simulations and lines are fit formulas. The metal and substrate surface loss is colored black and blue, respectively. Numerical simulations are for an infinitely thin metal with an integration cutoff $t/2 = 0.05 \mu\text{m}$, with the fit also using $c_m = c_s = 0$. Dashed lines include corner correction $c_m = 5.0$ and $c_s = 1.6$.

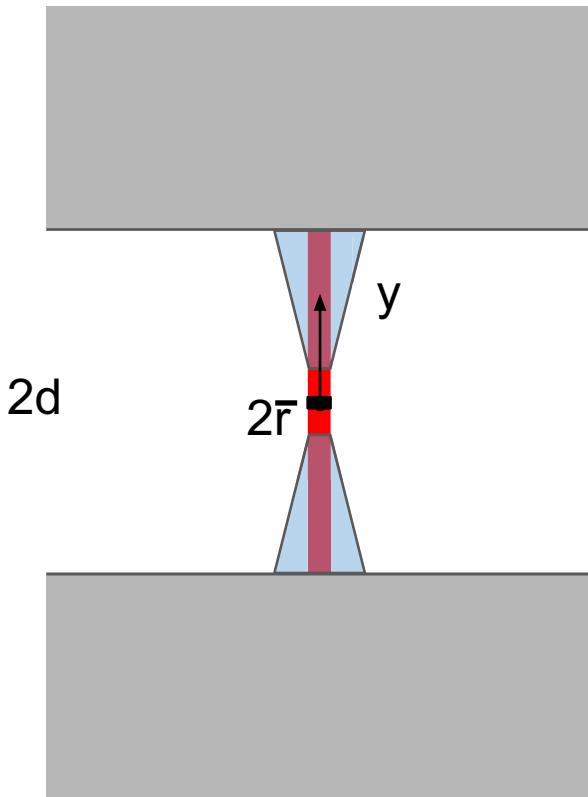


Fig. 12 Junction wires. Top view of wires connecting the Josephson junction to capacitor pads, with each wire of length d . A straight wire of width $2r$ is drawn in red, and a tapered wire in blue.

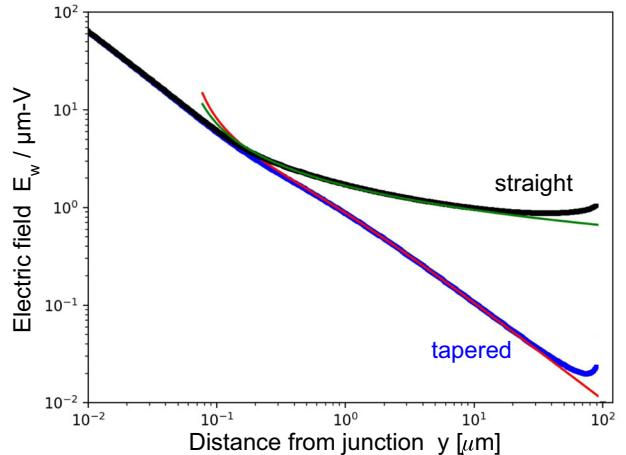


Fig. 13 Electric field of cylindrical wire. Plot of the surface electric field for a cylindrical wire for both straight ($S = 0$) and tapered ($S = 0.2$) radius. Numerical solutions (black and blue) match well with the approximation formulas (green and red) of Eq. (69). Parameters are $r = 0.1 \mu\text{m}$ and $d = 100 \mu\text{m}$. The uptick of the field at the end of the wire is expected for an edge field.

of treating these wires as round with radius r and placed end-to-end each with length d , the surface field can be calculated numerically using the potential matrix Eq. (97) for a 2-D geometry with cylindrical symmetry. For a differential voltage V , the surface electric field as a function of distance y from the junction is well described by

$$E_{\text{cw}}(y) = \frac{1}{2} \frac{V}{r \ln(2y/r)}, \quad (69)$$

as shown in Fig. 13. In comparison with Eq. (9), the second term is equivalent to a coax of inner radius r and outer radius $2y$. The first term $1/2$ represents this coax placed in series with a second coax of the same dimensions, which represents the fields emanating from one circular wire, expanding to a distance $2y$, and then converging in to the other circular wire.

This 2-D numerical calculation also allows the radius r to change with distance y . Modeling a linear taper with $r = Sy$, the electric field is found to be well described by Eq. (69) with r replaced by $r(y)$, as long as the taper is not too large $S < 0.4$; larger slopes are found not to reduce the electric field significantly. Figure 13 shows numerical results for both a straight and tapered cylindrical wire, with good agreement to the approximation formula Eq. (69).

A solution for a flat wire can be obtained by assuming the wire has the x -dependence of the electric field as given in Eq. (16), but with an overall dependence of E_{fw} with y that is determined numerically. Equation (100) in the appendix shows how to solve this problem with a potential matrix. Numerical solutions for both straight and tapered flat wires show that a good fitting function is

$$E_{\text{fw}}(y) = \frac{1}{2} \frac{V}{r \ln(4y/r)}, \quad (70)$$

which has the form of E_f in Eq. (15) but with $2R$ replaced by $4y$. It is again valid for small slope $S < 0.4$. The factor of 4 in the logarithm can be understood as a factor of 2 from the coax to the wire geometry, and another factor of 2 from the circular to flat coax formula in Eqs. (9)–(15).

The metal surface energy for a straight wire of constant width can thus be found by integrating this surface field, which is equivalent to integrating one-fourth of the line energy Eq. (25)

over the wire length

$$U_{sw}^m = 2 \int_{2\bar{r}}^d \left[\frac{1}{4} U_f^m(R=2y)/\ell \right] dy \quad (71)$$

$$= 2\epsilon V^2 \int_{2\bar{r}}^d \frac{\ln(4\bar{r}/t) + c_m}{4\bar{r}\ln^2(4y/\bar{r})} dy \quad (72)$$

$$\simeq \frac{\epsilon V^2}{2} \frac{\ln(4\bar{r}/t) + c_m}{\ln^2(d/\bar{r})} \frac{d}{\bar{r}}, \quad (73)$$

where the factor of 2 before the integral accounts for both junction wires. The last formula was fit to numerical integration. Because of the d/\bar{r} factor, this surface energy can be large, so a more optimal solution is to taper the wire as explained below.

Similarly from Eq. (29), the surface energy of the substrate for a straight wire of constant width is

$$U_{sw}^s = 2 \int_{2\bar{r}}^d \left[\frac{1}{4} U_f^s(R=2y)/\ell \right] dy \quad (74)$$

$$\simeq \frac{\epsilon V^2}{4} \frac{\ln(4\bar{r}/t) + c_s}{\ln^2(d/\bar{r})} \frac{d}{\bar{r}}, \quad (75)$$

The participation ratios for straight wires are

$$p_{MA}^{sw} = \frac{1}{\epsilon_{MA}} \frac{t_{MA} d}{L \bar{r}} p_M^{sw}, \quad (76)$$

$$p_{MS}^{sw} = \frac{\epsilon_s^2}{\epsilon_{MS}} \frac{t_{MS} d}{L \bar{r}} p_M^{sw}, \quad (77)$$

$$p_{SA}^{sw} = \epsilon_{SA} \frac{t_{SA} d}{L \bar{r}} p_S^{sw}, \quad (78)$$

where multiplicative factors are given by

$$p_M^{sw} = \frac{1}{2} \frac{\ln(4\bar{r}/t) + c_m}{\ln^2(d/\bar{r})}, \quad (79)$$

$$p_S^{sw} = \frac{1}{2} \frac{\ln(4\bar{r}/t) + c_s}{\ln^2(d/\bar{r})}. \quad (80)$$

As found previously, the equations differ only in the relative dielectric constants and the corner constant.

The capacitance of the straight junction wires is found from numerical simulation

$$C_{sw} \simeq 4.1 [(\epsilon_s + 1)/2] \epsilon_0 d / \ln(d/\bar{r}). \quad (81)$$

Tapered junction wires

The large d/\bar{r} ratio in the above participation ratios contributes to a large surface energy, since the small width of the wires produce large electric fields at its surface. As surface loss decreases with increasing size, it is natural to increase the width of the wire to lower loss. A solution to minimize surface energy is to taper the wire, increasing the wire width with increasing distance y from the junction as shown in Fig. 12. The contribution to the line energy, the surface energy per line length dy , is the integrand of Eq. (72), where \bar{r} is now a function of y . The integrand is minimized at distances $y/t = (10, 100, 1000)$ for a half-width $\bar{r}/y = (0.363, 0.402, 0.425)$, respectively.

An effective solution is to taper the wire according to $\bar{r}(y) = \max(\bar{r}_0, (y - 5t)S)$ with the taper starting at $y = 5t$, optimizing the slope S for lowest energy. Numerical integration of the line energy gives the metal surface energy for a tapered wire that is fit by

$$U_{tw}^m \simeq 0.38 \epsilon V^2 \frac{\ln(d/\bar{r}_0)}{S} \frac{\ln(4Sd/t) + c_m}{\ln^2(4/S)}, \quad (82)$$

Although this has a minimum energy at slope $S = 0.45$, it is a broad minimum increasing by 2% at $S = 0.28$ and only 10% at

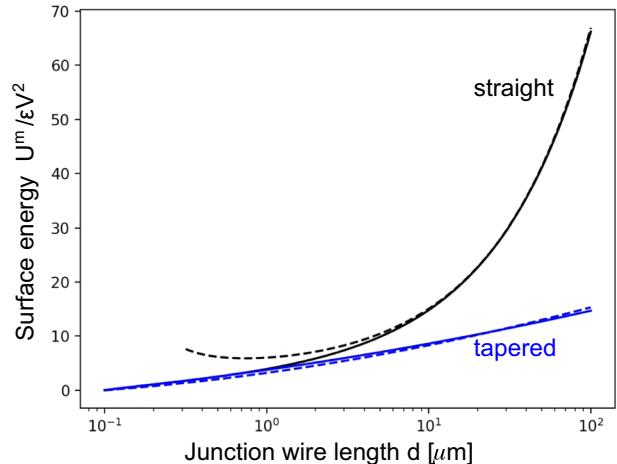


Fig. 14 Junction wire surface energy. Metal surface energy (and loss) of the junction wire for straight (black) and tapered (blue) designs versus wire length per side d , obtained from the integral of Eq. (72). Dashed lines are approximate formulas from Eqs. (73) and (82). The tapered wire shows significantly lower energy for wire lengths $d \gtrsim 10 \mu\text{m}$. At large distances the straight and tapered energy scale with d approximately linearly and logarithmically, respectively. Parameters are $t = \bar{r}_0 = 0.1 \mu\text{m}$ and $S = 0.4$.

$S = 0.16$. Note that this formula is similar to Eq. (73) for a constant width wire, except for the logarithm dependence on d .

Similarly, the substrate surface energy for a tapered wire is fit by

$$U_{tw}^s \simeq 0.15 \epsilon V^2 \frac{\ln(d/\bar{r}_0)}{S} \frac{\ln(4Sd/t) + c_s}{\ln^2(4/S)}. \quad (83)$$

The metal surface loss for the junction wires is plotted in Fig. 14 for the straight and tapered cases, obtained by numerical integration of Eq. (72). At small distances $d \lesssim 5 \mu\text{m}$, the two results are similar, but at large distances the logarithmic scaling makes the tapered loss significantly lower. It is standard practice to increase the overall size of the qubit capacitor to lower its loss. When using a large d , it is thus increasing important to optimally design the junction wires with a taper.

The formulas for the participation ratios for a tapered wire are

$$p_{MA}^{tw} = \frac{1}{\epsilon_{MA}} \frac{t_{MA} \ln(d/\bar{r}_0)}{L} p_M^{tw}, \quad (84)$$

$$p_{MS}^{tw} = \frac{\epsilon_s^2}{\epsilon_{MS}} \frac{t_{MS} \ln(d/\bar{r}_0)}{L} p_M^{tw}, \quad (85)$$

$$p_{SA}^{tw} = \epsilon_{SA} \frac{t_{SA} \ln(d/\bar{r}_0)}{L} p_S^{tw}, \quad (86)$$

with multiplicative factors

$$p_M^{tw} = 0.38 \frac{\ln(4Sd/t) + c_m}{\ln^2(4/S)}, \quad (87)$$

$$p_S^{tw} = 0.30 \frac{\ln(4Sd/t) + c_s}{\ln^2(4/S)}. \quad (88)$$

It is recommended using a continuous taper as described above, not a stepped taper as in previous designs, since the continuous taper is optimal at every distance from the junction x ; the sharp corners of the steps will produce larger electric fields and increase the surface energy. It is not reliable to accurately compare the surface loss of stepped versus tapered wiring since numerical solutions do not have meshing dense enough, which is difficult for 2D simulations and especially problematic for 3D.

Table 1. Check data.

Loss $\times 10^6$	MA	MS	SA
Ref. ⁴	0.10	6.13	4.02
This work	0.060	5.93	3.57
Participation ratio (%)	MA	MS	SA
Ref. ¹⁰ ($d_t = 0.28 \mu\text{m}$)	0.017	0.297	0.156
This work ($d_t = 0$)	0.0012	0.139	0.027
Ref. ⁵ ($d_t = 0.04 \mu\text{m}$)	0.01	0.31	0.17
This work ($d_t = 0$)	0.003	0.414	0.086

Comparison of prior numerical results from finite element analysis with formulas from this paper. The first example shows good agreement for $(a, b, t) = (2.5, 4.5, 0.1) \mu\text{m}$ and surface parameters $(\epsilon_s, \epsilon_{MA}, \epsilon_{MS}, \epsilon_{SA}) = (10, 10, 10, 10)$, thickness 3 nm and loss tangent 0.002. The second example does not agree well and uses $(a, b, t) = (3, 6, 0.25) \mu\text{m}$ and surface parameters $(\epsilon_s, \epsilon_{MA}, \epsilon_{MS}, \epsilon_{SA}) = (11.7, 11.4, 10, 4)$ and thickness 2 nm, but different trench depths d_t . The third example is for C13 and uses $(a, b, t) = (1.35, 3.45, 0.04) \mu\text{m}$ and surface parameters $(\epsilon_s, \epsilon_{MA}, \epsilon_{MS}, \epsilon_{SA}) = (11.7, 10, 7.6, 3.9)$ and thicknesses $(t_{MA}, t_{MS} \text{ and } t_{SA}) = (3, 2, 3) \text{ nm}$.

The capacitance of the tapered junction wires is found from numerical simulation

$$C_{tw} \simeq 3.5 [(\epsilon_s + 1)/2] \epsilon_0 \sqrt{S} d. \quad (89)$$

Comparisons and transmon devices

These formulas agree well with a prior numerical simulation, as detailed in Table 1. The first example shows good agreement with numerical results from Ref.⁴. Note the only difference in the MS and SA formulas are from the corner constants c_m and c_s . The second example does not agree well with the MS geometry of Ref.¹⁰, although the results here are for a flat substrate with no trenching $d_t = 0$. It is unexpected that the prior numerical results with trenching gives a higher participation ratio for *all* surfaces. This table suggests that numerical calculations may give participation ratios with errors as high as a factor of 3–10.

Surface loss closely scales as the inverse of the system size, as described previously in Ref.⁴. However, the calculation for the participation ratio from the junction wires has the opposite effect, as its participation increases with length. Thus there is a crossover in distance d where the surface loss of the wire goes from relatively unimportant to dominant. Formulas for predicting this crossover is an important result of this work.

Table 2 shows the participation ratios for the 3 interfaces and 5 qubit capacitance types, for an example geometry of size scale of $\sim 100 \mu\text{m}$ that is appropriate for current devices. Here a constant thickness 2 nm of the surface oxides is assumed. The ribbon has the same participation as the coplanar geometry, as expected. Of course, predictions depend on actual device parameters, which can be readily made with these formulas.

For the qubit capacitance, the metal-substrate (MS) interface dominates the surface participation. For the ribbon design, the substrate-air (SA) is about 5 times smaller due to the dielectric factors, half the surface, and a lower corner constant c_s . However, the wire loss is not much smaller and clearly indicates that for present designs this contribution should be carefully considered. Importantly, the tapering of the wire will produce a significant improvement in qubit performance, about a factor of 3.

When qubit designs use multiple chips that are bump-bonded together, a parallel plate capacitance is often formed between the qubit chip and ground. Table 2 shows that the participation ratio of this structure needs to be considered even for a plate separation of $s = 5 \mu\text{m}$, especially since the thickness of the other surfaces are likely less than 3 nm.

Table 2. Participation ratios for various qubit structures.

Interface	Eqs.	MA	MS	SA
Parallel plate	(8)	8.16e-5		
Ribbon	(49)–(51)	1.04e-6	1.42e-4	2.74e-5
Coplanar	(57)–(59)	1.04e-6	1.42e-4	2.74e-5
Straight wires	(76)–(80)	7.47e-7	1.02e-4	1.30e-5
Tapered wires	(84)–(88)	2.35e-7	3.22e-5	4.90e-6

The top three are for the primary qubit capacitance, and the bottom two are for straight and tapered wires that connect to the junction with capacitance $\sim 7 \text{ fF}$. For comparison purpose, they all use a length ℓ such that the total capacitance is 100 fF. Geometry parameters are thickness $t = 0.1 \mu\text{m}$; parallel plate $(s, w, \ell_p) = (5, 100, 1130) \mu\text{m}$; ribbon and coplanar $(a, b, \ell_r, \ell_c) = (50, 100, 1391, 1138) \mu\text{m}$; junction wires $(2d, \bar{r}, \bar{r}_0) = (100, 0.1, 0.1) \mu\text{m}$ and $S = 0.4$. Dielectric parameters are $(\epsilon_s, \epsilon_{MA}, \epsilon_{MS}, \epsilon_{SA}) = (11.7, 9.8, 9.8, 3.8)$. For simplicity, here the oxide thickness is assumed to be $t_{MA} = t_{MS} = t_{SA} = 2 \text{ nm}$; results can be simply scaled with expected thickness. Total loss can be estimated by multiplying the surface loss tangents¹⁰; typical values for amorphous insulators are 0.005¹⁴.

Although the formulas predict surface energy will decrease slightly with taper slopes greater than 0.4, doing so is not recommended since numerical simulations show that electric fields do not decrease in this range. Besides, the surface energy only slightly decreases above a slope of 0.2.

An interesting question is how much more surface loss is there for thin films, arising from the large fields at the edges. It is possible to compare surface energy for a round coax and flat coax of the same width using Eqs. (12) and (25), which shows that the ratio of the metal surface energy is

$$\frac{U_f^m}{U_c^m} \simeq \frac{\ln(4\bar{r}/t) + c_m}{\pi} \simeq 4.0 \quad (90)$$

for $\bar{r} = 50 \mu\text{m}$ and $t = 0.1 \mu\text{m}$, typical dimensions considered here. Although the metal-film edges produce more loss, the increase is still acceptable. Note that the logarithm factor is 7.6, so that about 1/3 of the surface energy comes from the corners within $t/2$ of the edges.

The MA and MS participation formulas in Eqs. (3) and (4) use surface energies $U/2$ for the two sides of the film, which are then multiplied by dielectric constant factors. However, since the metal film usually sits on top of the substrate, this splitting of surface energy should change somewhat. One expects the air side of the surface energy to include both sides of the top corner and the outside of the bottom corner, while the substrate side only includes the film edge of the bottom corner. Since these two sides of the corner contributes similarly, one expects the constant factor added to the logarithm to be about $1.5 c_m$ for the air side and $0.5 c_m$ for the substrate side. For example, this modification changes the MA prediction of Table 1 from 0.060 to 0.077, closer to the numerical result 0.010.

Since the MS interface clearly dominates in the participation ratio, there has been effort to minimize this oxide layer by surface treating the silicon wafer before depositing the metal film^{12,13}. The MS thickness and loss tangent are thus parameters that should be measured carefully to optimize a design. The qubit capacitor is much larger size than the junction and its wires are often made in a separate step patterned with optical lithography, while the junction and wire is patterned with electron-beam lithography. If the surface treatment is easier or even possible with the optical lithography step, it is then recommended that the taper is brought down to within 1 μm or so of the junction to minimize its loss. In this case the data in Fig. 14 would be used to estimate the loss from both sections of wire; because of the logarithmic

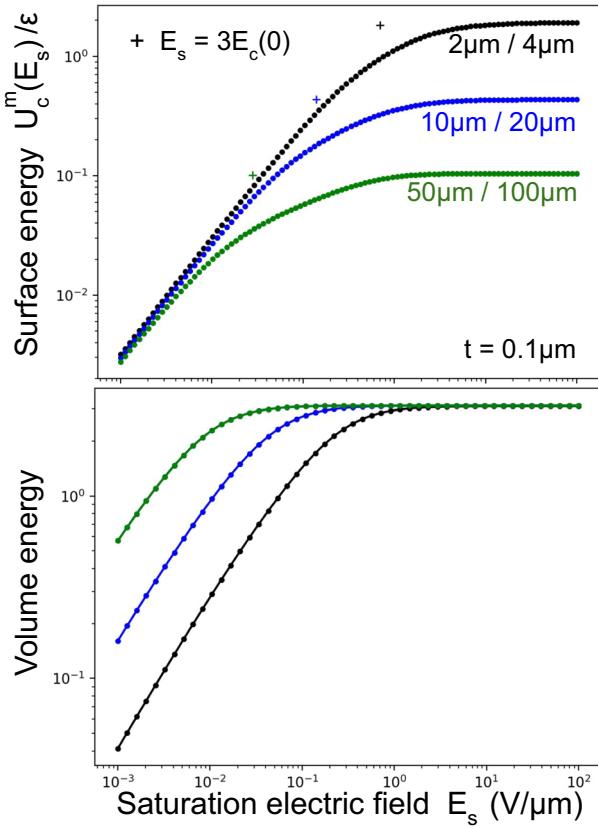


Fig. 15 Saturation loss of a coplanar resonator. Top panel: Plot of surface energy versus saturation electric field E_s , using surface loss scaled for saturation according to Eq. (91). The single-ended coplanar resonators have voltage $V = 1$ Volt and parameters $a = (2, 10, 50) \mu\text{m}$, $b = 2a$ and $t = 0.1 \mu\text{m}$. In the low power limit (high saturation E_s), the loss is inversely proportional to $1/a$, whereas at high power the curves merge together. The plus symbol (+) is the characteristic crossover point, given here by the single-ended prediction of the surface energy Eq. (55) and $3E_c(0)$, where $E_c(0)$ is the center $x = 0$ electric field of Eq. (54). Bottom panel: Volume energy versus saturation field for the same geometric parameters and colors. The volume energy is $\int dx dy |E(x, y)|^2 / \sqrt{1 + |E(x, y)|^2 / E_s^2}$, where $E(x, y)$ is the conformal mapping solution. At low fields the volume energy is equivalent to the capacitance per unit length for all curves, as expected. At left, the characteristic saturation field scales inversely with metal dimension.

dependence, there would still be some contribution from even the short junction section.

Two-level states

Surface loss typically comes from two-level states (TLS)¹⁴, which saturate and produce less loss at high excitation fields. Using the numerically computed surface fields, the dependence on power can be found by scaling the reduction in loss from the local electric field E with

$$E^2 \rightarrow E^2 / \sqrt{1 + E^2 / E_s^2} \quad (91)$$

$$= E E_s \text{ for } E \gg E_s, \quad (92)$$

where the saturation electric field E_s depends on microscopic parameters of the TLS¹⁴.

Since saturation measurements are typically made with coplanar resonators, numerical integration of the surface loss is shown in Fig. 15 for three values of a , each with the gap equal to the inner metal width $b = 2a$. As expected, for large saturation

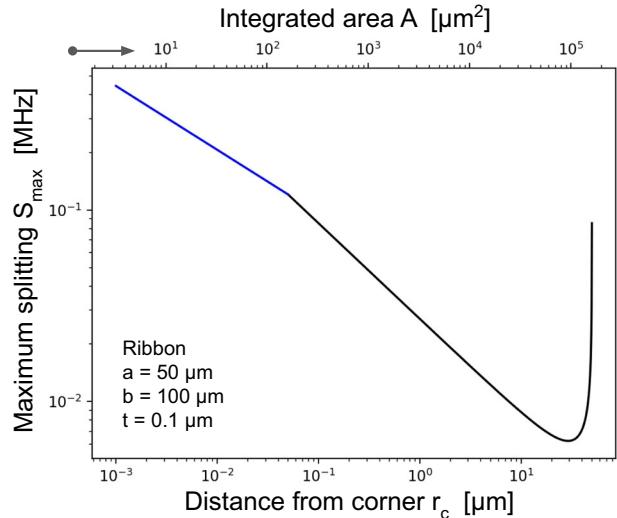


Fig. 16 TLS for ribbon capacitor. Plot of maximum splitting S_{\max} versus distance from edge of ribbon capacitor r_c . Black is ribbon solution of ϵ_s/ϵ_{MS} multiplied by Eq. (35) ($\sim r_c^{-1/2}$), and blue is edge scaling Eq. (20) ($\sim r_c^{-1/3}$). The integrated area $A = 1.5(2\ell r_c)$ is shown on the top x-axis for $\ell = 1.4 \text{ mm}$, showing that the effective areas are typically much greater than $1 \mu\text{m}^2$ (arrow). Thus TLS at the metal edges are statistically observable. The upturn at $r_c = 50 \mu\text{m}$ is from the large fields at the outside metal edge.

fields (loss at low power) the largest resonator gives lowest loss. At large fields, the loss of all three resonators converges. This behavior can be understood using dimensional analysis: scaling all the lengths by D decrease the electric field by $E \sim 1/D$, but increases the surface integration by D . For loss at low power, the integral scales as $E^2 D \sim 1/D$. But when saturated, $EE_s D \sim E_s$ gives constant scaling. Figure 15 also shows volume saturation, for example coming from TLS in the substrate.

The analysis so far has treated the dissipation continuously. However, surface loss comes from a bath of two-level states, with individual states that are spectroscopically observable for small-area devices¹⁴. Simple models predict both the magnitude and the density of TLS, so its spectrum can be extremely useful for identifying the physical location of the loss.

The dipole moment of the TLS couples to the electric field of the 0 to 1 qubit transition. This produces a qubit splitting with random frequency and splitting size, but with a maximum splitting size given by Eq. (3) of Ref. 14

$$S_{\max} = 2(d_{TLS}/x_j) \sqrt{E_{10} e^2 / 2C}, \quad (93)$$

where d_{TLS}/x_j is the relative size of the dipole to the dielectric thickness, E_{10} is the qubit energy, and $e^2/2C$ is the qubit charging energy. Note that S_{\max} is proportional to the qubit electric field and inversely proportional to the square-root of the qubit capacitance. For a junction capacitor with parallel-plate separation 2 nm and a qubit capacitance 2 pF, a value $S_{\max} = 74 \text{ MHz}$ was measured.

For a transmon qubit with $C = 0.1 \text{ pF}$, the above scaling gives

$$S_{\max} = (330 \text{ MHz} \cdot 2 \text{ nm}) E/V, \quad (94)$$

where E/V has a dimension of inverse distance and has been computed here for the various surface electric fields. Since two-level-states tend to have universal behavior, especially if one considers amorphous oxides, this formula is useful for estimating S_{\max} from other surfaces.

For the MS interface of a ribbon capacitor, Fig. 16 shows a plot of S_{\max} versus the distance from the inner corner r_c , which includes edge corrections at a distance less than the half-thickness $t/2$. The

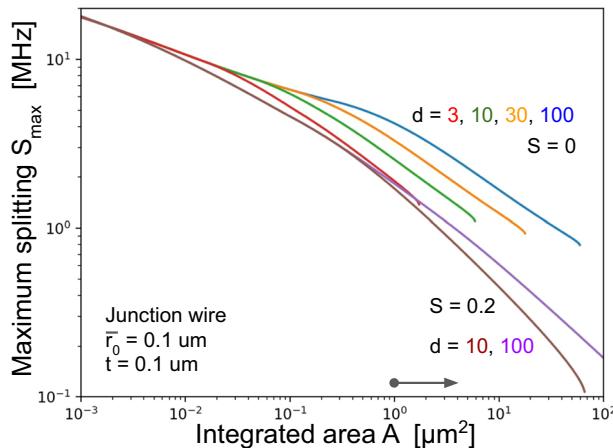


Fig. 17 TLS for junction wire. Plot of S_{\max} versus integrated area for untapered ($S = 0$) and tapered ($S = 0.2$) wires. The electric fields are obtained from Eqs. (16) and (70), and numerically breaking up the wire into small area sections. The tapered wire shows lower maximum splitting, consistent with the continuum results. For the untapered wire, the observable areas $A > 1 \mu\text{m}^2$ (arrow) has S_{\max} in the 1–4 MHz range, whereas for tapered it is below 1.5 MHz. Note that the dominant contribution comes from wire surfaces at a distance greater than about 10 μm .

size of the largest splittings are in the few hundred kilohertz range.

The number of splittings is proportional to the capacitor volume. Figure 2 of Ref. ¹⁴ shows that the size of the splittings have a log-normal distribution, so that the largest splittings are between $S_{\max}/3$ and S_{\max} and have a density $0.5/\mu\text{m}^2\text{GHz}$. The expected TLS density of the ribbon capacitor can be estimated by the effective integrated area $A(S)$, obtained by multiplying r_c by twice the length of the ribbon 2.8 mm and a factor 3/2 to account for the thicker 3 nm thick surface oxide. Since the observed splittings are dominated by those close to S_{\max} , the splitting density ρ_S between splittings S_1 and S_2 is thus approximately given by

$$\rho_S \simeq (0.5/\mu\text{m}^2\text{GHz})[A(S_2) - A(S_1)]. \quad (95)$$

If one assumes the qubit splitting measurements spans a 2 GHz frequency range, then the first observable splitting should occur on average for an integrated area $A = 1 \mu\text{m}^2$. As shown in Fig. 16, TLS should be statistically observable even within a few nanometers from the metal edge. The largest splittings at 3 nm should have size 300 kHz, with an average spacing of about one per 200 MHz in the qubit frequency.

For a parallel plate capacitor, the effective distance for the electric field is the separation multiplied by $\epsilon_{\text{MA}} = 9.8$. For the example of Table 2, this gives 49 μm . One finds a splitting size of 13 kHz, and an effective area of 1.5 times the capacitor area.

Junction wire results are shown in Fig. 17 for the untapered and tapered cases. These plots were obtained by numerically breaking up the wire into about 100k sections, then computing S_{\max} and the differential area dA for each section. The curve is obtained by sorting S_{\max} from large to small, and then cumulative summing over the corresponding dA to obtain the integrated area A . The tapered case shows lower splittings S_{\max} , consistent with the continuum theory. The TLS become statistically observable for $A > 1 \mu\text{m}^2$, which predicts splittings in the several MHz range. The dependence on d shows that the dominant contribution to the TLS are for distances greater than about 10 μm ; shorter distances are unimportant because they have small areas. The dominance of an intermediate length scale is perhaps a surprising result, and shows why detailed theory is needed to optimize the wire design.

This result suggests that undercutting the junction wires into the substrate can be an effective solution to decrease the contribution of the metal-substrate interface. Since there is little contribution at small distances, it is not essential to undercut around the junction, which should improve the reliability of the fabrication and the stability of the junctions.

Summary

Calculation of participation ratios and surface loss is challenging because of the divergence of the electric fields at metal edges. Previously, these fields were solved in the infinitely thin limit using solutions from conformal mapping. Here, the solutions were extended to the useful limit where the thin surface oxide (few nm) is less than the metal film thickness (0.1 μm), and less than the typical film size (100 μm). The finite thickness condition was solved via a calculation that matched the conformal fields to edge fields, then checked and refined with numerical simulation. Going forward, these formulas are also useful when checking numerical simulations for systematic errors due to meshing.

Formulas are given for common capacitor structures. By separating out the geometry of actual designs, participation ratios can be calculated accurately and then used to optimize the design. This is an important check on numerical calculations since misleading results can come from finite meshing when structures range in size from nanometers to millimeters.

For junction wires, a solution for the capacitance and surface loss was obtained using well-formed models, approximations and numerics, which should give accurate and reliable formulas. A tapered junction wire was shown to have superior performance compared to straight wires when the wire length is longer than about $\sim 10 \mu\text{m}$. This design feature is important for the latest generation of devices that use large capacitor size to lower surface loss. A further design improvement for the taper was suggested.

These electric field solutions enable a prediction of the TLS spectrum, which could be invaluable to identify where the TLS comes from in the qubit design.

Finally, it is hoped that these results will encourage researchers to precisely test surface loss theory, and measure in additional experiments the various surface loss parameters. By doing so, this should speed the optimization and development of long coherence time qubits.

METHODS

Numerical calculation of surface electric fields

For thin films suitable for superconducting qubits, it is useful to numerically calculate the electric fields, for example for a thin film of finite thickness. Fortunately, realistic transmon designs are well approximated by simple geometries with fields that can be well described using simple fitting functions, so that they can be physically understood and optimized. Two-dimensional geometries are particularly amenable to efficient numerical solutions and thus their method of solution will be described here first. For simplicity, the calculations here will assume a constant dielectric constant ϵ . Corrections due to the substrate and vacuum are included in the main text.

Figures 7, 9 and 10 show geometries to be considered here. The first is 2-dimensional, with solutions given per unit length in the third dimension, with results typically scaled with length ℓ . The second solution uses cylindrical symmetry to turn a 3-dimensional problem to 1-D. The last uses an approximation to the edge fields so that a thin film wire can be similarly calculated in 1-D.

Numerical solutions can be obtained through inverting a matrix. For a 2-D geometry with translational invariance in the z direction, the problem is first broken into a vector of points in the x - y plane that have line charge \vec{q} . The voltage \vec{V} can be solved with the matrix equation $\vec{V} = \vec{M}\vec{q}$, where the potential matrix \vec{M} has elements

$$M_{ij} = \frac{1}{2\pi\epsilon} \ln(1/\rho_{ij}), \quad (96)$$

where ρ_{ij} is the distance between point i and j . For metal electrodes the voltage is set instead, so the charge can be obtained using $\bar{q} = \bar{M}^{-1} \bar{V}$, where the inverse matrix \bar{M}^{-1} can be thought of as a capacitance matrix. The time to solution grows as the cube of the number of points, which can be solved quickly for size 1k - 10k.

For a 3-D geometry with cylindrical symmetry, the potential matrix can be solved for a circular ring of total charge q , giving a potential matrix with elements

$$M_{ij} = \frac{1}{2\pi^2\epsilon} \frac{\text{ellipk}(-4r_i r_j / \rho_{ij}^2)}{\rho_{ij}}, \quad (97)$$

$$= \frac{1}{4\pi\epsilon\rho_{ij}} \text{ for } \rho_{ij} \gg r_i r_j, \quad (98)$$

where ρ_{ij} is the distance between points in the r-z plane, and r_i and r_j are the radial components. The Python `ellipk(m)` function is equivalent to `K(k)` but with $m = k^2$, and allows negative m arguments.

For a similar 3-D geometry of a flat coax, the potential matrix for the inner conductor is

$$M_{ij} = \int_{-\bar{r}_j}^{\bar{r}_j} \frac{1/\pi}{\sqrt{\bar{r}_j^2 - x^2}} \frac{1/4\pi\epsilon}{\sqrt{x^2 + y_{ij}^2}} dx \quad (99)$$

$$= \frac{1}{2\pi^2\epsilon} \frac{\text{ellipk}(-\bar{r}_j^2 / y_{ij}^2)}{y_{ij}}, \quad (100)$$

$$= \frac{1}{4\pi\epsilon y_{ij}} \text{ for } y_{ij} \gg \bar{r}_j, \quad (101)$$

where y_{ij} is the distance between points i and j on the centerline of the wire. In comparison with the matrix for the cylinder geometry Eq. (97), the difference is the absence of the factor of 4 in the ellip argument.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

CODE AVAILABILITY

The Python code that support the findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

J.M. contributed solely to this work.

COMPETING INTERESTS

The author declares no competing interests.

ADDITIONAL INFORMATION

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