Proceeding Paper

SBND Trigger System: Status and MTC/A Configuration

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Abstract: We present a brief description of the Short-Baseline Near Detector (SBND) hardware trigger system. The SBND experiment is a liquid argon neutrino detector that sits on the central axis of the Booster Neutrino Beam (BNB), located at Fermilab. The detector is currently being assembled and is expected to start operating in 2023. Neutrinos delivered by the BNB will interact with liquid argon inside the SBND, producing charge and scintillation light that will be collected, respectively, by the charge collection wires and the photon detection system. SBND will record over a million neutrino interaction events per year while simultaneously being exposed to a large flux of cosmic ray interactions. It is imperative to determine which events in the detector are of interest for analysis. This is the work of the SBND trigger system, which receives several prompt inputs, discriminates these inputs and qualifies them to form a trigger decision. In this work, we will focus on the general overview of the trigger system for SBND, and, specifically, we describe the configuration of the Analog Master Trigger Card used in the photon detection trigger.

Keywords: trigger; data acquisition; neutrino detectors

1. Introduction

The Short-Baseline Near Detector, or SBND, consists of two Liquid Argon Time Projection Chambers (LArTPCs) [1] placed in the beamline of the Booster Neutrino Beam (BNB) [2] at Fermilab. In combination with the finalized MicroBooNE [3] and the operating ICARUS [4] LArTPCs, SBND will integrate the upcoming Short-Baseline Neutrino Program, or SBN [5,6]. SBND is currently in the final stage of construction, and it will attempt to start taking data in 2023. The main physics goals of SBN include searches on the eV-scale sterile neutrinos, other beyond standard model scenarios as well as measurements on neutrino-argon cross-sections with world-leading accuracy.

Because of its proximity to the neutrino source (about 110 m), SBND will record over two million neutrino interactions per year. Such high event rates in conjunction with thousands of cosmic ray interactions per second inside the detector require an equally fast and efficient trigger system able to manage a large amount of information.

In this report, we present the capability of the SBND trigger system. The purpose of a trigger system is to select and qualify detector events based on logic operations inside its electronics. The electronics decide to pass or not data to the Data Acquisition (DAQ) System. We will briefly describe the trigger logic of the different electronic subsystems and their connection with timing and DAQ setups.

With the purpose of showing the flexibility of the SBND hardware trigger, we will specifically describe the configuration of the Analog Master Trigger Card (MTC/A). This board monitors the activity of the photo-multiplier tubes inside SBND by discriminating the input signals into three different voltage thresholds. For completeness, we will also show how to properly set these thresholds in MTC/A.

2. Neutrino Detection in SBND LArTPCs

SBND LArTPCs are arranged in a 4 m × 4 m × 5 m box to be confined inside a cryostat and filled with 112 tons of liquid argon. When a neutrino coming from the BNB arrives to the detector, it may weakly interact with the argon nuclei, producing charged particles. These particles ionize the environment during their propagation, creating electron–argon ion pairs. A strong and constant electric field (500 V/cm) drifts the electrons towards the LArTPC anode, where they are collected by planes of wires [7].

In total, there are 11,264 wires distributed in SBND LArTPC anodes. Signals generated by electrons in the wires are then processed and distributed to dedicated readout and trigger systems before being sent to offline storage. We will not cover the LArTPC trigger and readout hardware components in this report. For further information, see Ref. [8].

Aside from electron drift, the remaining argon ions produce scintillation light through the processes of de-excitation and recombination [9]. The photons are detected by a set of 120 photo-multiplier (PMT) tubes and 192 X-ARAPUCAs [10] that compose the SBND photon detection system (PDS). The light emission is faster than charge drift to the anode planes ($\mathcal{O}$ (ns) versus $\mathcal{O}$ (ms)); thus, the signals from the PDS provide a time reference for the particle interactions inside the detector. As a consequence, the use of the PDS reference time improves the timing accuracy for event reconstruction.

Some of the trigger subsystems we have discussed in this report use the inputs from the PDS to characterize the level of activity inside the LArTPC. We will describe them in Sections 3 and 4.

3. The Photon Trigger Board

The Penn or Photon Trigger Board (PTB, shown in Figure 1) intersects all the SBND hardware trigger components. Previously used in DUNE 35-ton prototype [11], PTB is a motherboard that establishes hardware interface with the trigger subsystems, while a field-programmable gate array (FPGA) implements trigger logic and has interface with the timing system. A Linux-based CPU configures the FPGA and communicates with the DAQ software v1_08_02 . Both FPGA and CPU side are part of the MicroZED [12] programmable board (Avnet, Pheonix, AZ, USA).
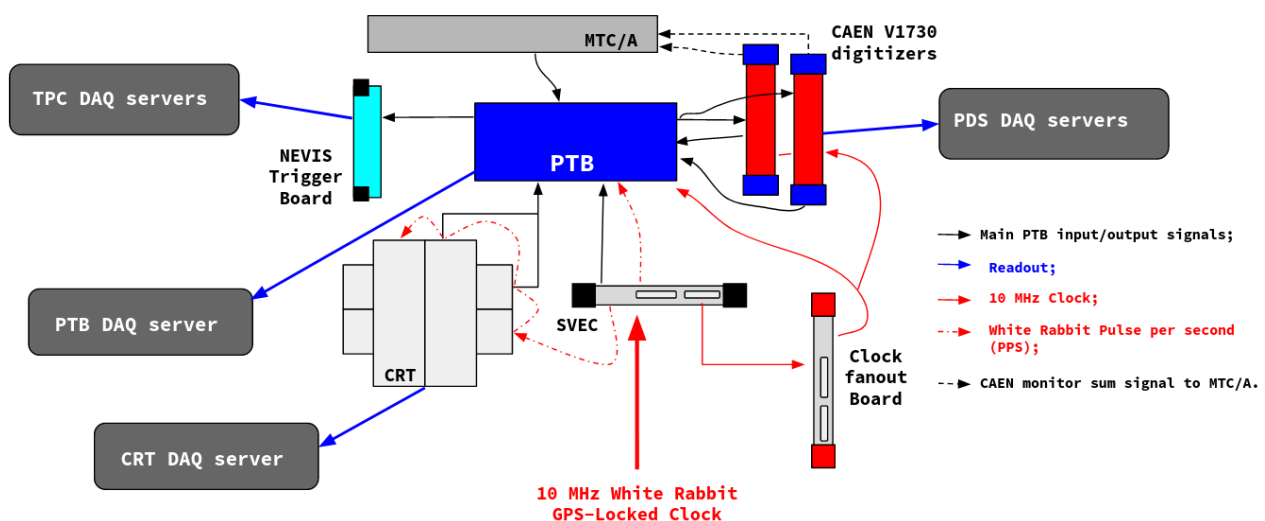

Figure 1. Front view of the Photon Trigger Board (University of Pennsylvania, Philadelphia, PA, USA), showing connectors in the chassis for some electronic subsystems: PDS, timing and LArTPC (NEVIS) trigger board.

The main PTB connections to the electronic subsystems are summarized in Figure 2. We present a short description of them as follows:

- **PDS—CAEN V1730 digitizers:** The signals from the PMTs and some of the X-ARAPUCAS are digitized by ten commercial CAEN V1730s (CAEN S.p.A., Viareggio, Italy), 16 channel modules. For the PMT digitizers, the trigger logic is built by pairs of odd–even channels and are configured as AND, OR, ONLY A and ONLY B. It is possible to define the so-called "majority level" by declaring the number of PMT pairs above a pre-set threshold in a specific time window. If the trigger logic is satisfied, CAEN V1730 sends an output signal to the PTB. Conversely, PTB serves as an external trigger to start the digitizers' readout. We will discuss PTB trigger logic in Section 3.

- **PDS—MTC/A:** CAEN V1730 modules also have an analog monitor output whose signals are proportional to the number of PMT pairs that are above a pre-set threshold. Such PMT multiplicity signals are inputs to the MTC/A. The MTC/A sums the signals from multiple V1730 digitizers and compares them to three individually programmed thresholds: LOW, MEDIUM and HIGH. An over-threshold signal from any of these discriminators propagates a trigger signal from MTC/A to the PTB. We will show in Section 4 how to program the MTC/A thresholds using PTB CPU side.
- **Cosmic Ray Tagger (CRT):** The Cosmic Ray Tagger, or CRT, system will entirely surround the SBND cryostat. It is responsible to measure crossing muons from cosmic sources. Each CRT basic module is formed by scintillation strips placed side by side and covered with an aluminum case. When a cosmic muon interacts with this module, scintillation light is produced and propagates along the CRT module. The signal is collected by Silicon PMTs and processed by electronics placed on the edge of each module. For further details, see Ref. [13]. The CRT panels are displayed in a vertical–horizontal overlaid configuration around SBND cryostat. In this way, the trigger logic for the CRT modules is defined by the coincidence of cosmic muon hits between two overlaid layers. When this logic is satisfied, the PTB receives a trigger pulse.
- **NEVIS Trigger Board:** The LArTPC-dedicated trigger system mentioned in Section 2 is denominated NEVIS trigger board. The PTB communicates with the NEVIS trigger board by sending pulses from PDS- and CRT-related triggers.
- **Timing and Accelerator Complex signals:** White Rabbit (WR) timing system [14] provides 10 MHz GPS-Locked Clock and pulse per second (PPS) to SBND trigger system. These signals are distributed using a WR fine delay and digital input output inside SVEC card as well as a clock-fanout module. The NEVIS trigger board as well as CRT electronics have independent internal clocks. The information from the accelerator complex is also delivered to the subsystems through WR. There are two main types of beam signals: the Booster Extraction Signal, sent when protons are leaving the accelerator ring, and the Resistive Wall Monitor, which signalizes the proton current upstream to the beam target.
- **DAQ:** The Data Acquisition system is responsible for the subsystem readout. DAQ establishes connection to the electronics through the servers. It is in charge to properly set user-defined configurations to the boards for the run, acquires and assembles data fragments and directs them to online monitoring or offline storage.

Figure 2. Summary of SBND Trigger System showing the main connections the Photon Trigger Board has with other trigger subsystems, timing and DAQ. The arrows show the direction of data stream and colors state the purpose of the connection, defined in the bottom right label.

Low- and High-Level Triggers

The PTB uses the inputs from the various trigger subsystems to perform its trigger logic. There are two types of PTB triggers: Low-Level Triggers (LLT), where the logic (coincidence, channel mask, etc.) is made with inputs from the same subsystem, and High-Level Triggers (HLT), where a compound of Low-Level Triggers participate in the trigger decision. When the conditions are satisfied, PTB sends the formed LLT and HLT to the DAQ and, in the case of the HLTs, generates trigger pulses to the other subsystems.

It is important to emphasize the flexibility of the SBND Trigger System, once the PTB LLTs and HLTs can be configured in a wide range of possibilities and their configuration is relatively fast, in the case of testing multiple scenarios during the physics run.

4. The Analog Master Trigger Card Configuration

As described in Section 3, MTC/A monitors the overall PMT activities by discriminating its inputs into "low", "medium" and "high" signals. The configuration of these discriminators occurs using the PTB Linux side. Each threshold value is set by programming a single digital-to-analog converter (DAC). We need to assign a 12 bit value to the DAC that corresponds to a specific voltage in the range $[-5 \text{ V}, 5 \text{ V}]$.

Basically, we follow the steps below, considering the configuration of only one threshold:

1. Use the PTB Linux side to map the MTC/A register addresses into virtual memory addresses. Use these memory pointers to change bit values;
2. For each MTC/A, we have five bits to assign: one for each threshold value, one for clock and one for syncbar;
3. Write "0" for the syncbar bit to enable bit assignment;
4. Set 32 clock cycles by writing to the memory address a sequence of "0" and "1" on the bit designated for clock;
5. After four clock-edge falls (from "1" to "0"), start writing the 12 bit number correspondent to the desired threshold voltage on the bit assigned for the threshold value;
6. After 12 clock-edge falls, set syncbar to "1" to lock more bit assignment.

The above steps are summarized in Figure 3, where 3.9 V was programmed in the "high" threshold.
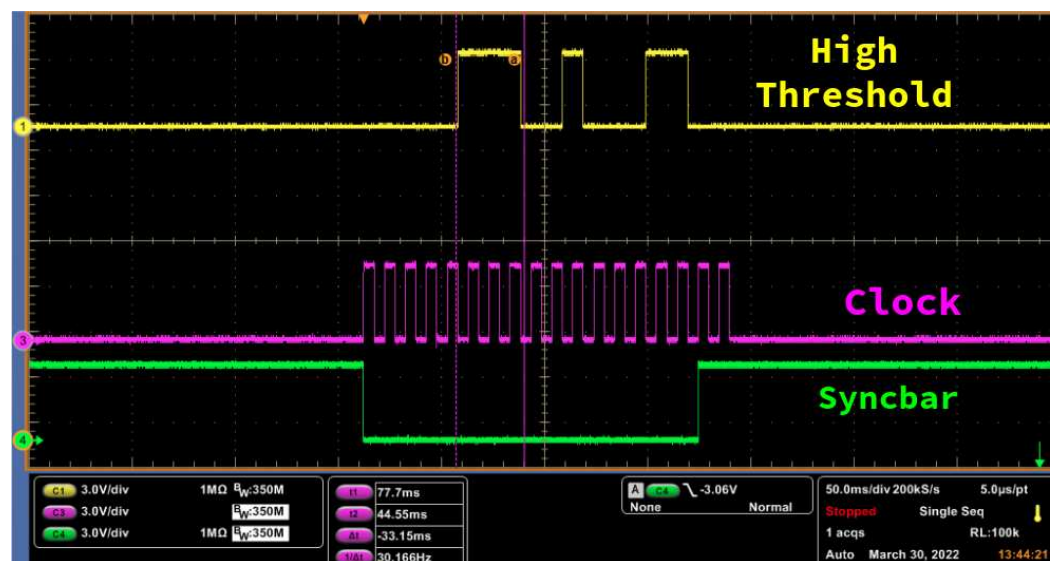
Figure 3. Oscilloscope channels streaming the signals for programming 3.9 V in one single MTC/A threshold: channel 1 (yellow curve) represents the "high" threshold value, channel 3 (magenta curve) is the clock action and channel 4 (green curve) is the reset bar. The oscilloscope cursors "b" and "a" highlight the bit values changing at the clock-edge fall.

5. Summary

The statistical power of SBND enables it, as a single detector or as part of an SBN program, to perform sensitive searches on sterile neutrinos and other beyond standard model scenarios as well as to precisely measure neutrino-argon cross-sections. Attempting to record over two million neutrino events per year, SBND needs an efficient trigger system to select and qualify worthy events for analysis.

We have shown in this report the capability of the SBND trigger system and specially the flexibility of the photon trigger board in communicating with all electronic subsystems and performing a significant variety of trigger logic with these subsystems inputs.

Additionally, we showed that PTB could also be used to configure MTC/A DAC with its CPU side by accessing and writing the bit values on the virtual memory.

Conflicts of Interest: The author declares no conflict of interest.

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