Thesis for the Degree of Master

A Preamplifier-shaper Design for High Density Sensor Readout System

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Abstract

The understanding of the origin of the CP violation is one of the most important subjects in modern particle physics. Belle detector is designed to experimentally measure the CP violation in the B meson system. This detector is now planned to be upgraded to what is called super Belle which is optimized to detect new phenomena that maybe originated from physics beyond the standard model, such as Supersymmetry with increase of the significant luminosity. While measuring the CP violation with asymmetric energy collider, accurate decay point measurement should be performed. Silicon vertex detector (SVD) gives the most accurate location of outgoing particles after the electron positron collision and used as an vertex detector. We are developing a preamplifier-shaper ASIC which can be used as a readout system of SVD. The first prototype was produced in 2006, tested, and immediately showed several serious problems and its initial performance is discussed in detail. A new design of the improved second prototype is completed and ready to be submitted. If the second prototype shows the performance similar level in the simulation result we obtained, our model can be used in super Belle detector and study CP violation with our devices. Theoretical noise calculation and expected performance of the second prototype based on simulations is discussed in detail.

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1.0 Introduction

The main goal of particle physics is to understand basic principle of the nature. Presently, the standard model is well established and it explains the interaction between six Quarks; up, down, strange, charm, bottom, top and six leptons; electron, muon, tau, and neutrinos. The CP violation which represent the violation of particle-antiparticle symmetry is well explained by weak coupling of the six Quarks in standard model [1]. By Kobayashi-Maskawa (KM) theory in standard model [2, 3], many people try to understand the CP violation and expect to explain why the universe we live in consists predominantly of the matter. Although the CP violation was first observed in 1964 in the decays of neutral K mesons, certain decay modes of B mesons are pointed out to have much bigger CP violating asymmetry rate than K meson system [4, 5, 6]. For these purpose, our laboratory joined Belle collaboration in the high energy accelerator research organization, KEK, in Japan to research CP violation on B meson system. In order to observe CP violation in the B meson system, KEKB accelerator accelerates electron and positron with different energy [7, 8]. With this asymmetric energy between electron and positron, the decay vertex of the B meson can be measured. And the decay vertexes of two B mesons are used to calculate the violating asymmetry of certain mode. KEKB accelerator is designed to achieve luminosity up to $10^{34}\text{cm}^{-2}\text{s}^{-1}$ and peak luminosity from experiment was approximately $17.12 \times 10^{33}\text{cm}^{-2}\text{s}^{-1}$. With these accelerator and detector, Belle experiment has verified the Kobayashi-Maskawa (so called KM) theory that explains CP violation and quark mixing in the weak interaction.

Now KEK is preparing a new project named super KEK B factory [9]. This new project is aimed to detect new phenomena such as Super symmetry or extra dimensions with B meson system. To satisfy the experimental requirements, new electron-positron collier for super KEK B are aimed to reach 50 times larger luminosity than present KEK B collider. According to the present schedule for the super KEK B, operation is anticipated to start in the middle of 2012. This situation motivated us to develop a readout amplifier for the silicon vertex detector which is used in super KEK B detector. We first provided a readout hybrid board with the VA chip [10] that is a preamplifier-shaper with serial output capability of 128 channels, to Korean ILC tracker R&D community successfully [11]. After that, we made a first prototype named Korea University Preamplifier Integrated Design (KUPID) v1.0 in 2006 that has in total 24 parallel channels with 9 different parameter types

in design without multiplexers for serial outputs [12]. However, test of KUPID v1.0 shows very bad noise property due to our ignorance in optimization and we discuss its performance in this letter. Therefore, we are starting a new improved version of the KUPID and here we report the expected performance of the new design (KUPID v2.0) which is well optimized for the noise performance. For this purpose, theoretical approach to preamplifier-shaper chain is calculated to get a guide line for a noise optimized design [13, 14, 15, 16, 17]. All the simulation results are obtained with Cadence Virtuoso Spectre Circuit Simulator (Spectre) [18].

1.1 B Meson Physics

To explain the CP violation, first we have to understand the most basic concepts about symmetry or invariance under discrete transformations such as charge conjugation C, parity P, and time reversal T. Table. 1 shows the physical observable in C, P, T transformations.

		C	P	T
coordinate	**r**	**r**	-**r**	**r**
momentum	**p**	**p**	-**p**	-**p**
angular momentum	**J**	**J**	**J**	-**J**
spin	σ	σ	σ	-σ
electric field	**E**	-**E**	-**E**	**E**
magnetic field	**B**	-**B**	**B**	-**B**
particle		antiparticle	particle	particle

Table 1: C, P, T transformation of physical observable.

The CP violation was first observed in the decay of K^0 meson [1]. K^0 meson can decay by weak interaction into two pions or three pions which CP value is 1 and -1 respectively with different decay time. For two pion decay, decay time is approximately 90 ps while 50 ns for three pion decay. If we assume that K^0 and $\bar{K^0}$ are composed of two particles, K_0 and K_1. Then it is possible to define K^0 and $\bar{K^0}$

state with two eigenstates K_0 and K_1.

$$|K^0 >\equiv \frac{|K_0 > +|K_1 >}{\sqrt{2}} \tag{1}$$

$$|K^1 >\equiv \frac{|K_0 > -|K_1 >}{\sqrt{2}} \tag{2}$$

In CP transformation, K_0 and K_1 are defined to be invariant and variant, respectively.

$$CP|K_0 >= +|K_0 > \tag{3}$$

$$CP|K_1 >= -|K_1 > \tag{4}$$

CP invariance should be conserved by K_0 decay into two pions and K_1 decay into three pions as total CP is conserved to 0. It was , however, observed that K_1 decay into two pions with little possibility. And as a result, the physical eigenstate of K^0 can be expressed as

$$|K_S^0 > = |K_0 > +\varepsilon|K_1 > \tag{5}$$

$$|K_L^0 > = |K_0 > +\varepsilon|K_1 > . \tag{6}$$

when $\varepsilon \neq 0$ represents the CP violation.

1.2 CKM Matrix

In KM theory, the mixing between the quark generations are simplified as

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = V \begin{pmatrix} d \\ s \\ b \end{pmatrix} \tag{7}$$

The primed d', s', b' are weak force eigenstates of Quarks and unprimed d, s, b are elements of mass eigenstates vector. The unitary matrix V which is called as CKM matrix describes the transition probability from one Quark to another Quark and expressed as

$$\begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \tag{8}$$

The constraints of unitarity of the CKM matrix on the diagonal terms can be written as

$$\sum_i |V_{ik}|^2 = 1. \tag{9}$$

This relation is called weak universality and implies the sum of all coupling of any of the up-type Quarks to all the down-type Quarks is the same. There is one more unitarity condition for CKM matrix

$$\sum_i V_{ij} V_{ik}^* = 0. \tag{10}$$

In Eq. 10, when j and k are chosen in different Quarks for a each i, this condition forms the sides of a triangle in the complex plane (Fig. 1 shows the case when d Quark for j and b Quark for k). There are six choices of j and k, and hence there are total six different triangles which are called unitary triangle. Unitary triangle for the B meson system, which Belle experiment is measuring, has d Quark for j and b Quark for k. Three angles for this unitary triangle is then defined as shown in Fig. 1.

$$\phi_1 \equiv arg\left(\frac{V_{cd}V_{cb}^*}{V_{td}V_{tb}^*}\right), \tag{11}$$

$$\phi_2 \equiv arg\left(\frac{V_{ud}V_{cb}^*}{V_{td}V_{tb}^*}\right), \tag{12}$$

$$\phi_3 \equiv arg\left(\frac{V_{cd}V_{cb}^*}{V_{ud}V_{ub}^*}\right), \tag{13}$$

The Belle experiment is focused on measuring three angles and three sides of this triangle. When one of the B^0 and $\bar{B}^0$ mesons decay into CP eigenstate and the other state that one can measure meson, the flavor of the CP violating asymmetry is given by

$$\frac{R(B^0 \to f) - R(\bar{B}^0 \to f)}{R(B^0 \to f) + R(\bar{B}^0 \to f)} = sin(2\phi_{CP})sin(\Delta m \Delta t) \tag{14}$$

where Δm and Δt in the equation are the mass difference between B^0 and $\bar{B}^0$, and the difference of proper time for B^0 and $\bar{B}^0$ decays, respectively. And ϕ_{CP} is the phase difference between the $B^0\bar{B}^0$ mixing amplitude and the $B^0 \to f$ decay amplitude. The angle ϕ_{CP} is directly related to the internal angles of the unitary triangle. As KEKB accelerator accelerates electron and positron with different energy, highly accurate measurement of B^0 and $\bar{B}^0$ decay vertex can determined the

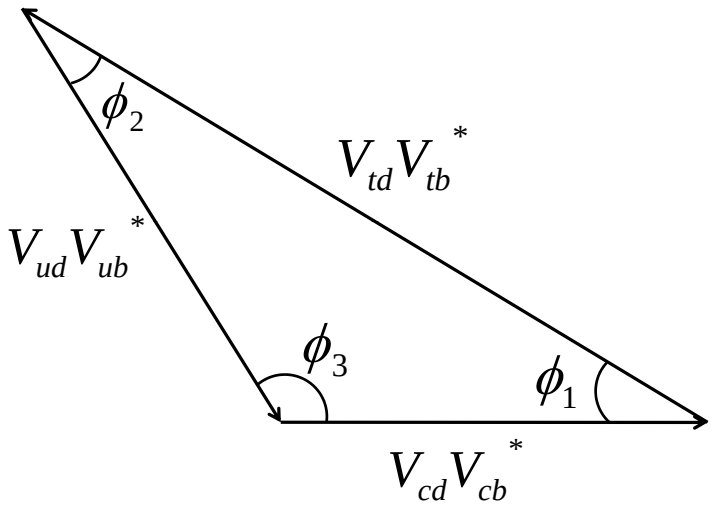

Figure 1: Unitary triangle for B meson system.

difference of proper decay time Δt. This vertex detecting is measured by silicon vertex detector (SVD) which gives the most accurate location of outgoing charged particle. KUPID is designed to amplify and serialize the high density signal from SVD. If our KUPID chip is designed in high performance for SVD readout device, it can be used in strip detector readout system for super KEK B detector.

2.0 Silicon Vertex Detector

Silicon vertex detector (SVD) is the innermost detector of Belle detector which measures the decay point of both B^0 and $\bar{B}^0$. As mentioned in previous section, accurate measurement of difference decay time between B^0 and $\bar{B}^0$ is required to obtain the CP violating asymmetry (equation (14)), SVD has a very good position resolution. In this section, strip detector which is used as a SVD in Belle detector, SVD for Belle detector, and super Belle detector are introduced.

2.1 Silicon Strip Detector

Silicon Strip detector is one of the most fundamental detectors with high position resolution. It is much easier to design and manufacture than pixel detectors. A strip

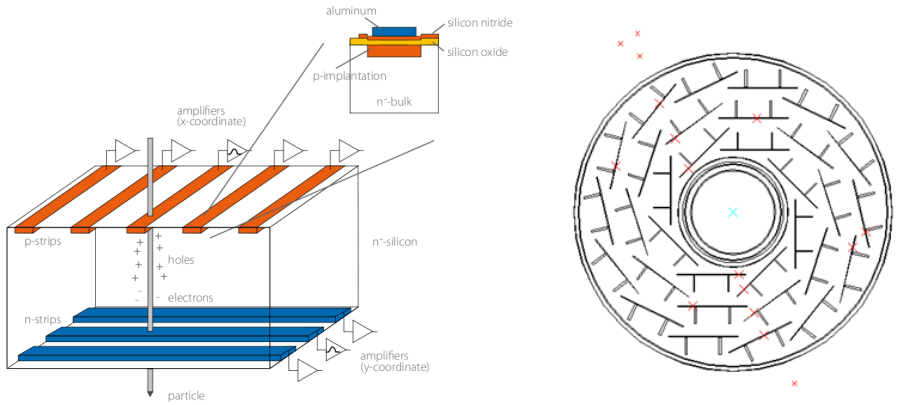

Figure 2: Simple schematic for double-sided silicon vertex detector on the left, while schematic for silicon vertex detector in Belle detector is plot on the right. In Belle detector, three layer double-sided strip detectors are covering the beam pipe.

detector is an arrangement of strip like implants which act like a charge collecting electrodes.

As strip detector is designed to measure one dimensional position, additional crossed strip detector layer is needed to measure two dimensional position. SVD for Belle and super Belle detectors are therefore designed as double-sided strip detector. Basic schematic for a double-sided strip detector is shown in Fig. 2. Each metalized strips are connected to charge sensitive preamplifier-shaper and multiplexer for a signal readout. For achieving high density channel readout, preamplifier-shaper and multiplexer integrated ASIC chip is mostly used as a readout device. Our second prototype KUPID ASIC chip is preamplifier-shaper and two channel multiplexer integrated design for super Belle SVD readout. The schematic for preamplifier-shaper chain is in Fig. 3.

2.2 SVD for Belle Detector

SVD in Belle detector is double sided silicon strip detector which is 300 μm thick. There are three layers and covers 86 % of the total solid angle. The strip detector consists of 1280 sense strips with 25 μm pitch on the π-side and 1280 sense strips with 42 μm pitch on the z-side. Total number of readout channels is 81,920.

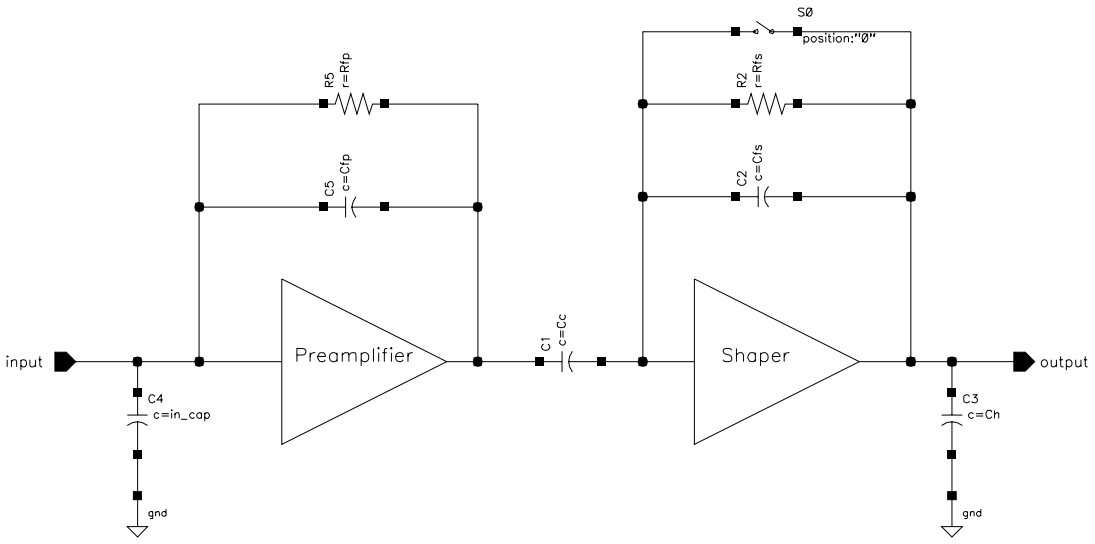

Figure 3: A simplified view of preamplifier-shaper chain design. The first stage on the left is the preamplifier that amplifies charge signals and shaper at the second stage performs the typical *CR-RC* filtering.

2.3 SVD for super Belle Detector

SVD for super Belle is desired to have six layer silicon sensors to achieve higher position resolution than Belle detector. The increased number of layers in SVD are expected to improve the tracking efficiency for low momentum particles and K_S^0 decays. This design is proposed assuming operation at a luminosity of $10^{36}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ while luminosity of KEKB was $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The upgraded strip type sensors and readout systems are needed for this design. Readout chip for super Belle SVD should have short shaping time (approximately 50 ns) to reduce the high occupancy induced by the harsh beam background. Our KUPID chip is designed to optimize the performance in super Belle SVD readout system.

3.0 Theoretical Calculation of Gain and Noise

3.1 Transfer Function of Amplifier

In Fig. 3, our amplifier is symbolized as a triangle which contains many transistors in it. To calculate the gain of amplifier, let us think amplifier (triangle) as shown in Fig. 4. R0 is a resistance of current source of input PMOS transistor and

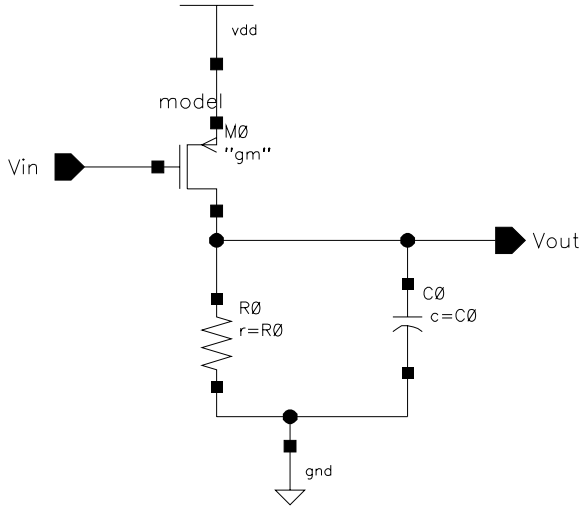

Figure 4: Simple amplifier circuit used for the noise calculation. Resistance of current source is expressed as $R0$ and capacitance at the output node of amplifier is expressed as $C0$ in the schematic. This model can be thought as an simplified inner circuit of Fig. 3's amplifier (triangle).

C0 is a capacitance of preamplifier output node. DC gain of amplifier G_{DC} will be then

$$G_{DC} = \frac{V_{out}}{V_{in}} = \frac{R0 \cdot I_{SD}}{Vdd - V_{SG}}$$

and hence the slope of DC gain A_{DC} is

$$A_{DC} = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{R0 \cdot \Delta I_{SD}}{\Delta V_{SG}} = R0 \cdot g_m \tag{15}$$

where g_m is the transconductance of the input transistor, ΔI_{SD} is the difference of current through drain to source in input transistor during signal input, and ΔV_{SG} is the difference of voltage between input transistors' gate and source during signal input. Not only DC gain, but also there is AC gain caused by the capacitance C0 between output terminal V_{out} and ground. As C0 will work like a low pass filter for the output terminal, AC gain of amplifier will be

$$A_{AC} = \frac{1}{1 + iwC0 \cdot R0} \tag{16}$$

where w is angular frequency of signal. Here, we express the AC gain with the frequency included and as a result, the total voltage gain of amplifier is

$$A = -\frac{R0 \cdot g_m}{1 + iwC0 \cdot R0}. \tag{17}$$

Here, the negative sign refers the change of polarity of the signal, showing the preamplifier is an inverting one. With this result, we can obtain transfer function which describes how current signal converts to voltage signal in the preamplifier. From the preamplifier part in Fig. 3, we can think that input current flow to detector capacitor (C4 in schematic. let's define it as C_{det} from now on) and feedback section. Then we can calculate total current input I_{in} as

$$I_{in} = iw \cdot C_{det} V_{in} + (V_{in} - V_{out}) \left(\frac{1}{R_{fp}} + iwC_{fp} \right) \tag{18}$$

where R_{fp} and C_{fp} are preamplifier feedback resistance and preamplifier feedback capacitance, respectively. The first term in the right hand side equation is current to C_{det} and second term is current to feedback section. After elimination of V_{in} in Eq. 18 with Eq. 17,

$$-\frac{V_{out}}{I_{in}} = \frac{R0 \cdot g_m}{\frac{1+R0 \cdot g_m}{R_{fp}} + iw[\frac{R0C0}{R_{fp}} + C_{det} + (1 + R0 \cdot g_m)C_{fp}] - w^2 R0 \cdot C0(C_{det} + C_{fp})}. \tag{19}$$

Now, let us assume that DC gain of amplifier is very big and feedback capacitance C_{fp} is much smaller than detector capacitance C_{det} in order to get high charge gain, namely

$$C_{det} \gg C_{fp}. \tag{20}$$

Then, the equation is simplified to

$$H(w) = -\frac{V_{out}}{I_{in}} \simeq \frac{R_{fp}}{1 + iw(\frac{C0}{g_m} + R_{fp}C_{fp}) - w^2 \frac{R_{fp} \cdot C_{det} \cdot C0}{g_m}}. \tag{21}$$

To make transfer function even simpler, we let rise time of amplifier output is much shorter than discharge time. Rise time of amplifier output could be expressed as $C0 \cdot C_{det}/g_m C_{fp}$. The term $g_m/C0$ is a unity gain bandwidth of amplifier and C_{fp}/C_{det} is feedback factor. Discharge time, on the other hand, is represented as $R_{fp}C_{fp}$. Short rise time compared with discharge time is required for shaper to response only rising edge of preamplifier output signal. It is therefore possible to assume

$$R_{fp}C_{fp} \gg \frac{C0 \cdot C_{det}}{g_m C_{fp}} \gg \frac{C0}{g_m}. \tag{22}$$

With this condition, transfer function could be further simplified to

$$H(w) = -\frac{V_{out}}{I_{in}} \simeq \frac{R_{fp}}{1 + iwR_{fp}C_{fp} - w^2\frac{R_{fp}C_{detC0}}{g_m}} \tag{23}$$

$$\simeq \frac{R_{fp}}{(1 + iwR_{fp}C_{fp})(1 + iw\frac{C_{detC0}}{g_m C_{fp}})}. \tag{24}$$

From the simplified transfer function above [13], we can understand that current signal of frequency w will converted to voltage output with two pole low pass filter and R_{fp} DC gain. Low pass property of preamplifier can be confirmed by the simulation result in Fig. 15 and will be discussed in the later section.

3.2 Noise from Preamplifier

In practical situation, there are many sources of electronic noise of the preamplifier. For example, noise from each transistors, detector, power supply and parasitics introduced at the layout design stage are possible sources of the noise. In this section, however, we consider the noise factors to sensor leakage current, transistor channel, $1/f$, and thermal noise of feedback resistor since they are more significant than others in our application.

Sensor leakage current is the first main noise source which we will treat. Sensor leakage current I_{leak} has a white noise spectrum with a spectral density A^2/Hz and represented as [13]

$$\frac{\mathrm{d}\langle i_{leak}^2\rangle}{\mathrm{d}f} = 2qI_{leak} \tag{25}$$

where q is the charge of a electron, and f is the frequency. As noise spectrum will be filtered by transfer function, squared rms noise is obtained by integrating noise spectrum over all frequencies.

$$\langle V_{out}^2\rangle_{leak} = \int_0^\infty |H(w)|^2 \frac{\mathrm{d}\langle i_{leak}^2\rangle}{\mathrm{d}f}\mathrm{d}f = 2qI_{leak}R_{fp}^2\frac{1}{4R_{fp}C_{fp}} \tag{26}$$

$$= \frac{qI_{leak}}{2}\frac{R_{fp}}{C_{fp}}. \tag{27}$$

Next main noise source from amplifier is the transistor channel noise. Transistor channel noise is the white thermal noise in the channel of the input transistor with spectral density V^2/Hz and induced by random thermal motion of the electron. General form of transistor channel noise is

$$\frac{\mathrm{d}\langle v_{therm}^2\rangle}{\mathrm{d}f} = \frac{8}{3}\frac{kT}{g_m}. \tag{28}$$

In the equation, k is Boltzmann constant and T is absolute temperature. To calculate squared noise voltage from transistor channel noise, let's assume that the sensor capacitance is dominant in input impedance. Noise current from transistor channel noise will be then

$$\langle i_{therm}^2 \rangle \simeq \langle v_{therm}^2 \rangle \cdot |(iwC_{det})^2|. \tag{29}$$

The output noise voltage from transistor channel noise is

$$\langle V_{out}^2 \rangle_{therm} = \int_0^\infty |H(w)|^2 \frac{\mathrm{d}\langle i_{therm}^2 \rangle}{\mathrm{d}f} = \frac{8}{3}\frac{kT}{g_m} C_{det}^2 R_{fp}^2 \frac{1}{4R_{fp}C_{fp}} \tag{30}$$

$$= \frac{2}{3} kT \frac{C_{det}}{C_{fp}C0}. \tag{31}$$

Another noise source is the transistor $1/f$ noise. $1/f$ noise is associated with carrier trap in semiconductors which capture and release carriers in a random manner [15]. Expression for $1/f$ noise in strong inversion region is

$$\frac{\mathrm{d}\langle v_{1/f}^2 \rangle}{\mathrm{d}f} = \frac{K_f}{C_{OX}W \cdot L} \frac{1}{f}. \tag{32}$$

K_f is device and technology dependent constant, C_{OX}, W, and L are the gate oxide capacitance per unit area, the effective transistor width and length, respectively. Same as before, output noise voltage can be calculated by

$$\langle V_{out}^2 \rangle_{1/f} = \int_0^\infty |H(w)|^2 \frac{\mathrm{d}\langle i_{1/f}^2 \rangle}{\mathrm{d}f} \tag{33}$$

$$\simeq \frac{K_f C_{det}^2 R_{fp}^2}{C_{OX}W \cdot L} \frac{R_{fp}^2 C_{fp}^2}{R_{fp}^4 C_{fp}^4 - \frac{R_{fp}^2 C_{det}^2 C0^2}{g_m^2}} \ln\left(\frac{R_{fp}^2 C_{fp}^2 \cdot g_m}{R_{fp}C_{det}C0}\right) \tag{34}$$

$$\simeq \frac{K_f}{C_{OX}W \cdot L} \frac{C_{det}^2}{C_{fp}^2} \ln\left(\frac{R_{fp}C_{fp} \cdot g_m}{C0} \frac{C_{fp}}{C_{det}}\right) \tag{35}$$

in condition Eq. 22.

The last source of noise we discuss is thermal noise of the feedback resistor. The equation of thermal noise of the feedback resistor can be modeled by

$$\frac{\mathrm{d}\langle i_{Rf}^2 \rangle}{\mathrm{d}f} = \frac{4kT}{R_{fp}}. \tag{36}$$

The spectrum of this noise is A^2/Hz, and calculation of output noise voltage is same with sensor leakage current when we replace qI_{leak} by $2kT/R_{fp}$. As a result, noise voltage from thermal noise of the feedback resistor is

$$\langle V_{out}^2 \rangle_{Rf} = \frac{kT}{C_{fp}}. \tag{37}$$

The total noise from all four noise sources will be then

$$\langle V_{out}^2 \rangle_{preamp} = \langle V_{out}^2 \rangle_{leak} + \langle V_{out}^2 \rangle_{therm} + \langle V_{out}^2 \rangle_{1/f} + \langle V_{out}^2 \rangle_{Rf}, \tag{38}$$

and ENC (Equivalent Noise Charge) could be obtained with above result. ENC is root mean square noise at the output of amplifier normalized to the signal of a single electron input charge. As the output signal is simply the voltage induced by feedback capacitance, ENC of total noise effect in preamplifier can be calculated by [13]

$$\text{ENC}_{preamp} = \frac{C_{fp}}{q}\sqrt{\langle V_{out}^2 \rangle_{preamp}}. \tag{39}$$

3.3 Noise in Preamplifier-Shaper Chain

The noise at the output of amplifying chain can be decreased by reducing bandwidth around signal frequency region. This role can be easily achieved by a CR-RC filter which consists of a CR high pass filter and a RC low pass filter. CR-RC filter usually referred to as shaper which means it translates step pulse to Gaussian signal. Generally there could be many poles for each high pass filter and low pass filter. In our case, however, we will only consider single pole CR-RC filter. As gain of each high pass filter and low pass filter is

$$\text{High Pass Filter} : |A_{HPF}| = \frac{w/w_0}{\sqrt{1+(w/w_0)^2}}$$
$$\text{Low Pass Filter} : |A_{LPF}| = \frac{1}{\sqrt{1+(w/w_0)^2}},$$

our transfer function of a shaper with gain A is

$$H_{shp}^2(w) = A^2 \cdot A_{HPF}^2 \cdot A_{LPF}^2 = A^2 \frac{(w/w_0)^2}{[1+(w/w_0)^2]^2} \tag{40}$$

when w_0 is a bandwidth constant $1/(R0 \cdot C0)$ in Fig. 4 [13]. Before using transfer function of shaper to obtain noise output from shaper, simplifying preamplifier noise factors will be carried out in order to simplify the discussion.

The noise of preamplifier could be modeled by a serial noise voltage source and a parallel noise current source at the input of preamplifier. In Fig. 5, a schematic of such noise model with a charge sensitive preamplifier is plotted. Feedback resistor is neglected in this schematic for simplify the noise source to parallel noise current source I_{par} and serial noise voltage source V_{ser}. I_{par} in Fig. 5 is parallel noise current

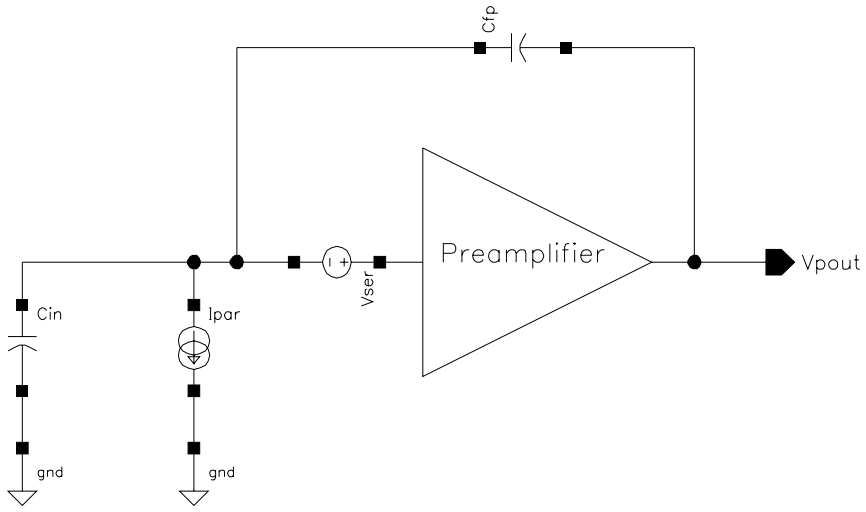

Figure 5: Charge sensitive preamplifier with two input noise sources and capacitive input load. Parallel noise current source is plotted as a current source named I_{par} and serial noise voltage source is plotted as a voltage source named V_{ser}.

source, V_{ser} is serial noise voltage source, and C_{in} is the total capacitance at the input node of preamplifier. If we consider the equations in previous section, we can obtain the frequency spectrum of each serial noise voltage and parallel noise current as [13]

$$\text{Serial noise voltage} : \frac{\mathrm{d}\langle v_{ser}^2(f)\rangle}{\mathrm{d}f} = \frac{\mathrm{d}\langle v_{therm}^2(f)\rangle}{\mathrm{d}f} + \frac{\mathrm{d}\langle v_{1/f}^2(f)\rangle}{\mathrm{d}f} = \frac{8}{3}\frac{kT}{g_m} + \frac{K_f}{C_{OX}W \cdot L}\frac{1}{f}$$

$$\text{Parallel noise current} : \frac{\mathrm{d}\langle i_{par}^2(f)\rangle}{\mathrm{d}f} = \frac{\mathrm{d}\langle i_{leak}^2(f)\rangle}{\mathrm{d}f} = 2qI_{leak}$$

As serial noise voltage source and parallel noise current source are uncorrelated, we can calculate output noise voltage spectrum separately.

For parallel noise, current should flow through the feedback capacitor when input of preamplifier is assumed virtually grounded. Noise output spectrum will be then

$$\text{Parallel noise} : \frac{\mathrm{d}\langle V_{pout.par}^2(w)\rangle}{\mathrm{d}w} = \frac{\mathrm{d}\langle i_{par}^2(w)\rangle}{\mathrm{d}w}\frac{1}{(w \cdot C_{fp})^2} = \frac{2qI_{leak}}{2\pi}\frac{1}{(w \cdot C_{fp})^2}. \quad (41)$$

Serial noise voltage is obtained through the capacitive divider made up of C_{fp} and $C_{in} = C_{det} + C_{parasitic} + C_{preamp}$ while $C_{parasitic}$ and C_{preamp} stand for parasitic capacitance and preamplifier input capacitance respectively. Output noise voltage from serial noise voltage source would be

$$V^2_{pout.ser} = v^2_{ser}\left(\frac{C_{in}+C_{fp}}{C_{fp}}\right)^2 \simeq v^2_{ser}\left(\frac{C_{in}}{C_{fp}}\right)^2.$$

The very right hand side term is obtained by assuming that $C_{fp} \ll C_{det} < C_{in}$ which is same assumption we made in the previous section. With above result, output noise spectrum from serial noise source becomes

$$\text{Serial noise}: \frac{\mathrm{d}\langle V^2_{pout.ser}(w)\rangle}{\mathrm{d}w} = \frac{\mathrm{d}\langle v^2_{ser}(w)\rangle}{\mathrm{d}w}\left(\frac{C_{in}}{C_{fp}}\right)^2 \tag{42}$$

$$= \left(\frac{\mathrm{d}\langle v^2_{therm}(w)\rangle}{\mathrm{d}w} + \frac{\mathrm{d}\langle v^2_{1/f}(w)\rangle}{\mathrm{d}w}\right)\left(\frac{C_{in}}{C_{fp}}\right)^2 \tag{43}$$

$$= \left(\frac{8}{3}\frac{kT}{g_m}\frac{1}{2\pi} + \frac{K_f}{C_{OX}W\cdot L}\frac{1}{w}\right)\left(\frac{C_{in}}{C_{fp}}\right)^2. \tag{44}$$

The total output noise voltage spectrum from both parallel and serial noise is then

$$\frac{\mathrm{d}\langle V^2_{pout.total}(w)\rangle}{\mathrm{d}w} = \frac{\mathrm{d}\langle V^2_{pout.par}(w)\rangle}{\mathrm{d}w} + \frac{\mathrm{d}\langle V^2_{pout.ser}(w)\rangle}{\mathrm{d}w}$$

$$= \frac{2qI_{leak}}{2\pi}\frac{1}{(w\cdot C_{fp})^2} + \left(\frac{8}{3}\frac{kT}{g_m}\frac{1}{2\pi} + \frac{K_f}{C_{OX}W\cdot L}\frac{1}{w}\right)\left(\frac{C_{in}}{C_{fp}}\right)^2$$

Finally, we can calculate total squared shaper noise output voltage by using both transfer function of a shaper and noise voltage spectrum. After quite tedious calculations, total squared shaper noise output voltage is obtained as

$$\langle V^2_{out}(w)\rangle_{shp} = \int_0^\infty H(w)^2_{shp}\mathrm{d}\langle V^2_{pout.total}(w)\rangle \tag{45}$$

$$= A^2\frac{\pi}{4}\left(\frac{qI_{leak}}{\pi C^2_{fp}w_0} + \frac{2}{\pi}\frac{K_f}{C_{OX}W\cdot L}\frac{C^2_{in}}{C^2_{fp}} + w_0\frac{8}{3}\frac{kT}{g_m}\frac{C^2_{in}}{2\pi C^2_{fp}}\right) \tag{46}$$

and this result is confirmed by Mathematica [19]. This output noise voltage must be normalized to a typical signal. Generally ENC is used for this normalization. Before normalization, we have to obtain the maximum amplitude of CR-RC shaper. By taking the inverse Laplace transformation of transfer function of shaper $H_{shp}(w)$, transfer function becomes

$$\frac{V_{out.shp}(t)}{\Delta V_{out.preamp}} = \frac{w_0 t}{e^{w_0 t}}$$

when $\Delta V_{out.preamp}$ is voltage step signal output from preamplifier and input signal for shaper. From the function, it is possible to derive peaking time T_p and peak voltage gain

$$\text{Peaking time}: T_p = \frac{1}{w_0}$$
$$\text{Peak gain}: \frac{V_{out.shp}(T_p)}{\Delta V_{out.preamp}} = \frac{1}{e}$$

With above results, peak output signal amplitude for an input charge of a single electron is $V_{MAX} = A \cdot q/(e \cdot C_{fp})$. Normalized total squared noise output voltage by peak output voltage for a single electron signal is then [13]

$$\text{ENC}_{total} = \sqrt{\frac{\langle V_{out}^2(w)\rangle_{shp}}{V_{MAX}^2}} = \frac{e}{2q}\sqrt{\left(qI_{leak}T_p + \frac{1}{2T_p}\frac{8}{3}\frac{kT}{g_m}C_{in}^2 + \frac{2K_f}{C_{OX}W \cdot L}C_{in}^2\right)}. \tag{47}$$

From the result above, we can find out that increment of W/L and I_{DS} (drain to source current of transistor) leads to an increase of g_m and thus reduces transistor channel noise as g_m in strong inversion region is $g_m \sim \sqrt{(W/L)I_{DS}}$. On the other hand, however, small L may worsen the $1/f$ noise and large I_{DS} will worsen power efficiency and increase the temperature of transistor. Also, increase of transistor width W helps g_m, but effective input capacitance is then also increased. In this manner, we have to optimize every single parameter of transistors such as W, L, and I_{DS} to get lowest noise level from preamplifier-shaper output.

Note that other noise contributions such as intrinsic input capacitance of amplifier, and parasitic capacitance have been neglected in above result and so the result presents only a possible lower limit.

4.0 Basic Mechanisms in MOSFET Amplifier

4.1 Input PMOS

While designing a MOSFET amplifier, it is good to start with understanding the very basic amplifier model. The Fig. 6 is one of the simplest amplifier with a feedback resistor. A PMOS is used as an input transistor for better thermal noise property in high frequency response [13, 20]. Prior to obtaining the transient response simulation result, DC response of the amplifier is investigated as shown in

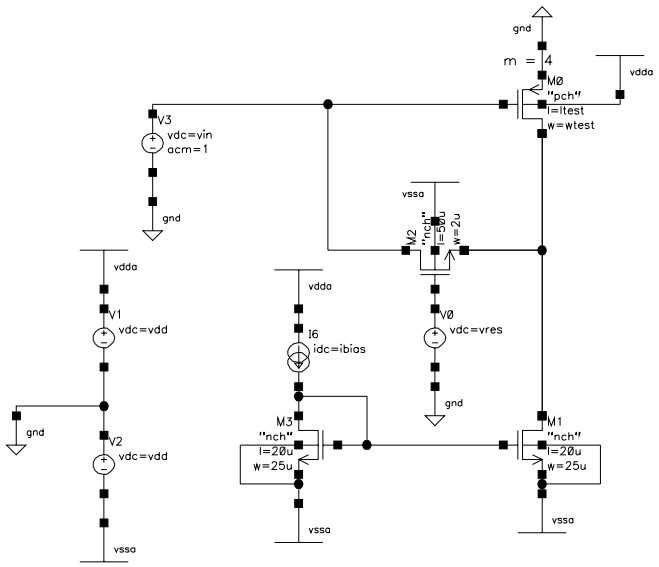

Figure 6: One of the most basic amplifier with feedback resistor. Even though output signal is presented, gain of amplifier is very small as there is no feedback capacitance which is main factor of charge sensitive amplifier.

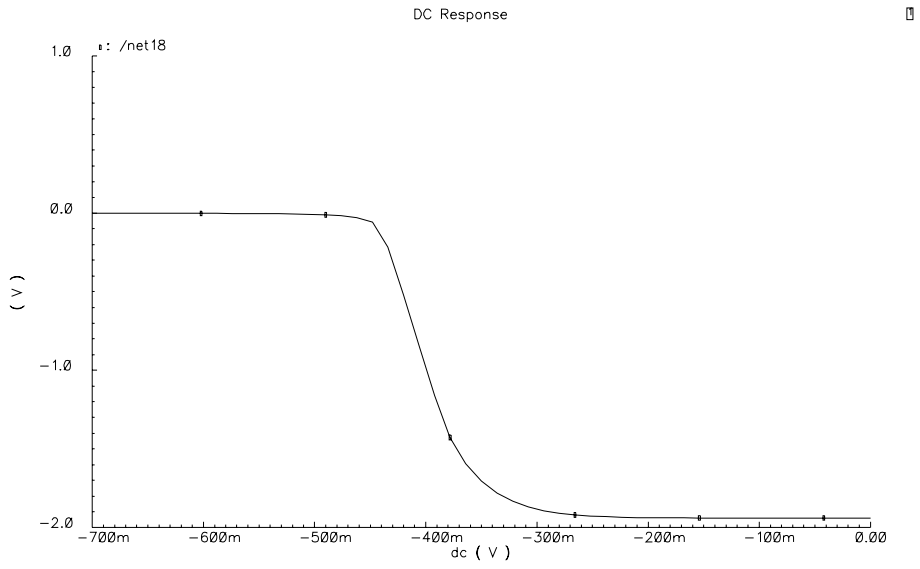

Figure 7: DC sweep simulation result. While input sweeps from -700 mV to 0 V output of amplifier shows the highest gain around -400 mV input voltage. We have to make sure our DC offset of amplifier is near the highest gain region.

Fig. 7. In the figure, we see that the desired DC offset of input and output is around -400 mV to get the highest gain (highest slope). With this conception, if we look at

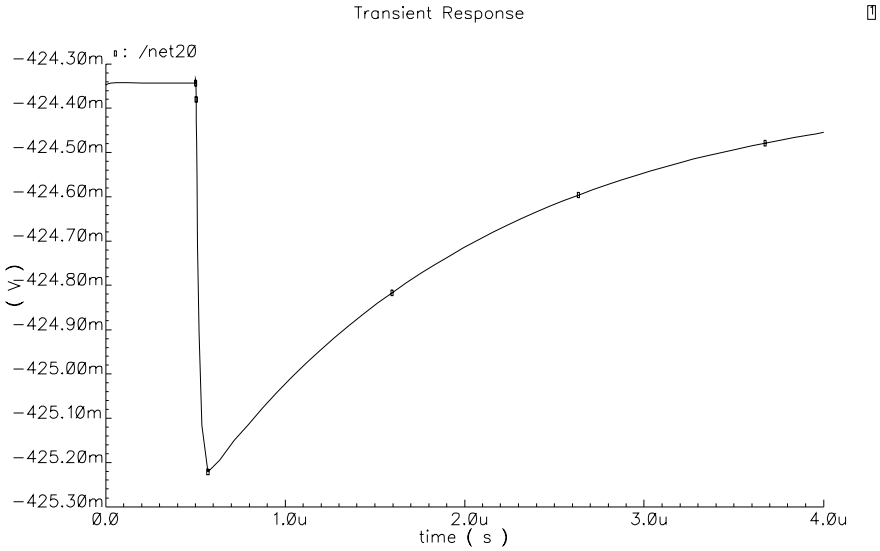

Figure 8: Transient response of basic amplifier (Fig. 6). 25,000 electrons are injected as a charge pulse input signal. DC offset of output is approximately -424 mV. This offset level consists with the highest gain region in Fig. 7.

transient response simulation result Fig. 8, DC offset of output is approximately -424 mV which is close to the highest slope in DC response. In Fig. 8 result, however, output signal is less than 1 mVpp (peak to peak). This is because this basic amplifier (Fig. 6) doesn't have any feedback capacitance which actually amplifies the current input to voltage output in it. In the basic amplifier model, our goal is to set the DC offset at the appropriate level. In our KUPID models, feedback capacitor will be present.

4.2 Cascaded NMOS

After we confirm that DC offset of our basic amplifier is in acceptable region, we moved on to the next stage, cascaded NMOS. In Fig. 9, a cascaded NMOS (M6) after input PMOS transistor is shown. Cascaded NMOS is attached to reduce big Miller capacitance result in big input PMOS transistor. Big input PMOS is necessary to reach low noise [13, 15, 16, 20]. With big Miller capacitance, however, it is impossible to obtain very fast output signal. The concept for cascaded NMOS is very simple. In Fig. 10, there are three unexpected capacitors which show Miller captaincies for each input and cascaded transistors. From input terminal to output terminal, signal

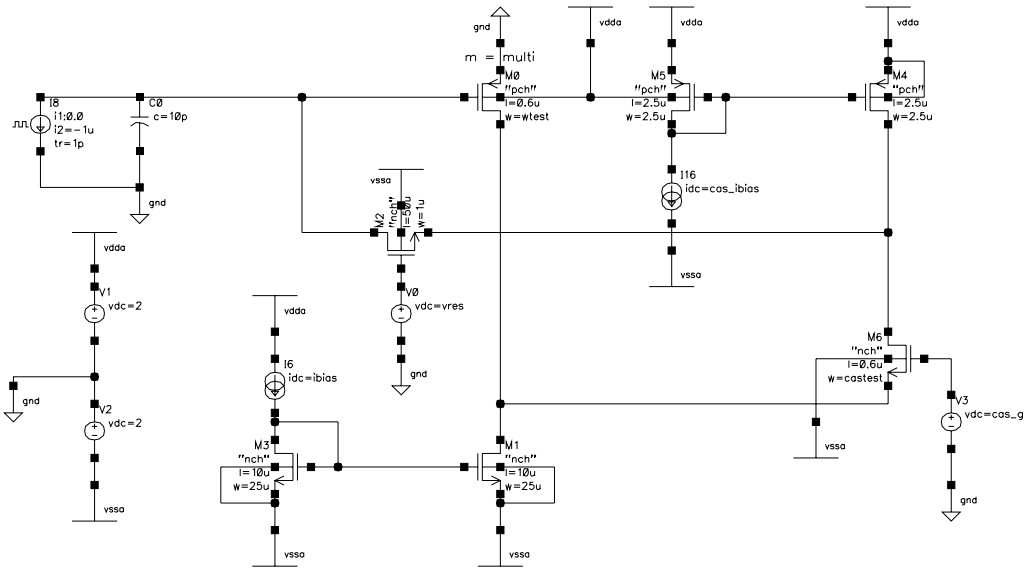

Figure 9: Preamplifier schematic with cascaded output. Cascaded NMOS (M6 in the figure) is added to reduce big Miller capacitance of input transistor. Input transistors with large W/L are designed to obtain low channel and $1/f$ noise from input transistor.

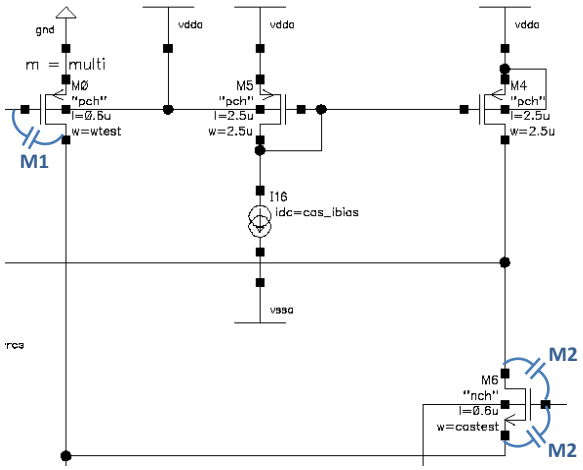

Figure 10: Miller capacitors in the preamplifier with cascaded output. In the schematic, input signal has to pass through three Miller capacitors to reach output node. As three Miller capacitors are connected serial, total capacitance will be close to smallest value. Cascaded NMOS is designed much smaller sized transistor compare with input transistor.

has to pass through three series connected Miller capacitors. As capacitance of serial connected capacitors become closer to the smallest connected capacitor, cascaded NMOS should have small Miller capacitance compare with PMOSs'. This condition makes cascaded NMOS to be a small-size transistor.

After understanding the role of cascaded NMOS, we simulated DC sweep for cascaded NMOS part to find correct DC offset for cascaded output. In Fig. 11, DC sweep is executed for cascaded input (V4) and cascaded output is obtained (net between M4 and M6 transistor). DC response and transient response is plotted in Fig. 12 and right plot of Fig. 13. Transient response shows that DC offset of cascaded output is about -711 mV and signal is about 2 mVpp. The slop in DC response (Fig. 12) around -711 mV output is about 1. As a result, cascaded output shows same peak to peak output signal with basic amplifier. However when we compare output signal of basic amplifier and cascaded amplifier (Fig. 13), cascaded output shows three times bigger signal than basic amplifier. We argue that less Miller capacitance of cascaded model caused better AC response and made cascaded model higher gain than basic amplifier model. Not only the gain, but also rise time of output signal could be faster by reducing Miller capacitance in cascaded model. Note that, the rise time of basic amplifier is approximately 80 ns while cascaded model is 20 ns, supporting the arguments above.

4.3 CR-RC Shaper

The output signal of preamplifier should be designed with short rise time and long discharge time according to the theoretical calculations described in the previous sections. Shaper which follows the preamplifier then has to be optimized to pass limited bandwidth frequency around rise time of preamplifier output signal. In shaper schematic shown in Fig. 14, we could form high pass filter and low pass filter components. C10 and M15 components form high pass filter while C6 and M15 make low pass filter in the schematic. As there are only one high pass filter and low pass filter, our shaper is a CR^N-RC^M shaper with $N = M = 1$ which is the simplest model. When we obtain AC response of preamplifier-shaper chain we can confirm whether shaper operates well or not. AC response simulation result is plotted in Fig. 15. In Fig. 15, one curve which behaves like low pass filter and another one which acts like band pass filter are AC response of preamplifier and shaper respectively. From the simulation result, we could find out that our shaper

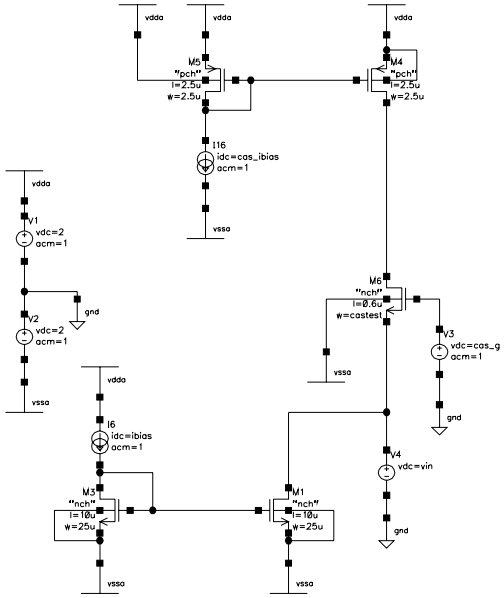

Figure 11: Test schematic for DC sweep of cascaded NMOS input. This schematic is cascaded output part of preamplifier Fig. 9.

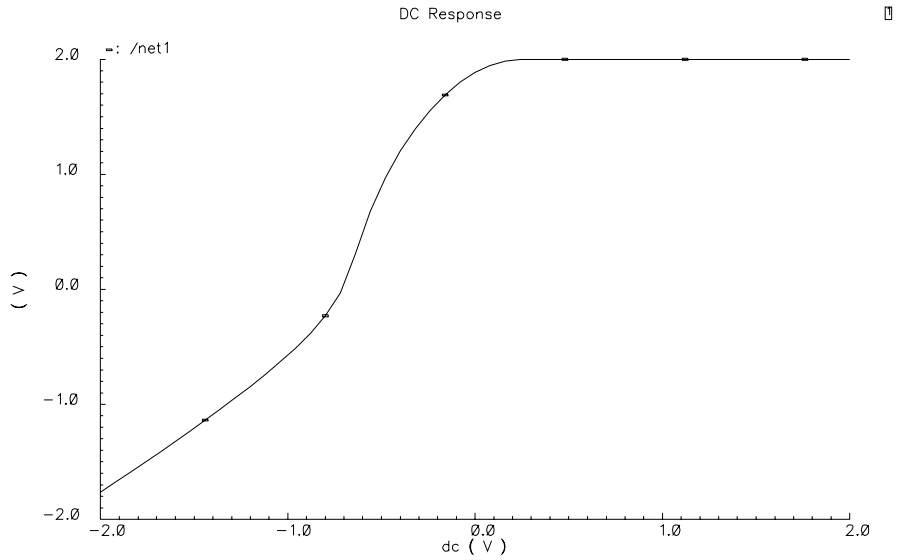

Figure 12: Simulation result of DC sweep of Fig. 11. Input voltage (V4 in Fig. 11) is swept from -2 V to 2 V. To get linear gain from cascaded NMOS, DC offset voltage should be lower than -700 mV.

satisfies the property of *CR-RC* filter.

With all simulation results and theoretical calculations, we could start designing

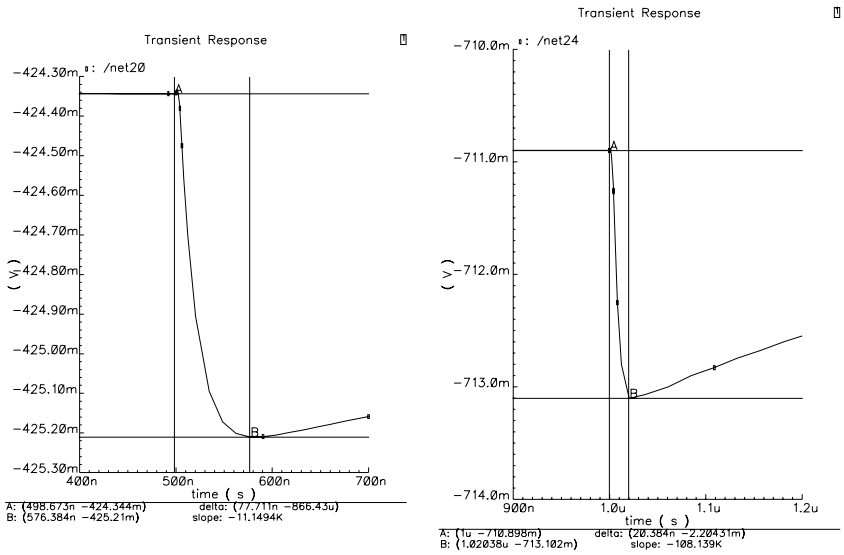

Figure 13: Transient responses from basic preamplifier (no cascaded, left plot) and preamplifier with cascaded output (right plot). Output of cascaded design has amplitude with three times bigger and 1/3 times shorter rise time. From this result, reduction of Miller capacitance is confirmed.

new version of prototype KUPID. Simulated performance of first prototype KUPID v1.0 and KUPID v2.0 will be shown in following sections. And we compared simulated and measured performance of KUPID v1.0.

5.0 KUPID v1.0 Simulation Results

In Fig. 16, a schematic for KUPID v1.0 preamplifier stage is shown. P0 is the input transistor which receives the current from the sensor, and P8 and C0 are feedback resistor and capacitor, respectively. The usual folded cascade configuration (N1 NMOS in Fig. 16) is adapted for a large dynamic range amplification and smaller noise performance. For the shaper design, schematic is basically same with the preamplifier design but has different shaping parameters for the CR-RC network. The size of the PMOS and biasing methods for preamplifier-shaper, however, were not fully optimized at the design stage due to imperfect knowledge in the entire circuit noise optimization process.

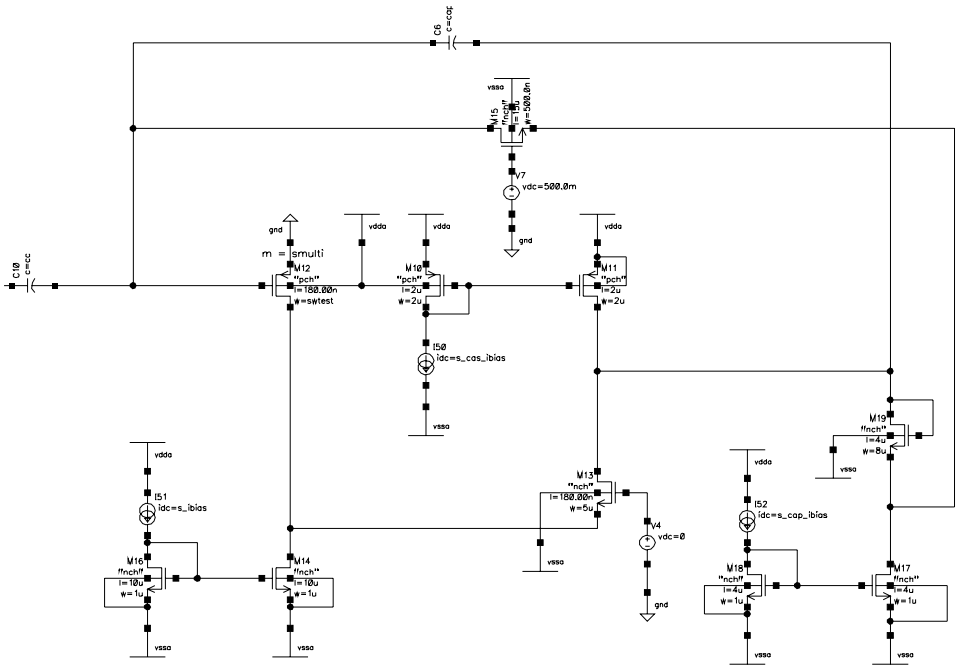

Figure 14: Schematic for *CR-RC* shaper with both feedback capacitor and resistor. In the schematic high pass filter is formed by components C10 and M15 (as a resistor), low pass filter by C6 and M15. As there are one high pass filter and low pass filter each, theoretical approach of single pole *CR-RC* filter in section 2.3 is applicable.

At the initial stage of the study of the v1.0, we used HSPICE simulation software to get simulation results. However, there was troubles with obtaining desired AC and noise response due to the fact that our knowledge on the HSPICE usage was limited at that time. As a result, we studied the voltage responses only in the initial phase. In Fig. 17, voltage steps of 40 mV with 100 ns width signals are injected as an input while there was no capacitor for charge input transition and detector capacitance simulation. As there was no input signal transition from voltage to charge, it is impossible to calculate input MIP signal from voltage signal. 200 mVpp (peak to peak) output signal from shaper in Fig. 17, however, led us to misunderstand that the gain from preamplifier-shaper is approximately 5 though preamplifier is designed as charge sensitive amplifier.

Later stage, we realized a easier tool called Spectre in terms of the flexibility and easiness of the usage with the help from Hawaii group [22] . We would like to point however that this came later than the submission of the v1.0 therefore serious

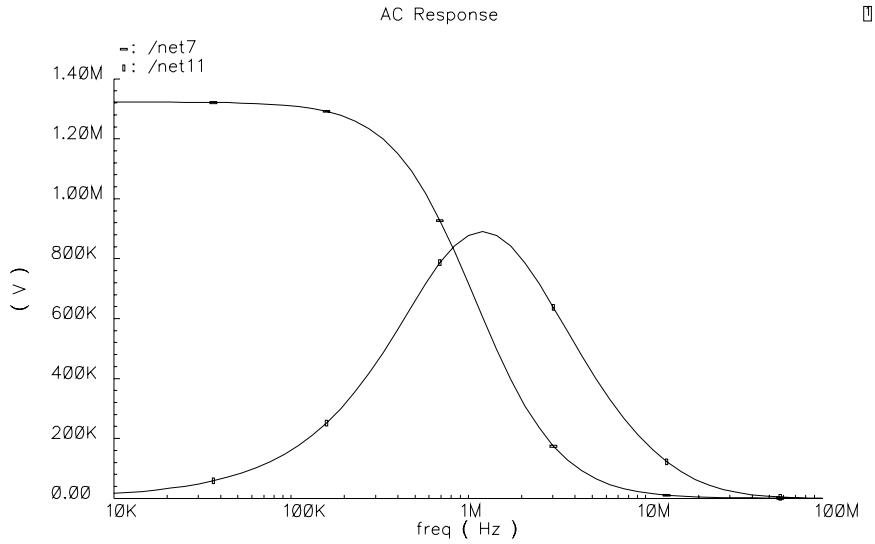

Figure 15: AC response simulation result of preamplifier-shaper chain. The curve on the left is AC response of preamplifier. AC response of shaper is shown as the right curve (Gaussian shape curve). Low pass filter like property of preamplifier is calculated in previous section (Eq. 17). The frequency band where shaper passes is around preamplifier output signal frequency.

simulation study including the noise study for example was only possible afterward.

We re-simulated v1.0 using Spectre with a signal step caused by an input current of one MIP signal which has 25,000 electrons from 300 μm thick silicon detectors. The results from Fig. 18, 19, and 20 are obtained with detector capacitor of 10 pF. From the result in Fig. 18, voltage output is a 2 mVpp (peak to peak) and therefore the gain is approximately derived as

$$2 \text{ mV/MIP} = 2 \text{ mV}/(25,000 \times 1.6 \times 10^{-19} \text{ C}) = 0.5 \text{ mV/fC} \qquad (48)$$

(for a comparison, output gain of VA is 10 μA/fC, [10]). AC response(Fig. 19) and noise response(Fig. 20, Fig. 21) are the results which we failed to obtain from HSPICE simulation. From AC response in Fig. 19, peak value is shown around 400 kHz. As input charge signal has frequency of MHz scale, low output gain is caused by low AC response in MHz area.

For the noise performance, we study the voltage power spectrum of the circuit, shown in Fig. 21. It shows the power spectra with detector capacitance values from 0 pF to 20 pF in steps of 5 pF. From this simulation result, we obtained RMS noise

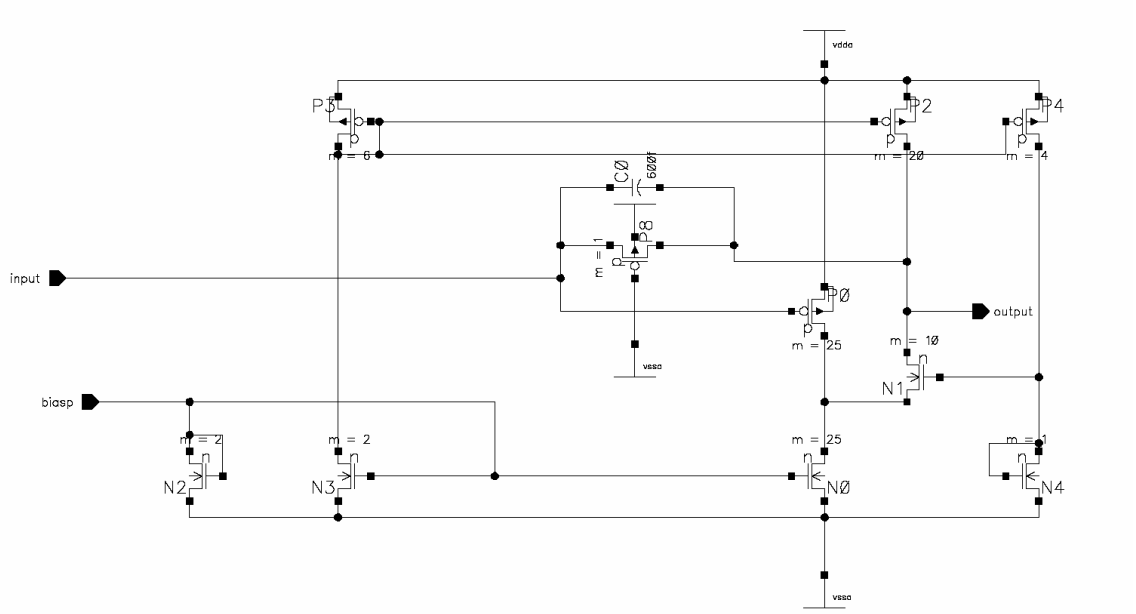

Figure 16: An example of KUPID v1.0 preamplifier schematic is shown. P0 is the main input transistor, which amplifies the current signal from a sensor. N1 is a cascade transistor which is intended to reduce big Miller capacitance of the input transistor.

value which is integrated value for a specific range of frequency. For example, with the 10 pF detector capacitance, RMS noise integrated from 10 kHz to 100 MHz value was approximately 4.399 mV. We then calculate the noise in the unit of the electron charge (ENC) at 10 pF detector capacitor as

$$\text{ENC} = \frac{\nu_{RMS} \cdot N_{in}}{V_{op}}$$

$$= \frac{4.399 \text{ mV} \times 25,000}{2 \text{ mV}}$$

$$\simeq 55,000$$

where, ν_{RMS} is RMS noise voltage value, N_{in} is number of electrons as an input signal, and V_{op} is output peak to peak voltage signal [14]. Repeating the above

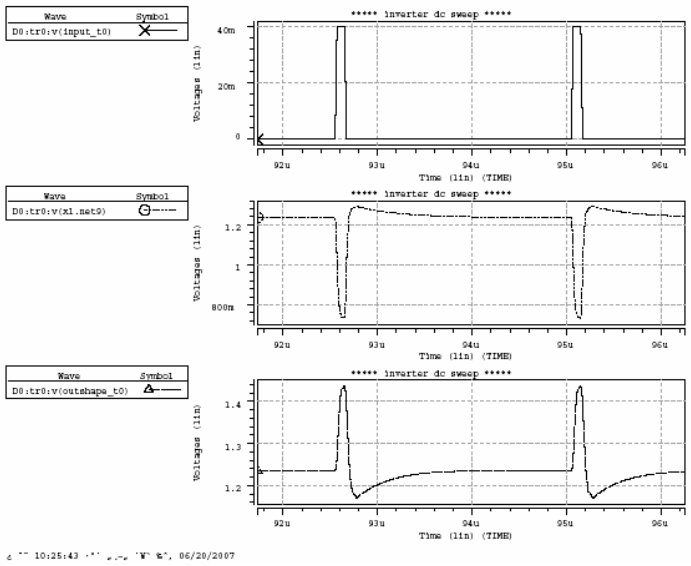

Figure 17: Transient response simulation result using HSPICE. Input voltage is presented on the top figure, while output signal from preamplifier and shaper is presenter on the middle and the bottom respectively. The values of heights and widths are better described in the context.

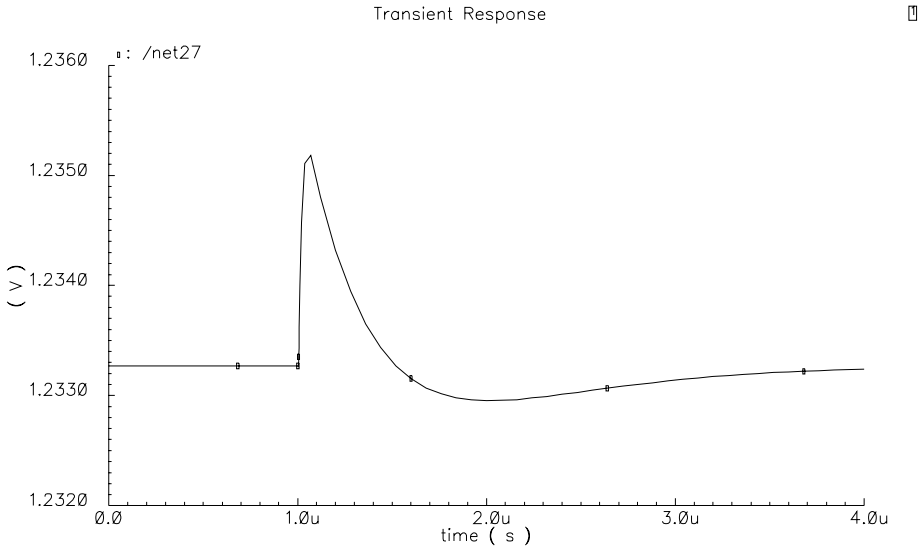

Figure 18: KUPID v1.0 transient simulation result of the full preamplifier-shaper output as a function of time in μs. A pulse corresponding to a MIP worth of charge is injected in to the circuit. A clear under shoot of the signal is seem at 2.0 μs.

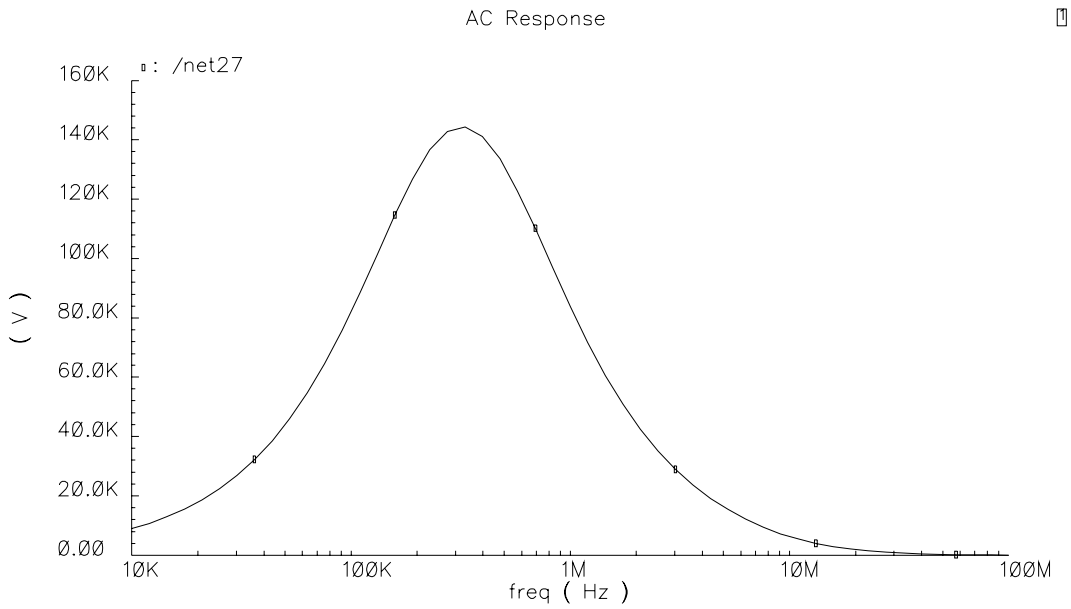

Figure 19: KUPID v1.0 AC response simulation result of the preamplifier-shaper output as a function of frequency in log scale. Peak AC response is shown around 400 kHz frequency area. To get better response in high frequency, peak point of AC response should be located higher frequency area.

calculation with different values of detector capacitance, we obtained ENC values for various detector capacitance and they are shown in Table 1 and Fig. 22. From the linear fit in Fig. 22, ENC values are modeled as

$$\mathrm{ENC} \simeq 25800 + 3211/\mathrm{pF} \tag{49}$$

From Eq. 49, the ENC value becomes 25800 at zero capacitance with the slope of 3211/pF and both are too large values to see one MIP signal. When one MIP signal from silicon detector has 25000 number of electrons, even if detector capacitor is 0 pF, noise charge is 25800 number of electrons which is bigger than one MIP. So, we conclude it is impossible to detect one MIP signal with v1.0. As was mentioned earlier, the first prototype has insufficient optimization in terms of the noise performance and this rather a large noise value is attributed from it. Nevertheless, we attempted to learn any extra information from the real data with the 1st prototype as much as possible and are described in the next section.

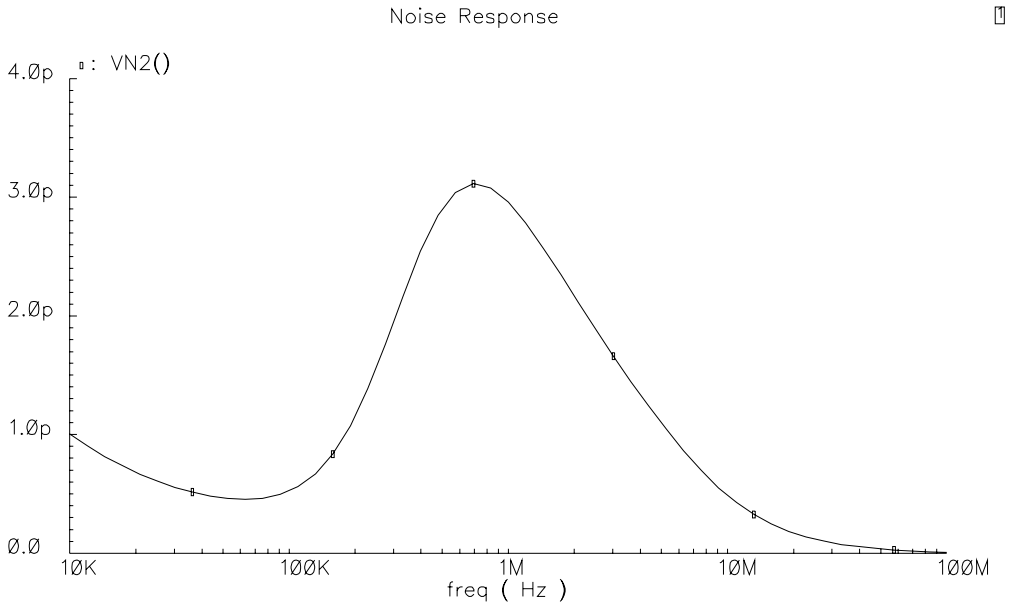

Figure 20: KUPID v1.0 noise response simulation result as a function of frequency in log scale. A lump around 1 MHz area changes it's shape as detector capacitance changes. Above result is when 10 pF detector capacitance presented.

6.0 Performance of KUPID v1.0

In the previous section, we summarized simulation results of KUPID v1.0 and described calculated ENC values. In this section, we describe real measurements and compare with simulation predictions. A simplified schematic for measurement setting is shown in Fig. 23. The charge injection is made from a pulse generator (Agilent 33250A) and is fed into a home made PCB which is shown in Fig. 24. There is a voltage regulator attached on PCB in order to stabilize the external VDD source.

A real transient response measured from v1.0 is shown in Fig. 25 when 50 mV step voltage is generated by the pulse generator. The top curve in the figure is the input voltage step injected into a 10 pF capacitor and the bottom curve is the output from v1.0. The first prototype that was made in out lab shows an output demonstrating its operation is achieved. On the other hand, we see a clear undershoot at the output. This may be partially understood from the fact that there is no pole-zero cancellation circuit implemented in the design.

After we verified that KUPID v1.0 is at least workable as a preamplifier-shaper,

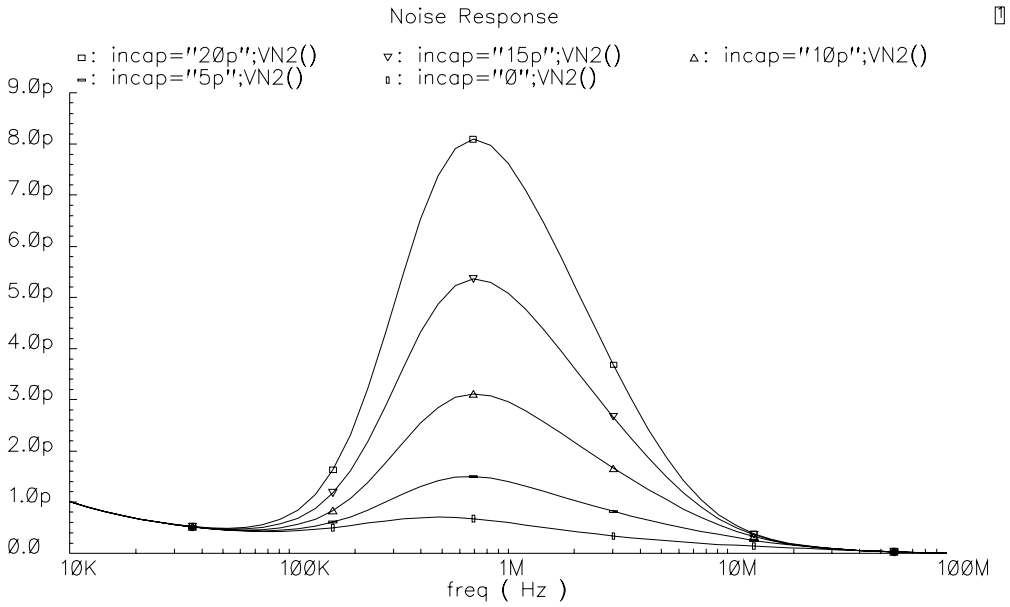

Figure 21: KUPID v1.0 noise response simulation result as a function of frequency in log scale with various detector capacitance. In the result, detector capacitance 0, 5 pF, 10 pF, 15 pF, and 20 pF are used. The smaller detector capacitance is, the smaller lump is shown in the result.

we measured the performance of KUPID v1.0 such as gain and ENC. To estimate the gain of KUPID v1.0, first we have to calculate the input voltage for one MIP signal when we used 25000 number of electrons as one MIP signal from 300 μm silicon sensor. The total charge for one MIP is

$$1 \text{ MIP} = 25000 \times 1.6 \times 10^{-19} \text{ C} \tag{50}$$

$$\simeq 4.0 \times 10^{-15} \text{ C} \tag{51}$$

To inject one MIP charge signal from voltage signal, we have to translate voltage signal to charge signal by series connected capacitor to KUPID v1.0 as we can't make a charge pulse with typical pulse generator. We used 10 pF capacitor for the signal translation and therefore, voltage signal for one MIP charge injection will be

$$\frac{1 \text{ MIP}}{10 \text{ pF}} = \frac{4.0 \times 10^{-15} \text{ C}}{10 \text{ pF}} \simeq 0.4 \text{ mV} \tag{52}$$

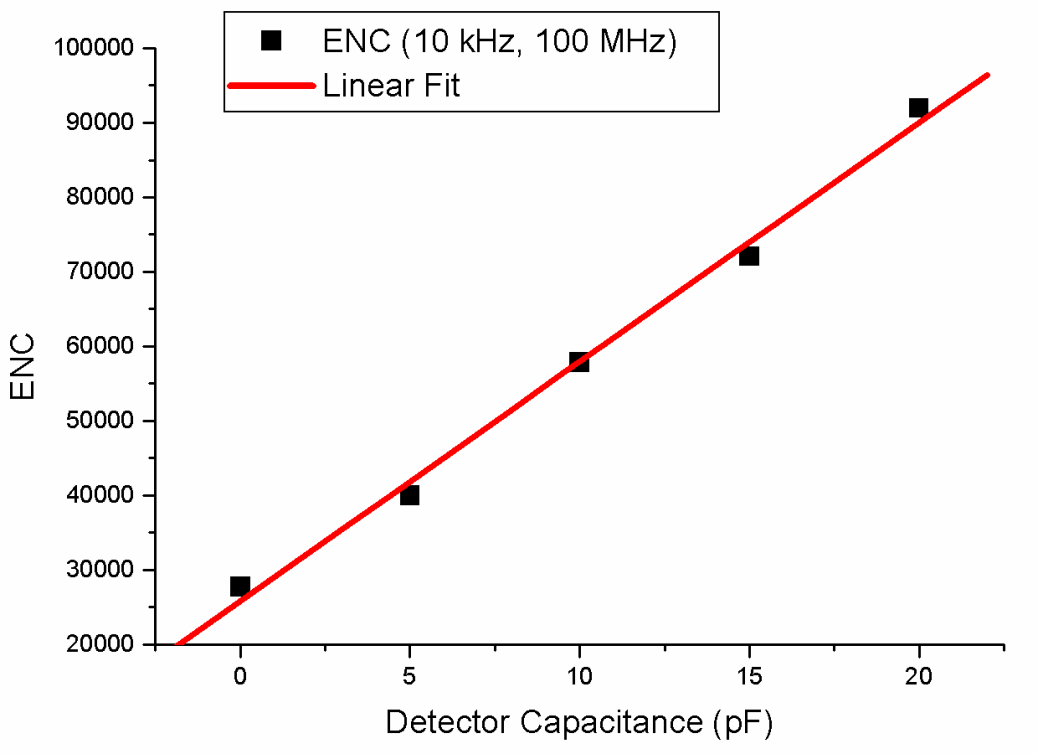

Figure 22: KUPID v1.0 ENC slope as a function of detector capacitance. Closed square boxes are from calculations and the line is from a linear fit.

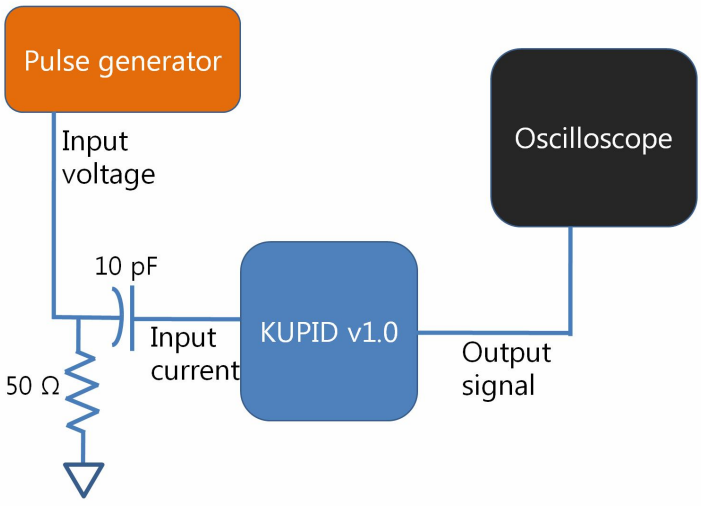

Figure 23: Measurement setting for KUPID v1.0. To inject current signal to preamplifier, 10 pF capacitor is connected serial. And output signal from KUPID is observed by an oscilloscope.

Detector Capacitance(pF)	ENC(number of electrons)
0	27740
5	39940
10	57880
15	72070
20	91950

Table 2: ENC for various detector capacitance. With these values, ENC slope is obtained by linear fit in Fig. 22.

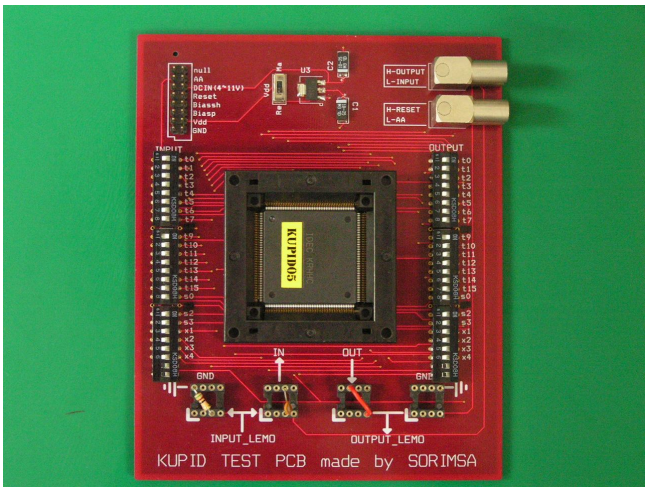

Figure 24: A PCB board fabricated for KUPID v1.0 is shown. In the PCB board, there is a voltage regulator which stabilizes VDD voltage to 1.8 V.

With this, the input voltage step is scanned in units of MIPs in order to check the linearity and the noise level. The result is shown in Fig. 27 and Table 2. Measuring the output, we were unable to separate signal and pedestal when injection signal is lower than 50 MIP due to the baseline voltage noise level seen in the scope. From the linear fit result 0.62 mV/MIP in Fig. 27, we obtain the gain of KUPID v1.0 to be

$$0.62 \text{ mV/MIP} = 0.62 \text{ mV}/(4 \times 10^{-15} \text{ C}) = 0.156 \text{ mV/fC} \tag{53}$$

Compare with the simulation result, 0.5 mV/fC (Eq.48), gain obtained from measurement is only 30% of what we expected from the simulation. After changing oscilloscope to a FADC in previous measurement setting, we obtained signal and

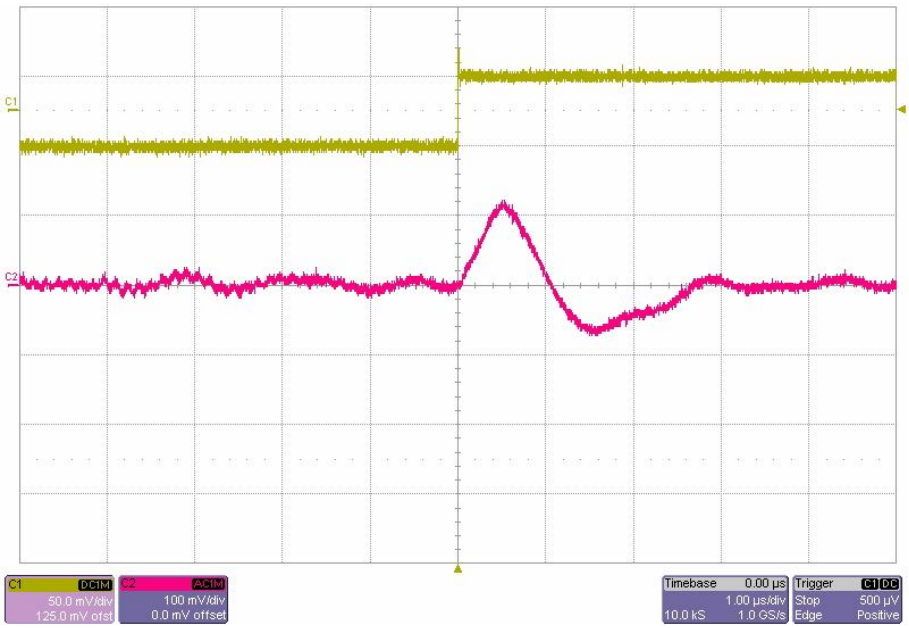

Figure 25: Transient response measured from KUPID v1.0 with zero detector capacitance. Channel 1 (C1; top curve) is the input voltage to KUPID v1.0 pass through series 10 pF capacitor. Channel 2 (C2; bottom curve) is output from KUPID v1.0 observed with oscilloscope.

pedestal histogram with a Gaussian fit in order to estimate the signal to noise ratio.

7.0 Design of KUPID v2.0 and Simulation Results

As noise problem of KUPID v1.0 was rather unpleasant and it was not easy to find a way to solve noise problem, we started to make a new design for KUPID v2.0, not modifying the old one. This time, we inherited large part of the design from NIKHEF [20]. From starting the most basic MOSFET amplifier to preamplifier-shaper chain, all simulations are produced. The figure below is the final schematic for preamplifier in KUPID v2.0.

Main differences between KUPID v1.0 and v2.0 are

- control voltage for each current sources and feedback resistor separately to optimize the status of each MOSFETs.

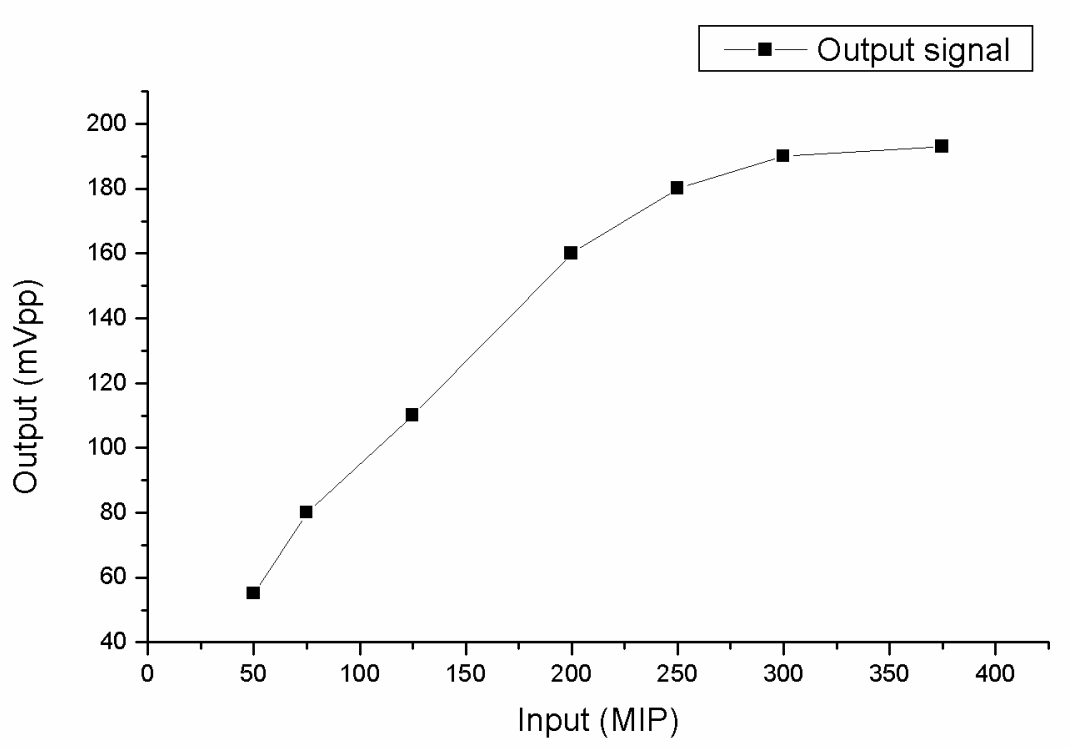

Figure 26: Saturation property of KUPID v1.0 as a function of injected MIP signal. Until approximately 250 MIP, output signal linearity preserved. After 300 MIP charge injection, output signal saturated to 190 mV approximately.

- increase the size of input transistor(M0 in Fig. 28) to reduce noise, and optimize each MOSFET size for noise performance.
- two channel sample/hold, multiplexer (MUX) added for test.

For the shaper part, design is same with preamplifier part but has different shaping parameters for *CR-RC* filter function, like KUPID v1.0.

From the transient response simulation result in Fig. 29, output signal is approximately 40 mV when 25,000 electrons are injected as one MIP signal with 20 pF detector capacitance. Therefore, the gain is derived as 10 mV/fC which is approximately 20 times bigger than KUPID v1.0 (0.5 mV/fC, Eq. 48). In Fig. 30, linearity property of KUPID v2.0 for transient response is shown. In the figure, from bottom curve to top curve, 7.5, 10, 12.5, 15, 17.5 and 20 MIP charge signals are injected. Between 15 and 17.5 MIP charge injection, output signal saturated to approximately 1.7 V. The linearity slope of KUPID v2.0 is obtained in Fig. 31.

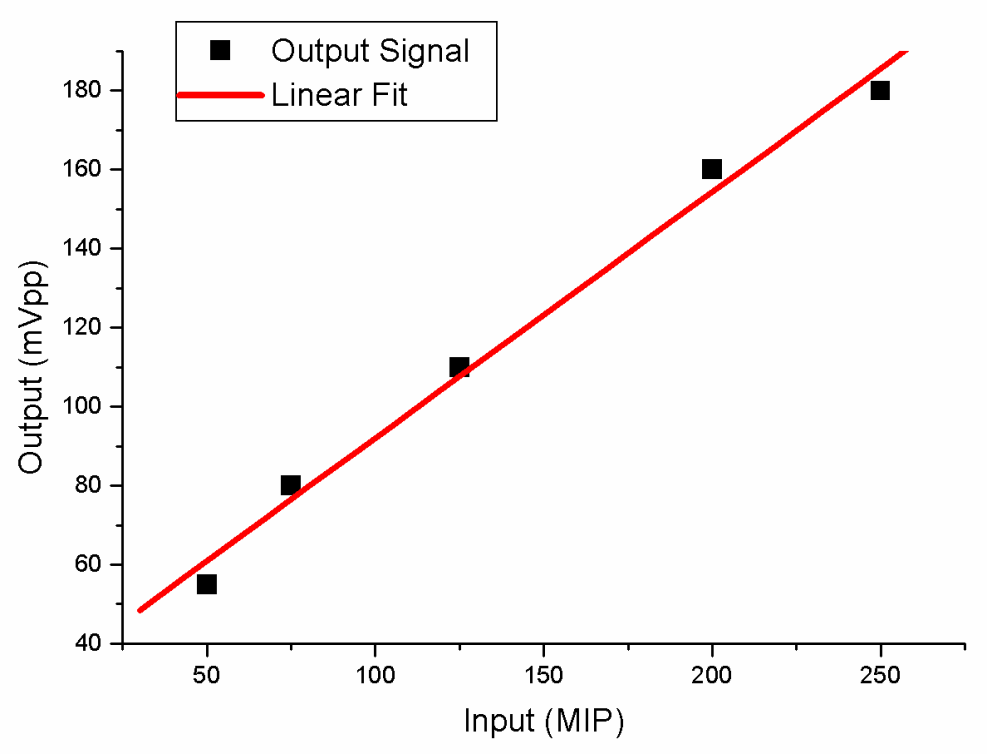

Figure 27: Linearity of KUPID v1.0 as a function of injected MIP signal. Injecting under 50 MIP, we can't distinguish the output signal from baseline voltage of pedestal. We used data points which are lower than saturated region from Fig. 26 to get the linearity slope. From the fit result, linearity slope is 0.62 mV/MIP.

As we are not observing the limitation of linearity (Fig. 30), this time we injected 0.5, 2.5, 5, 7.5 and 10 MIP charge to KUPID v2.0. From the linear fit result in Fig. 31, we obtained that the linear slope is approximately 63.7 mV/MIP which is 100 times bigger than KUPID v1.0's performance. In AC response simulation result (Fig. 32), we can confirm that AC response in high frequency area became much better than KUPID v1.0 (Fig. 19) as the summit of AC response for KUPID v2.0 is at 1 MHz while v.10 was at 400 kHz instead. The AC response values at 1 MHz for both KUPID v1.0 and v2.0 are 80 kV and 850 kV respectively, and the increase of gain of KUPID v2.0 would be caused by this increment of AC response. Not only transient and AC response, but also noise response improved its performance in the simulation result. In Fig. 33 it is certain that noise level was reduced from pV^2 to fV^2 order compared to KUPID v1.0s result (Fig. 20). The RMS noise integrated from 10 kHz to 100 MHz in 10 pF detector capacitance is 1.3767 mV, and with this

Input (mV)	Input (MIP)	Output (mV)
20	50	55
30	75	80
50	125	110
80	200	160
100	250	180
120	300	190
150	375	193

Table 3: Output signals from various input signals. MIP values are calculated with Eq. 52.

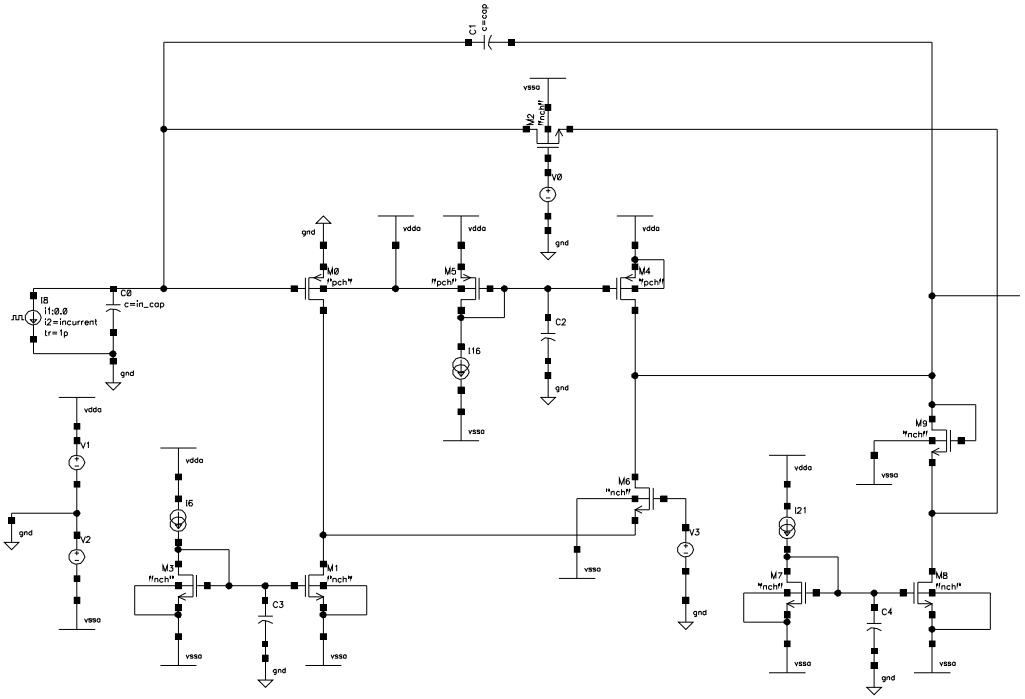

Figure 28: KUPID v2.0 preamplifier schematic. M0 PMOS and M6 NMOS are input and cascaded transistor respectively. While there was only one controllable bias voltage for KUPID v1.0, there are three controllable bias voltage and one for feedback resistor control in KUPID v2.0.

RMS noise and transient response output values, we can calculate ENC at 20 pF detector capacitance as,

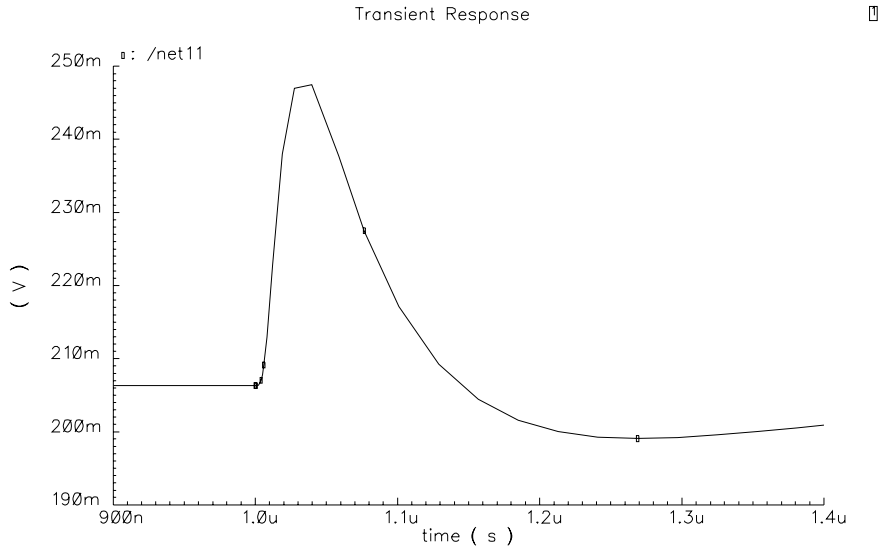

Figure 29: KUPID v2.0 transient simulation result of the full preamplifier-shaper output as a function of time in μs. This time, 25,000 number of electrons are used as one MIP signal which produced in 300 μm thick silicon detectors.

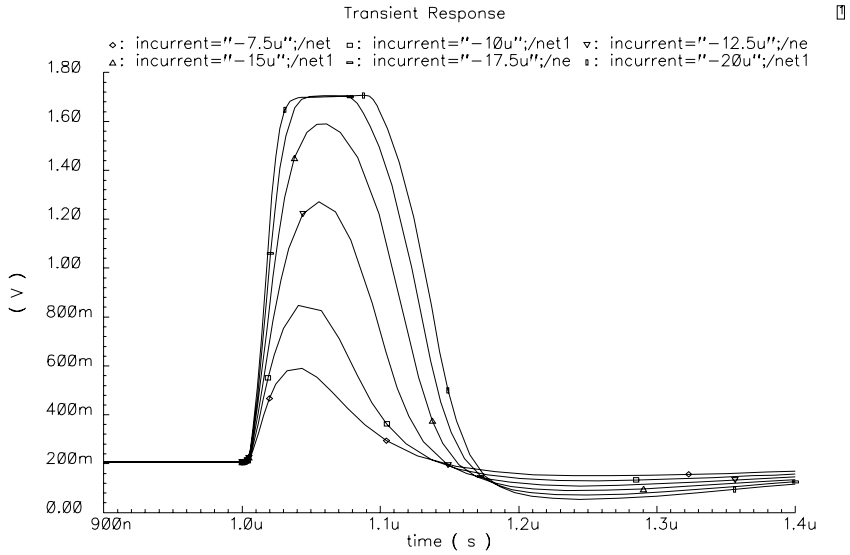

Figure 30: Linearity property of KUPID v2.0. 5 different input signals from 7.5 MIP to 20 MIP are injected in order. In the figure, output signal saturated to approximately 1.7 V when input signal increased higher than 15 MIP.

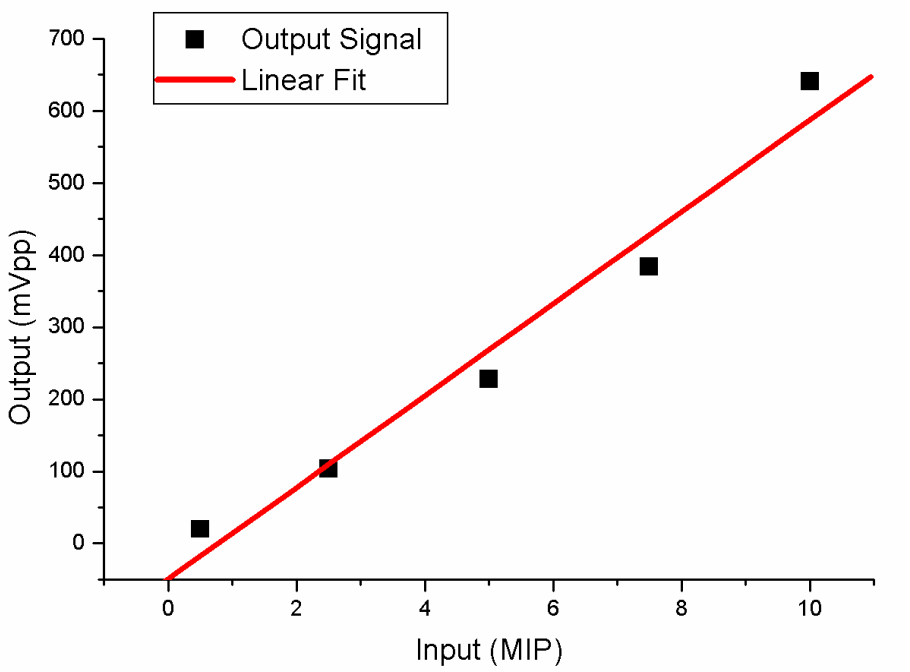

Figure 31: KUPID v2.0 linearity slope with linear fit. 0.5, 2.5, 5, 7.5, and 10 MIP signals are used to obtain linearity. From the fit result, linearity slope is 63.7 mV/MIP, which is approximately 100 times bigger than KUPID v1.0's performance (Fig. 27).

$$\text{ENC} = \frac{1.3767 \text{ mV} \times 25,000}{41 \text{ mV}}$$

$$\simeq 826$$

Similar to what we have done in the previous section, we obtained ENC values for detector capacitors of 0, 5, 10, 15, and 20 pF in Table 4.

By a linear fit of Table 4. results, we obtain Fig. 34.

The result of linear fitting from Fig. 34 is

$$\text{ENC} = 176 + 32/\text{pF} \tag{54}$$

From the ENC obtained in Eq. 54, noise level was reduced from the result in the KUPID v1.0 (25800+3211/pF; Eq. 49) significantly, as each y intercept and slope values decreased to 0.7% and 1% respectively. In case of one MIP (25,000 number of

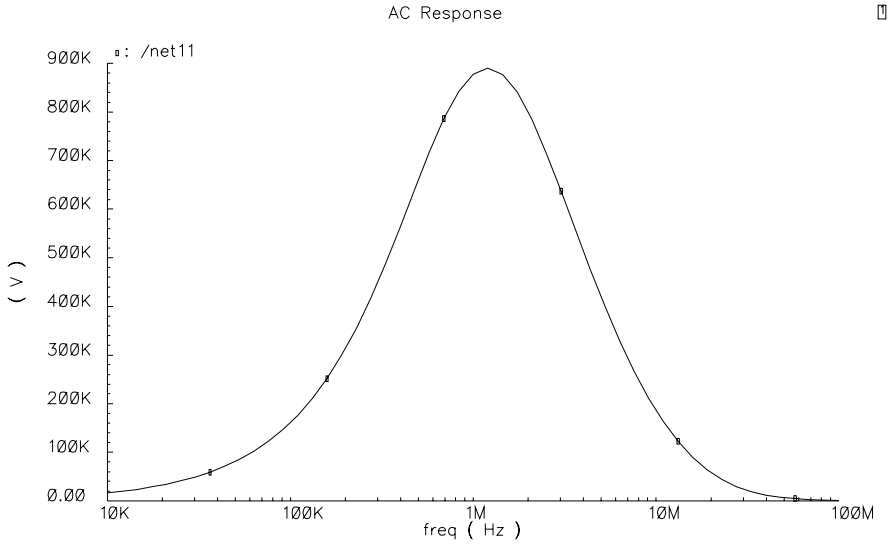

Figure 32: KUPID v2.0 AC response simulation result. Peak AC response frequency increased from 400 kHz to 1 MHz compare with KUPID v1.0 (Fig. 19).

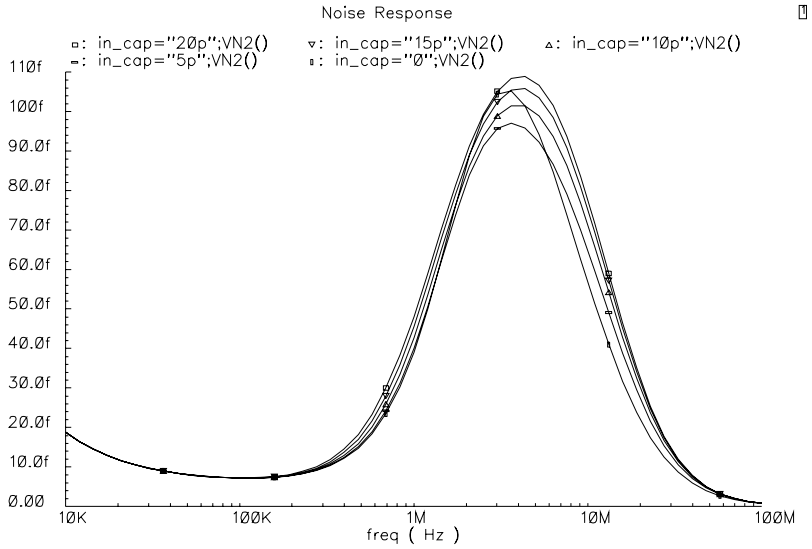

Figure 33: KUPID v2.0 noise response simulation result as a function of frequency. Noise level of peak noise response value reduced from pV^2 to fV^2 order compare to KUPID v1.0 (Fig. 20).

electrons) signal input, with KUPID v2.0, we should be able to separate output sig-

Detector Capacitance(pF)	ENC(number of electrons)
0	177.3
5	337.8
10	498.3
15	665.1
20	826

Table 4: Table 4. ENC for various detector capacitance. With these values, ENC slope is obtained by linear fit in Fig. 34.

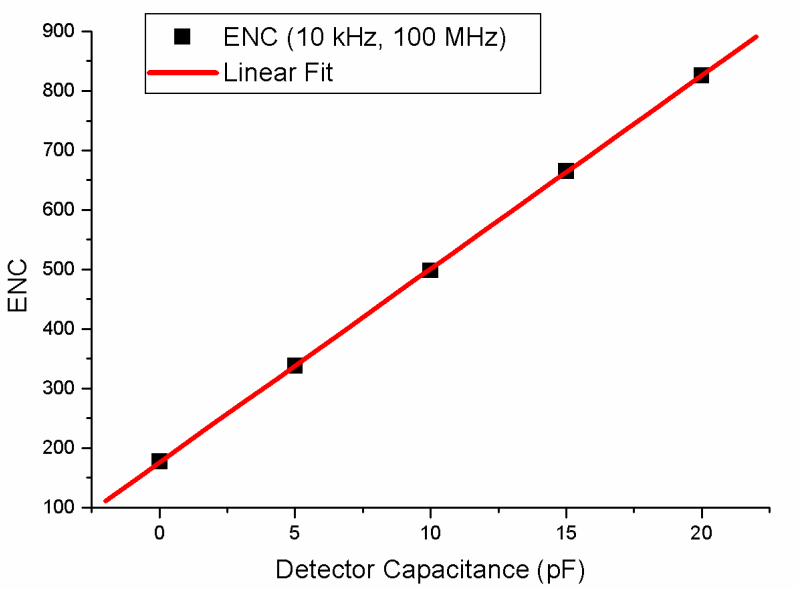

Figure 34: KUPID v2.0 ENC slope with linear fit. Compare with ENC slope of KUPID v1.0 (Fig. 22), y intercept and slope values decreased to 0.7% and 1% respectively.

nal from pedestal, as ENC with 20 pF detector capacitor is 826 number of electrons which is about 7% of one MIP signal according to the simulation.

With this new baseline design of KUPID v2.0, we also simulated sample/hold and MUX with two channel preamplifier-shaper chain. Main designs for sample/hold and MUX are from reference [15].

In Fig. 35 schematic, left upper boxed area is for sample/hold, right upper square is for two channel MUX, and bottom square is reset for sample/hold. To make less

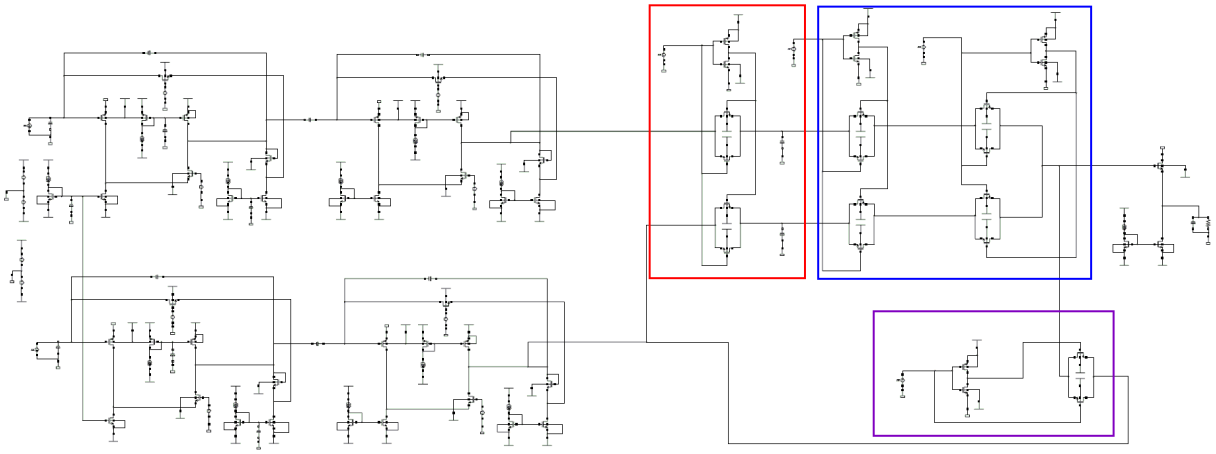

Figure 35: Schematic for KUPID v2.0 with sample/hold and multiplexer. The left upper boxed area is for sample/hold, right upper square is for two channel MUX, and bottom square is reset for sample/hold. In sample/hold design, 1 pF capacitor is inserted to charge the output signal from preamplifier-shaper.

MOSFET charge feed through error, size of MOSFET switches are designed very small, and each switch has there dummy transistor with inverter([16],[17]). And for optimized sample/hold signal, 1 pF capacitor is inserted to charge output signal from preamplifier-shaper.

In our simulation, 0.5 MIP, and one MIP signals are injected to each preamplifier-shaper channels. Fig. 36 shows the output signals from both 0.5 MIP, and one MIP injected preamplifier-shaper channels. You can confirm that the output signals are proportional to injected charge. When the output signal from preamplifier-shaper reaches to the peak point, sample/hold (red box in Fig. 35) captures the value and hold until reset sequence. Fig. 37 is the output signals from each sample/hold channels. And finally, two channel MUX serializes two sample/hold signals in order. In Fig. 38, MUX output shows that two channel signals which held by sample/hold are serialized from 2.5 μs to 3.0 μs, and 3.0 μs to 3.5 μs. As the reset switch for sample/hold closed in 3.5 μs for 0.1 μs, there are distorted signal around 3.5 μs in Fig. 36, 37, and 38. After confirming that two channel MUX operates well with KUPID v2.0, multi channel MUX (more than two channels) will be designed for the next version of KUPID.

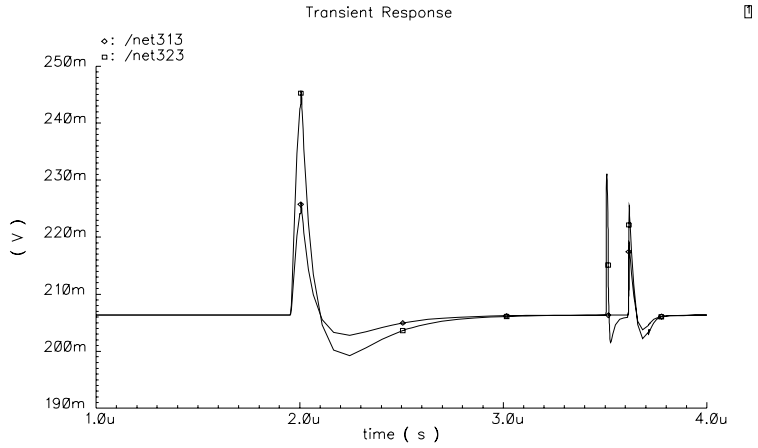

Figure 36: Two output signal from each KUPID v2.0 preamplifier-shaper channel. To net313 channel, 0.5 MIP charge injected for input signal while one MIP charge injected for net323 channel in 2.0 μs. Output signal from each channel are proportional to injected charge signal. Distorted signal around 3.5 μs is caused by reset switch for the sample/hold.

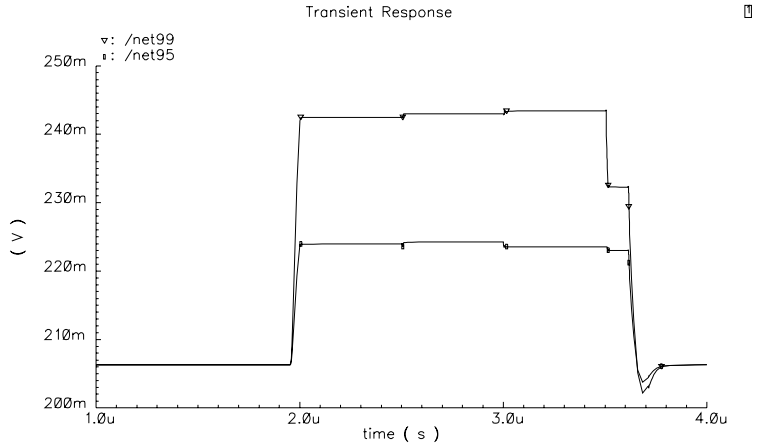

Figure 37: Two sample/hold signals for each channels. From 2.0 μs to 3.5 μs, net95 shows sample/hold signal for 0.5 MIP injected channel (bottom curve), and net99 shows for one MIP injected channel (top curve). Charged signal during hold sequence didn't change much as expected. Similar with Fig. 36, there are unexpected step signal around 3.5 μs caused by reset for sample/hold.

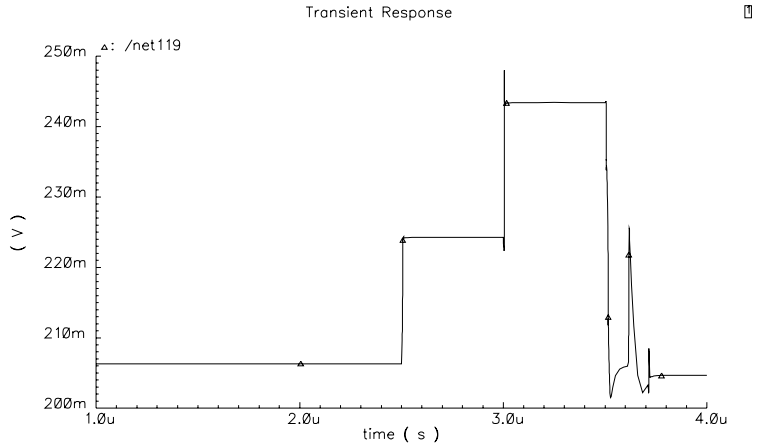

Figure 38: Two channel MUX output result. MUX serialized two parallel channel signal from sample/hold, 0.5 MIP signal channel output from 2.5 μs to 3.0 μs and one MIP signal channel output from 3.0 μs to 3.5 μs. Reset sequence affected the MUX output and result in distorted signal around 3.5 μs.

8.0 Conclusions

Throughout the simulation results and measurements from KUPID v1.0 and v2.0, we expect to obtain significantly better performance from KUPID v2.0 in both gain and noise. From our simulation results, KUPID v2.0's offset for ENC became approximately 0.7% and ENC slope for 1% compare with KUPID v1.0. And also, output gain for KUPID v2.0 is expected to increase 20 times bigger than v1.0. However, real measured performance for KUPID v2.0 might not be as much as simulation results, since KUPID v1.0 didn't show same ENC value with simulation and measurement. Even though the performance of produced KUPID v2.0 chip could be less than simulated results, we still look forward to obtaining better results than v1.0. KUPID v2.0 is scheduled to be submitted in winter 2008. We hope to obtain much improved performance from KUPID v2.0 in near future.

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