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# Trends in integrated circuit design for particle physics experiments

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**Abstract.** Integrated circuits are one of the key complex units available to designers of multichannel detector setups. A whole number of factors makes Application Specific Integrated Circuits (ASICs) valuable for Particle Physics and Astrophysics experiments. Among them the most important ones are: integration scale, low power dissipation, radiation tolerance. In order to make possible future experiments in the intensity, cosmic, and energy frontiers today ASICs should provide new level of functionality at a new set of constraints and trade-offs, like low-noise high-dynamic range amplification and pulse shaping, high-speed waveform sampling, low power digitization, fast digital data processing, serialization and data transmission. All integrated circuits, necessary for physical instrumentation, should be radiation tolerant at an earlier not reached level (hundreds of Mrad) of total ionizing dose and allow minute almost 3D assemblies. The paper is based on literary source analysis and presents an overview of the state of the art and trends in nowadays chip design, using partially own ASIC lab experience. That shows a next stage of using micro- and nanoelectronics in physical instrumentation.

## 1. Introduction

Integrated circuits are one of the key complex units available to designers of multichannel detector setups. Complexity of custom or Application Specific Integrated Circuits (ASICs) for particle physics experiments is strongly correlated with integration scale. According to Moore Law, the number of transistors in a chip (integrated circuit) roughly doubles every two years. As a result the scale gets smaller and transistor number increases at a regular pace to provide improvements in integrated circuit functionality and performance while decrease costs [1]. Now the interpretation of the law is not classical quantity of elements over space (area), but effective usage of the fixed space for increasing functionality. Thus if we refer to scaling as the reduction in cost (somehow) of the money/transistor on a chip, then surely several more generations of Moores Law are ahead of us [2].

According to forecast of the International technology roadmap for semiconductors (ITRS) [3], the main acting factors for further chip development or system integration challenges are: design productivity, power management, manufacturability, bandwidth, cooling. All integrated circuits, necessary for physical instrumentation, should be radiation tolerant at new earlier not reached level (hundreds of Mrad) of total ionizing dose and allow minute almost 3D assemblies [2, 4].



## 2. How could future systems in detector instrumentation look like?

Future systems should ideally:

- be based on hybrid technologies (at element, chip, package, board and finally system levels);
- have highly integrated very sensitive analog front-end;
- provide digitization of data at an earliest stage. Thus signal processing will be mostly in digital domain (DSP);
- have high data rates via output interfaces with a speed in the multi-Gb/s range;
- extract Big Data processing (for example, CMS detector raw data provides more than 1000 Pbyte/day (1 Mbyte x 40 MHz) [5]);
- not be cheaper than today [2].

## 3. ASIC development trends

The section lists the trends in ASIC development for particle physics as they may be viewed from a university ASIC design lab. These are:

- The increasing quantity of elements at a simultaneous increase in their complexity and density. Moore law is still valid and a further increase in integration scale is expected;
- Heterogeneous integration of ASICs and detectors (sensors) to be read out. The figure 1 shows diversification (variety) of today technologies [6];

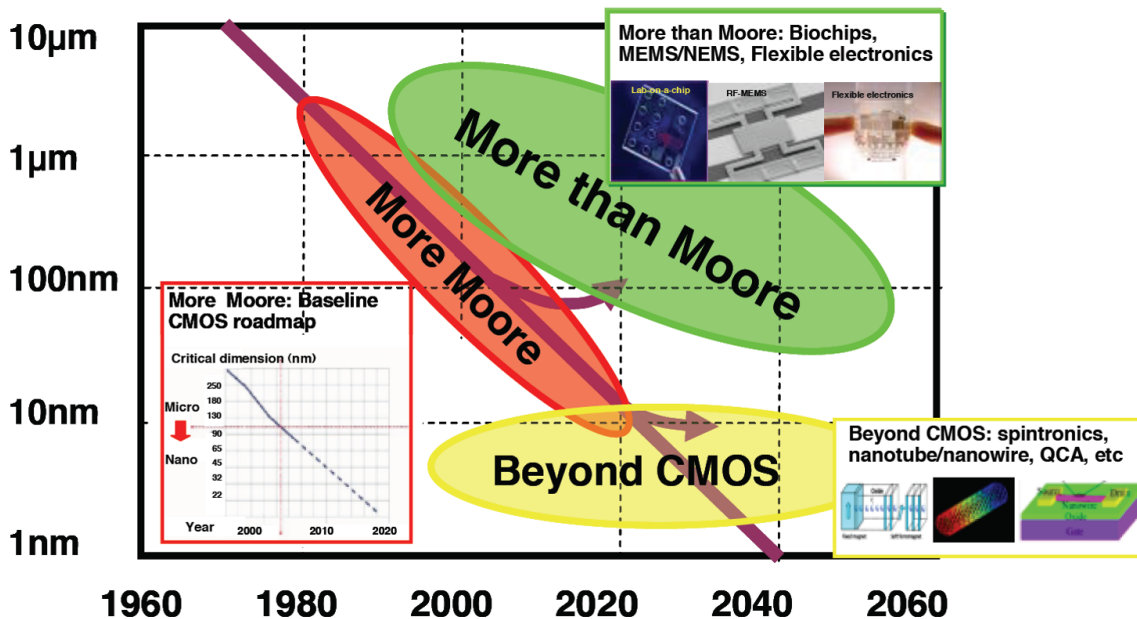


Figure 1. Diversification of technologies.

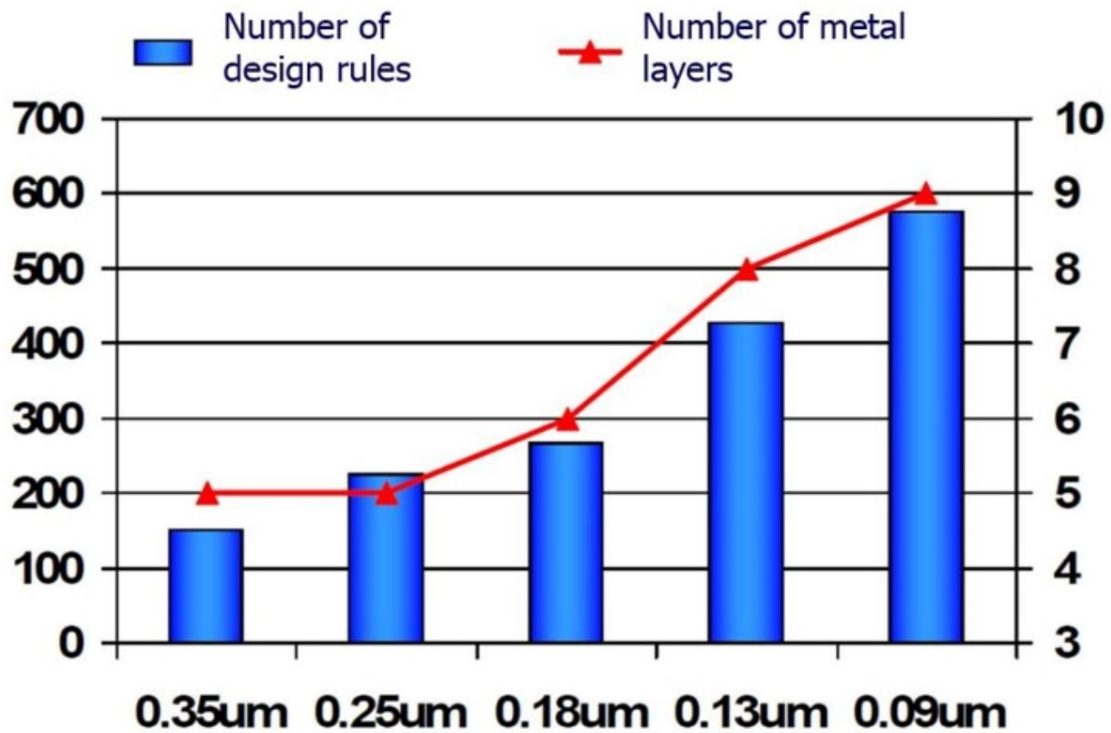
- Digital signal processing part more and more replaces the analog one. The 250 nm CMOS process provides 10 K gates/mm<sup>2</sup> allowing to place in the area of 100\*100 µm<sup>2</sup> a few registers only. Having shifted to the 28 nm process with density of 3900 K gates/mm<sup>2</sup> the designer can place a whole microprocessor in the same area. Thus the trend pushes the designer in the era of necessary minimum analog and analog-to-digital conversion design followed by programming all other almost unlimited functionality in digital domain;
- Design cost increases comparing to the one of manufacture;

- Design timeline and number of prototype cycles (respins) are necessary to be reduced to get more faster the final result;
- Technologies available today are well ahead of most requirements foreseen for the next generation experiments [2];
- For the majority of projects the minimum set of ASICs is to be developed in a one well verified technology (LHC – IBM 130 nm, SLHC – TSMC 130 and 65 nm, FAIR – UMC 180 nm). That is in fact a standardization trend. Technology choice is based on the necessity to use processes more and more advanced (with life time beyond 2020), but well characterized for design tools and having a reasonable cost;
- Extremely compressed timeline for each cycle (respin) of custom design (4-6 months);
- Start-to-finish (system level) design is necessary: Structural and behavioral modeling – Design of IP blocks at transistor level and that of systems at high-level language – Layout – Verification (ERC, DRC, LVS, PE, PS) – GDSII;
- Possibility of ASIC adaptation for other projects as criterion of economic efficiency, thus providing a universalization trend;
- Functionality increase at a limited power consumption budget;
- Increase in demand for a high technology (expensive) product. The accent at design is done at system (architectural) questions. ASICs as Systems On a Chip (SOCs) dictate a mixed-signal character of design route. Today almost all projects are mixed-signal one. For example, digital ASICs need an analog interface blocks, while analog chips are supplied by digital slow control or power saving functionality;
- The demanded number of ASIC wafers is small and can't interest a manufacturer. For example, if an experiment requires  $10^6$  channels, ASIC contains 100 channels per chip and one can get 1000 chips from each wafer, that results in 10 wafers only;
- Design is based on the usage of constantly and fastly advanced tools at all levels of design: Computer Aided Design (CAD) systems (Cadence, Mentor Graphics, Synopsys, Agilent and other), technological libraries or Design Kits (elements, standard digital and IP blocks), including design rules of manufacturer, the quantity of which quickly grows for advanced processes (for example, more than 2000 for 22 nm node). As shown in figure 2 there is a strong correlation between the number of design rules and layers for CMOS process. At the same time figure 3 shows that due to technology trend for shift from 2D to 3D space the complexity of element models grows quickly [8], demanding more and more powerful computing;
- Necessity of a fast and actually continuous retraining of experts as well as a skilled staff of young engineers (to support team competence level for experiment at least);
- Close integration of the design centers for both chip and system (hardware) levels.

#### 4. Trends for radiation-hardened ICs

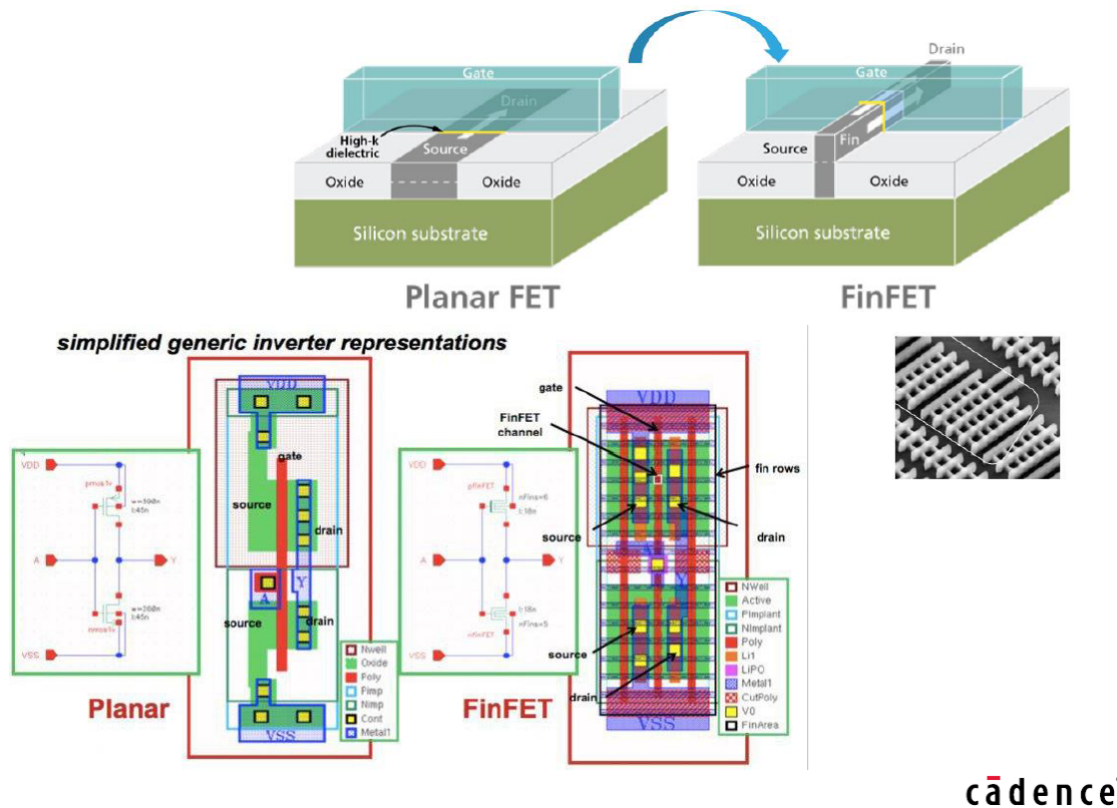
Among of trends for radiation tollerant or radiation hardened ICs one may list the following:

- Improvement of radiation hardness against total dose effects for new commercial CMOS processes. At the same time there is a wide spread of parameters among various manufacturers and no guarantee of long-term stability;
- Radiation-hardness processes lag behind commercial ones for 5-7 years (three generations according to Moore Law). As an example the figure 4 compare commercial and rad-hard CPUs in terms of throughput over years [6];



**Figure 2.** The number of design rules and layers for CMOS processes.

- Radiation hardening of modern ASICs is provided by a wider usage of commercial CMOS processes and a refinement of different methods and means, used at early design stages (*rad-hard by design methodology*);
- Radiation-hard technologies themselves are not economically efficient. For them there exists only a small volume of orders;
- Designer experience allows to carry out only a correct choice of the manufacturer, who can provide specific target requirements;
- Active investigation of radiation effects for new bulk CMOS technologies and their compiling into the standard of design rules and CAD tools (Calibre, Assura, PVS, etc.) both at element and behavioral levels;
- A number of rad-hard applications will demand the design of rad-hard components and their manufacture in a radiation hardened technology to meet rigid requirements. The part of such ASICs will decrease each year;
- Continuous improvement of very complex rad-hard systems will critically depend on the introduction of commercialized micro- and nanoelectronic innovations in these systems;
- Raising the ultimate complexity of these systems to the level, reached in commercial technologies, will demand a shift of many projects in the direction of creating radiation-tolerant components, using traditional commercial technologies, applying the methods of maintaining an acceptable radiation hardness. An actual task is the analytical comparison of technologies by the radiation hardness:
  - (i) Industrial (commercial) CMOS technology with use of "rad-hard-by-design" methods,
  - (ii) Rad-hardened technology, according to the Moore law, lags more than 3 generations behind the commercial CMOS one.



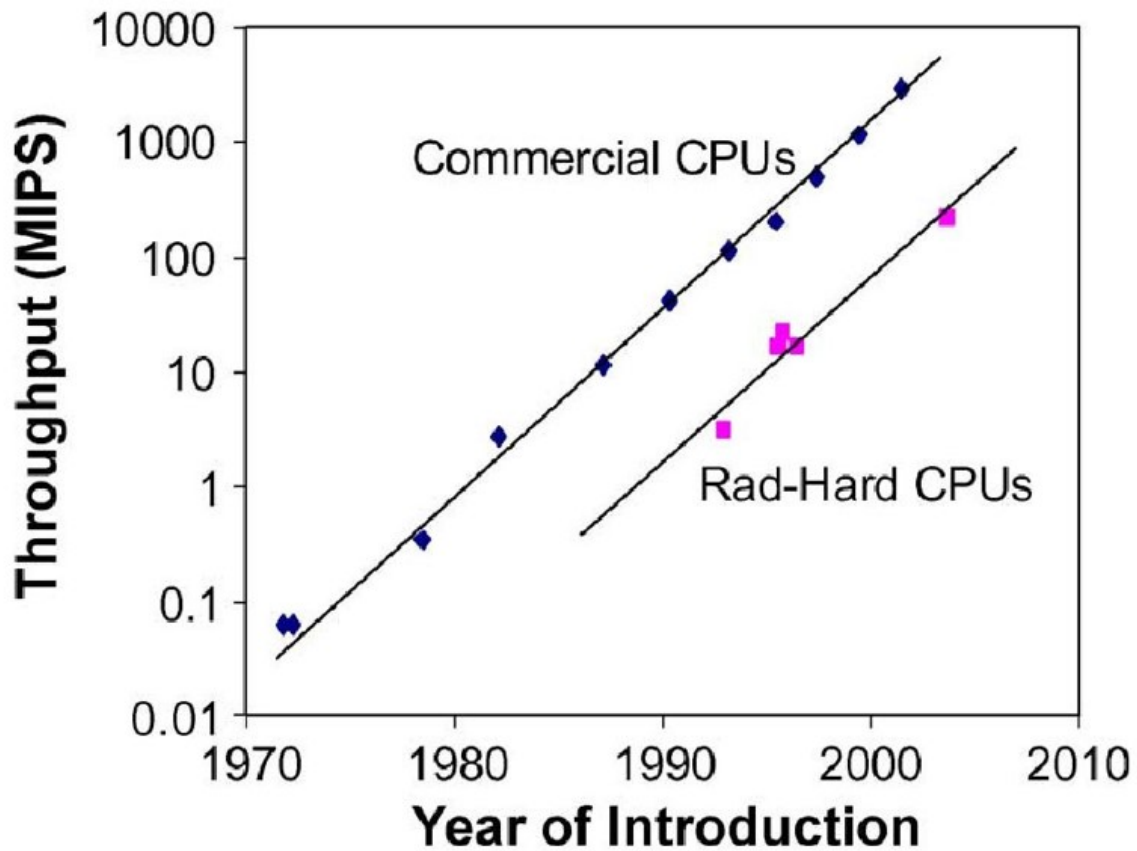
**Figure 3.** Complexity transistor models grows due to shift to 3D technology.

For example, further presented is the practical dilemma. What is better: either a rad-hard 350 nm process (for example, silicon-on-insulator) or a bulk CMOS 130 (90) nm process? The latter is better also in terms of economics.

- Traditional methods for radiation hardening are: 1) Circuitual (reservation, redundancy, coding, adaptive biasing and so on); 2) Layout ones (guard rings, ring transistors, and so on); 3) Technological (low volume CMOS, SOI, trench isolation, and so on). The required rad-hardness level is provided by a semiconductor structure choice and use of the special technological processes.
- Rad-hard by design concept consists in the following:
  - (i) Refinement of traditional non- rad hard libraries for computer aided design (CAD);
  - (ii) Elaboration of additional design rules, improving rad-hardness at the following 3 levels of design:
    - (a) Transistor level,
    - (b) Level of cells, gates and IP blocks,
    - (c) System level;
  - (iii) Creation of calibrated test structures and expansion of the scaled element libraries;
  - (iv) Monitoring and statistical analysis of the ASIC rad-hard stability, provided at manufacture;
  - (v) Rad-hard tests of chips at both passive and active work modes.

### 5. Phases of ASIC development

One can recognize five phases in the ASIC development. These are:



**Figure 4.** Throughput of commercial and rad-hard CPUs.

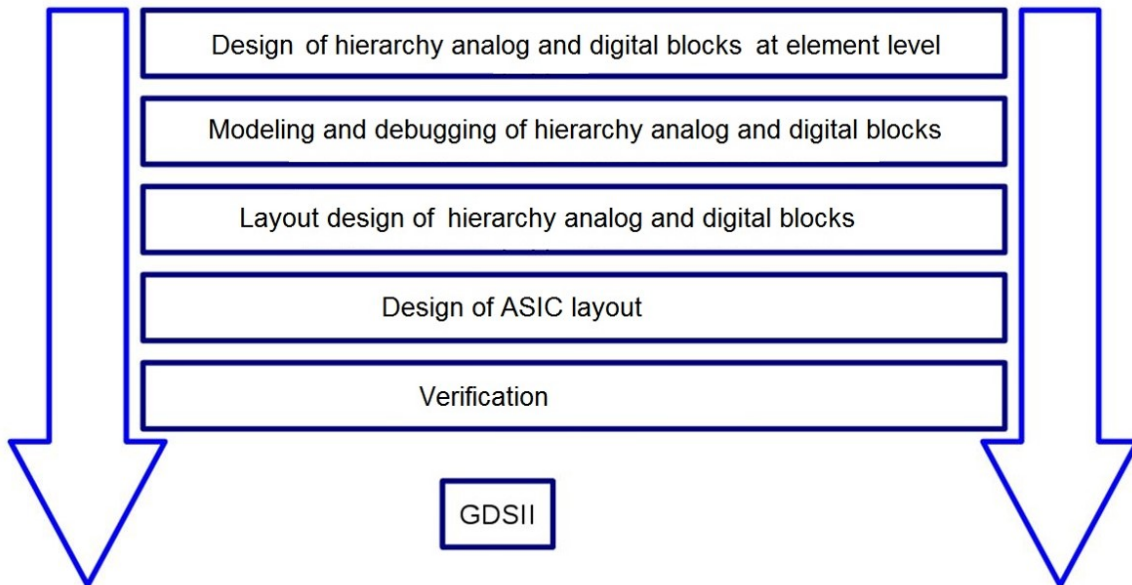
- Phase I: CAD based design of ASICs;
- Phase II: Prototyping and test technique development;
- Phase III: First tests and prototype characterization;
- Phase IV: Qualification of ASICs;
- Phase V: Preparation for a batch (engineering) production and testing automation.

The most known traditional route used for ASIC design is *bottom-to-top* one. The block diagram of the route is shown in figure 5.

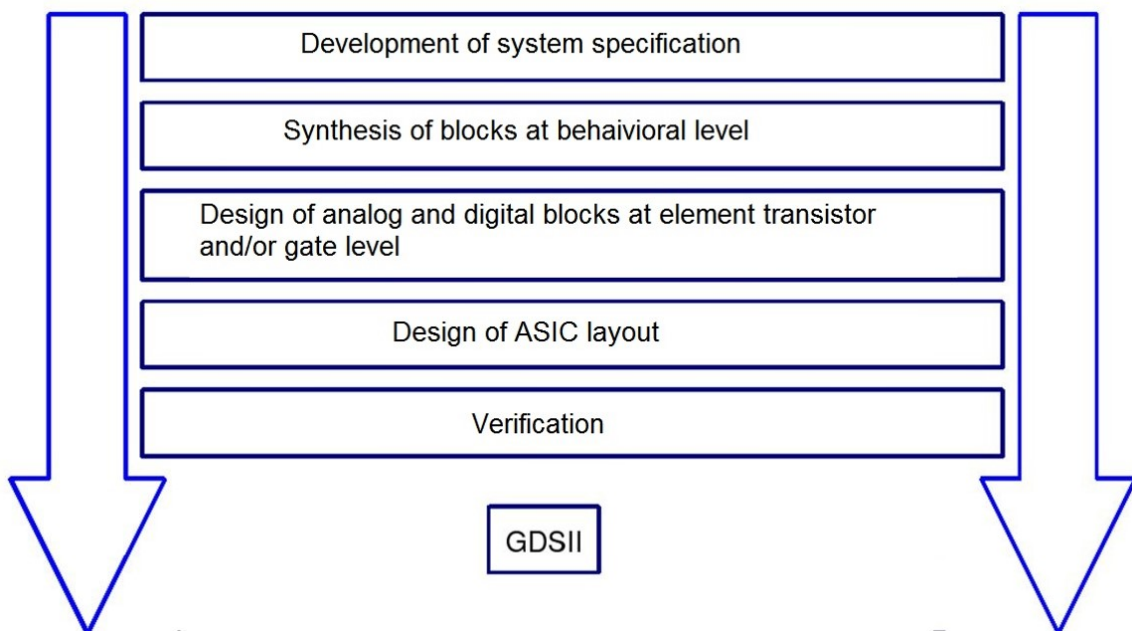
It consists in consequent development of all building (*bottom*) blocks, followed by their integration in system (building a *top* level of design). Feature of this approach to design is a possibility to perform a mixed-signal simulation for analysis of blocks interaction appears only after the all separate blocks being ready.

A more advanced alternative for ASIC design is a route *top-to-bottom*. Its conceptual block diagram is shown in figure 6.

Main feature of the top-to-bottom route is the usage of mixed-signal simulations for whole system (chip, ASIC) at early stage. Due to system synthesis at structure level, it becomes possible to develop fastly the block descriptions at behavioral level, that is RTL-Verilog, Verilog-A Verilog-AMS. The same level of abstraction is available with VHDL. Further efforts of chip designer allow to use the different levels of abstraction for system building blocks (along their design) making more precise simulation results and finally shortening the design.



**Figure 5.** Traditional *bottom-to-top* design flow.



**Figure 6.** *Top-to-bottom* design flow.

## 6. General principles of mixed-signal design

Among trends on the general principles of ASIC design one can list the following:

- Modern ASICs, as a rule, are mixed-signal chips. They surely include both analog and digital parts;
- Analog part is designed as a custom (application specific) block, whereas the digital one is described by VHDL or Verilog and then synthesized as a semicustom block, based on

standard digital cell libraries;

- Now a system simulation at element (transistor) level requires an unacceptable lot of time. Usage of high description languages and software tools for hierarchy design allows to perform simulation with different abstraction level of blocks.
- Traditional design routes use the mixture of CAD tools, issued by different known suppliers, supplementing each other in functionality of both analog and digital design routes.

## 7. Conclusions

The future of instrumentation is tightly bound with a wide usage of ASICs due to the new challenge in integration scale. Commercial technologies available today are well ahead of most requirements foreseen for particle physics' ASICs. The solution of system (architectural, structural) problems will demand substantially higher efforts to create not only separate components, but whole systems on chip (SoC). Almost all new chips have a mixed-signal character.

Nowadays the design is based on microelectronic CAD tools of different suppliers and the adapted Design Kits of the chosen manufacturer. Reduction of timelines for design, extension of reusable IP block libraries, new level of system tests for readout electronics all of that requires the usage of advanced CAD in distributed fast networks of powerful computing clusters.

New projects more and more require a tight collaborative work of expanding team and accurate sharing all design infrastructure (computing clusters, CAD tools etc). The necessity of much stronger collaboration and coordination between all participants, sharing: the process of preparing human resources; the cost of expensive CAD and chip prototyping as well as updating existing design competences.

The "rad-hard by design" approach for commercial CMOS technology is considered to be the best way of providing an acceptable rad-hardness by circuitual and layout techniques. For radiation hardness, temperature stability and reliability of the chips it is important to refine the existing libraries and design routes.

Long term planning becomes an extremely important factor, especially taking into account the "life time" of both the chosen technology and the design staff.

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