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TCAD analysis of conditions for DIBL parameter misestimation in cryogenic MOSFETs

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The study aimed to theoretically investigate the transfer characteristics of MOSFETs at cryogenic temperatures to elucidate the experimental conditions affecting the accurate estimation of the drain-induced barrier lowering (DIBL) parameter. Our Technology Computer Aided Design (TCAD) simulation revealed that MOSFETs featuring an underlap between the gate and source/drain edges experience a significant shift in threshold voltage (V_t) in the low drain voltage (V_d) region, which causes the misestimation of the DIBL parameter. This V_t change is due to a notable increase in carrier concentration within the underlap region. To mitigate misestimation in such underlap devices, confirming the dependence of the DIBL parameter on the linear region of V_d serves as an effective method to ensure accurate estimation.

1. Introduction

Recently, quantum computers have garnered attention for their ability to solve practically significant problems that are challenging for classical computers. The quantum bit (qubit), which is the building block of quantum computer hardware, can be implemented in several ways.[1–6] Notably, there are high expectations for superconductor[1] and semiconductor[2–4] qubits, particularly concerning large-scale integration. Currently, these qubits are housed within dilution refrigerators. However, commercial electronic devices are used to control the qubits and are installed at RT. These electronic devices connect to qubits through numerous wiring cables. As the number of integrated qubits increases, so does the number of wiring cables, leading to a large amount of heat inflow from the RT stage to the cryogenic stage via the wiring cables. This influx of heat raises the temperature of the refrigerator system, thereby impeding qubit operation.

One proposed solution to this problem is the utilization of CMOS integrated circuits for qubit control at the cryogenic stage.[7] This approach aims to minimize the number of wiring cables between the RT and cryogenic stages. Such integrated circuit and device technology, called cryo-CMOS, is currently undergoing intensive research and development.[8–11] To realize cryo-CMOS circuits, a thorough understanding of MOSFET characteristics at cryogenic temperatures is essential for effective circuit design. Recent studies have identified various behaviors of MOSFET characteristics during cryogenic operations that cannot be explained by conventional theoretical models.[12–15] Efforts are underway to elucidate these behaviors.

This paper focuses on one of the fundamental phenomena in short-channel MOSFETs, known as drain-induced barrier lowering (DIBL), wherein the threshold voltage (V_t) decreases as the channel potential decreases due to the drain bias voltage (V_d).[16] This phenomenon is experimentally evaluated by the DIBL parameter, which represents the difference in V_t between the linear and saturated regions.

The DIBL parameter is defined as the decrease in $|V_t|$ with an increase in $|V_d|$. Several reports indicate an increase in the DIBL parameter at cryogenic temperatures compared to RT operation.[17–23] Conversely, some studies have reported a decrease in DIBL parameters at cryogenic temperatures.[22–26] Therefore, the understanding of DIBL parameters at cryogenic temperatures remains unclear based on these experimental reports.

In a previous study, we reported experimental results demonstrating an anomalous increase in the DIBL parameters at cryogenic temperatures in MOSFETs with an underlap between the gate and source/drain.[27] Our findings revealed that the anomalous increase in the DIBL parameters is because of an anomalous increase in $|V_t|$ due to carrier depletion in the underlap region during the linear region at cryogenic temperatures. Notably, this anomalous increase in $|V_t|$ was not observed at RT in such MOSFETs. Indeed, the negligible underlap at RT causes a problem at cryogenic temperatures. This $|V_t|$ increase originates from a different reason than the conventional DIBL mechanism. Consequently, this result suggests that the experimental DIBL parameters could be incorrectly evaluated for MOSFETs with a gate-source/drain underlap.

The purpose of this paper is to elucidate the experimental conditions leading to misestimation of DIBL parameters and to explore strategies for avoiding such misestimation in devices possessing the gate-source/drain underlap structure. Device simulations were performed to investigate the transfer characteristics of underlap MOSFETs at cryogenic temperatures, with a focus on the dependence on drain voltage.

2. Methods

The schematic of the device structure used for simulation is shown in Fig. 1. The device width (W) was 1 μm, and the gate length (L_g) was 100 nm. We determined the dopant concentration for each part based on the dopant profile in the devices using extension/halo technology.[27] Following our previous study reporting the anomalous V_t increase,[27] this

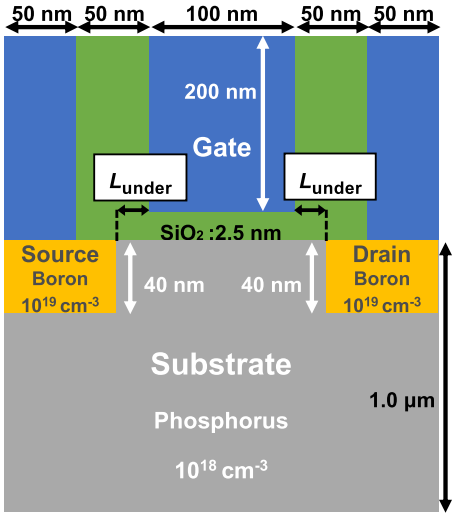

Fig. 1. Schematic device structure of p-MOSFET used in the simulation. We assumed short-channel MOSFETs taking advantage of extension/halo technology to suppress short-channel effects.

paper focused on the p-channel MOSFET (PMOS). Note that the anomalous V_t increase occurrence depends on the underlap design and dopant concentration, regardless of the type of MOSFETs. Hence, the misestimation of DIBL parameters discussed in the following could potentially occur not only in PMOS but also in n-channel MOSFETs (NMOS). The underlap length (L_{under}) was defined as the gap length between the gate edge and the source/drain regions. The work functions of the metal electrodes for the gate, source, and drain were set at 5.2 eV.

We performed Technology Computer Aided Design (TCAD) simulation by using our in-house device simulator (Impulse TCAD).[28] Regarding the simulation method at cryogenic temperatures, we employed the drift-diffusion model based on the generalized Einstein relation corresponding to the Fermi–Dirac distribution, expressed by the following equation:[29]

$$qD_n = \mu_n kT \frac{F_{1/2}((E_{Fn} - E_c)/kT)}{F_{-1/2}((E_{Fn} - E_c)/kT)}, \quad (1a)$$

$$qD_p = \mu_p kT \frac{F_{1/2}((E_v - E_{Fp})/kT)}{F_{-1/2}((E_v - E_{Fp})/kT)}. \quad (1b)$$

Here, q represents the elementary charge, D_n (D_p) is the diffusion coefficient for electron (hole), μ_n (μ_p) is the mobility for electron (hole), E_{Fn} (E_{Fp}) is the quasi Fermi energy for electron (hole), E_c (E_v) is the conduction (valence) band energy, k is the Boltzmann constant, T is the temperature, and ψ is the potential. F_j denotes the Fermi integral of order j, given by:

$$F_j(\eta) = \frac{1}{\Gamma(j+1)} \int_0^\infty dx \frac{x^j}{\exp(x - \eta) + 1}, \quad (2)$$

where Γ is the gamma function. We can more accurately simulate the carrier depletion at cryogenic temperatures by properly treating the Fermi–Dirac distribution. Additionally, we employed the model and parameters for the incomplete ionization of dopants described by the following equations:[30,31]

$$\frac{N_D^+}{N_D} = 1 - \frac{b}{1 + g \bullet \exp[-(E_{F_n} + E_{dop} - E_c)/kT]}, \quad (3a)$$

$$\frac{N_A^-}{N_A} = 1 - \frac{b}{1 + g \bullet \exp[-(E_{F_p} + E_{dop} + E_v)/kT]}, \quad (3b)$$

where N_D^+ and N_A^- are the concentrations of ionized donors and acceptors, respectively, N_D and N_A are the concentrations of donors and acceptors, respectively, g is the degeneracy factor, and E_{dop} is the peak of the concentration of states of the dopants. b is the function of dopant concentration N_{dop}, and is expressed by the following equation:

$$b = \frac{1}{1 + (N_{dop}/N_b)^d}, \quad (4)$$

where N_{dop}, N_b and d are the fitting parameters utilized to replicate the experimental concentration of states reflecting the metal-insulator transition under highly doped conditions.[30,31]

Using the above method, we simulated the drain current (I_d) versus gate voltage (V_g) characteristics for various drain voltage conditions at cryogenic temperature. V_t was calculated based on the constant-current method and defined as the gate voltage at which $I_d \times L_g/W = 10$ nA.[27]

3. Results and discussion

We initiated our investigation by replicating the anomalous increase in DIBL at cryogenic temperatures, as observed in our previous experimental studies.[27] First, we investigated the condition of the L_{under}, which is responsible for the anomalous increase of $|V_t|$. Figure 2 shows the simulated $|V_t|$ as a function of L_{under} at certain temperatures and V_d conditions. $|V_t|$ increased slowly with increasing L_{under} at 300 K, while an anomalous increase in $|V_t|$ is observed at 15 K for devices with $L_{under} > 12$ nm. This anomalous increase is solely observed at cryogenic temperatures. In Fig. 2, the difference between the solid red and dashed yellow lines corresponds to the DIBL parameters at 15 K. For devices with $L_{under} > 12$ nm, the DIBL parameter increased. Additionally, it is observable that $|V_t|$ experiences a significant increase when $|V_d| = 50$ mV (linear region). The $|V_t|$ increase in the saturation region ($|V_d| = 1.0$ V) was negligible. To elucidate the difference in the $|V_t|$ behavior between the linear and saturation regions, we analyzed the carrier

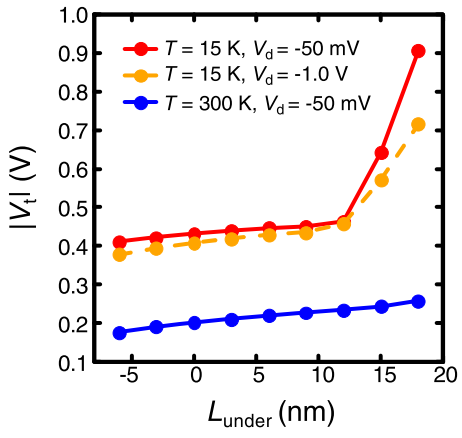

Fig. 2. Summary of $|V_t|$ depending on L_{under}, which is the gap between the gate and source/drain edges, at 15 K and 300 K.

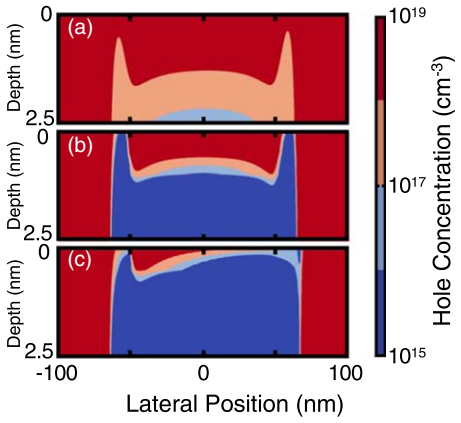

Fig. 3. Contour plots of hole concentration in silicon layer near the gate surface for three cases: (a) at 300 K and $|V_d| = 50$ mV, (b) at 15 K and $|V_d| = 50$ mV, and (c) at 15 K and $|V_d| = 1.0$ V. Device is with $L_{under} = 15$ nm. The V_g is set at −0.63 V. Gray dotted lines are eye guides for position of the gate edges.

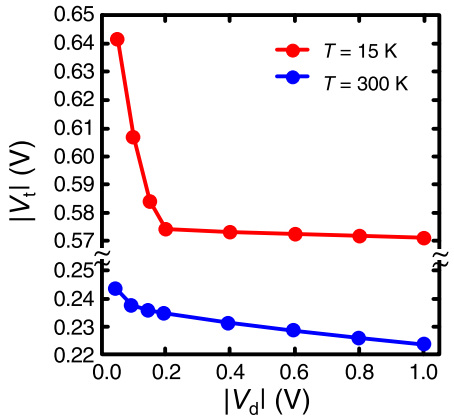

Fig. 5. $|V_d|$-dependent $|V_t|$ at 15 and 300 K.

distribution for a device with $L_{under} = 15$ nm. Figures 3(a) and 3(b) show contour plots of the hole concentration near the top surface of the substrate for $|V_d| = 50$ mV and $|V_g| = 0.63$ V at 300 K and 15 K, respectively. At 300 K, the channel region between the source and drain is electrically connected by holes with a sufficiently high concentration because of the inversion. However, at 15 K, the hole concentration significantly drops in the underlap region, resulting in the disconnection of the channel. The increase in channel resistance due to this disconnection causes an anomalous increase in $|V_t|$ at cryogenic temperatures. Figure 3(c) shows the contour plot of the hole concentration near the substrate surface at 15 K in the saturation region, $|V_d| = 1.0$ V. In contrast to Fig. 3(b), the hole concentration in the underlap region recovers as $|V_d|$ increases, and the channel weakly reconnects. This mitigates the increase in $|V_t|$ compared to that in the linear region.

Subsequently, we investigated the V_d dependence of the V_t to comprehend the behavior of DIBL parameters at cryogenic temperatures. Hereafter, we focus on the device with $L_{under} = 15$ nm that exhibits the anomalous $|V_t|$ increase. Figure 4 shows the V_d dependence of the transfer characteristics at 15 and 300 K. The value of V_d varied in the range of −50 mV to −1.0 V. This figure indicates that the transfer characteristics at 15 K significantly change depending on the value of V_d. Figure 5 summarizes the V_t shift as a function of V_d at 15 and 300 K. At 300 K, $|V_t|$ decreases linearly with increasing $|V_d|$ over the range from $|V_d| = 100$ mV to $|V_d| = 1.0$ V. Conversely, at 15 K, $|V_t|$ decreases rapidly from 50 mV to 0.2 V, after which $|V_t|$ decreases slightly from 0.2 to 1.0 V.

Now, let us discuss the features of DIBL parameters at cryogenic temperatures. In general, DIBL is defined as the difference in $|V_t|$ between the low $|V_d|$ condition ($V_{d\text{-low}}$) corresponding to the linear region and the high $|V_d|$ condition ($V_{d\text{-high}}$) corresponding to the saturation region. At 300 K, $|V_t|$ decreases as $|V_d|$ increases, aligning with the conventional behavior of DIBL. At 15 K, an anomalous increase in $|V_t|$ due to carrier depletion in the underlap region was observed in the voltage range below 0.2 V. In this scenario, choosing a $V_{d\text{-low}}$ smaller than 0.2 V for estimating the DIBL parameter could lead to misestimation. Additionally, we note that the change in $|V_t|$ from 0.2 to 1.0 V at 15 K is smaller than that at 300 K. This suggests that the DIBL parameter at cryogenic temperatures inherently tends to be smaller than that at RT, indicating that the DIBL phenomenon is less pronounced at cryogenic temperatures than at RT. The effect of underlap on V_t, representing an additional unexpected factor, affects the estimation of the DIBL parameter, especially at cryogenic temperatures.

Based on the preceding discussion, we propose a method to verify the correctness of estimated DIBL parameters in experiments, aiming to avoid misestimation. Figure 6 shows the $V_{d\text{-low}}$ dependence of the DIBL parameters. Here, the

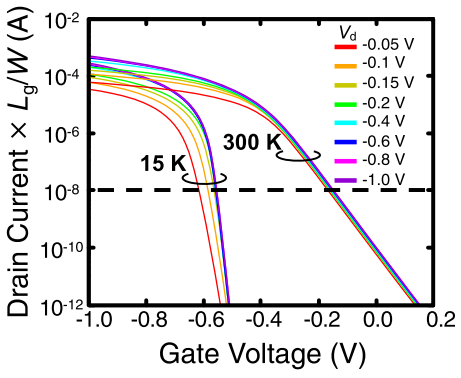

Fig. 4. I_d–V_g characteristics for device with $L_{under} = 15$ nm at 15 K and 300 K. $|V_d|$ was varied from 50 mV to 1 V.

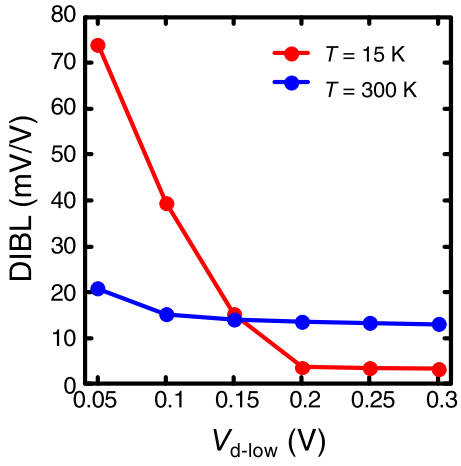

Fig. 6. Summary of extracted DIBL parameters depending on $V_{d\text{-low}}$ (V_d for linear region side). V_d for saturation region side is fixed at 1.0 V.

DIBL parameters are defined as follows:

$$\mathrm{DIBL} = \frac{|V_t(|V_d| = V_{d-high}) - V_t(|V_d| = V_{d-low})|}{(1.0 - V_{d-low})}, \quad (5)$$

where $V_{d\text{-high}}$ is set to 1.0 V.

The figure indicates that misestimation of the DIBL parameter occurs under cases $V_{d\text{-low}} < 0.2$ V at cryogenic temperatures. However, for $V_{d\text{-low}} > 0.2$ V, the DIBL parameter appears to be estimated correctly. Therefore, confirming the $V_{d\text{-low}}$ dependence of the DIBL parameter in experiments would be an effective method to mitigate misestimation. It is important to note that these discussions suggest that the discrepant temperature dependence of the DIBL parameter in previous experimental reports, as mentioned in the introduction, could be attributed to the existence of gate-source/drain underlap and the choice of $V_{d\text{-low}}$.

To gain further insight into the unique V_d dependence of V_t in the presence of an underlap at cryogenic temperatures, we examine the I_d–V_d characteristics (Fig. 7). Here, V_g is fixed to V_t at $V_d = -50$ mV. This curve deviates from the conventional I_d–V_d characteristics of MOSFETs. The magnitude of $|I_d|$ increases rapidly in the low $|V_d|$ range of 0–0.2 V and then slowly increases in $|V_d| > 0.2$ V. This indicates the existence of nonlinear resistance. We investigated this by analyzing the distribution of potential and carrier concentrations.

Figure 8 shows the potential and hole concentration along the substrate surface in the low $|V_d|$ range of 0–0.2 V. A significant potential barrier leads to carrier depletion in the underlying region. However, the potential barrier becomes smaller as the $|V_d|$ increases and the hole concentration increases in the underlap region. This occurs due to the strong electric field in the underlap region, resulting from the electric field screening by the channel region with a high carrier concentration. Consequently, a steep $|I_d|$ increase accompanies the rise in hole concentration in the underlap region within the low $|V_d|$ range of the I_d–V_d curve. Figure 9 shows the potential and hole concentrations along the substrate surface in the high $|V_d|$ range of 0.2–1.0 V. Within this range, the hole concentration is sufficient for efficient conduction, and the channel between the source and drain is electrically connected. As a result, the channel potential is influenced by the drain bias, akin to the conventional DIBL phenomenon. This nonlinear resistance, stemming from carrier depletion in the underlap region, leads to an anomalous $|V_t|$ increase in the low $|V_d|$ range discussed in this paper. It is worth noting that similar characteristics have been reported in recent experiments with planar MOSFETs.[32)]

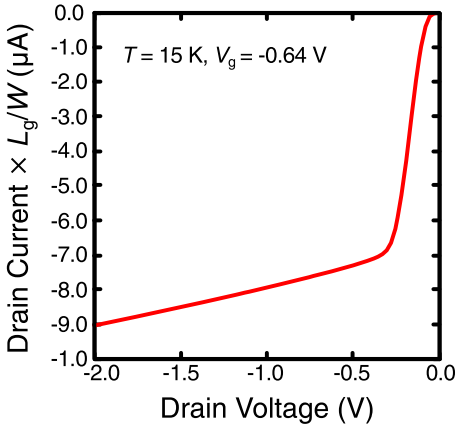

Fig. 7. I_d–V_d curve at 15 K. V_g is equal to V_t.

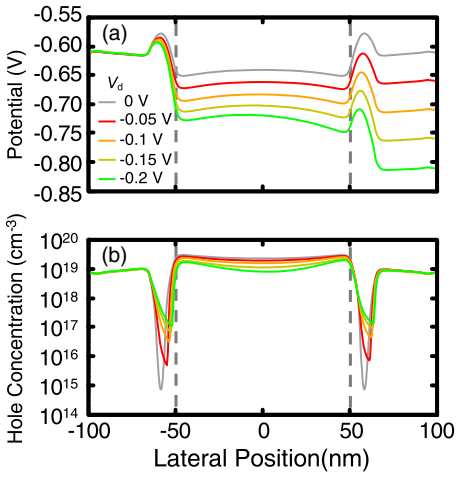

Fig. 8. (a) Potential and (b) hole concentration at gate surface in case of low $|V_d|$ in the range of 0–0.2 V. Gray dotted lines represent edges of the gate.

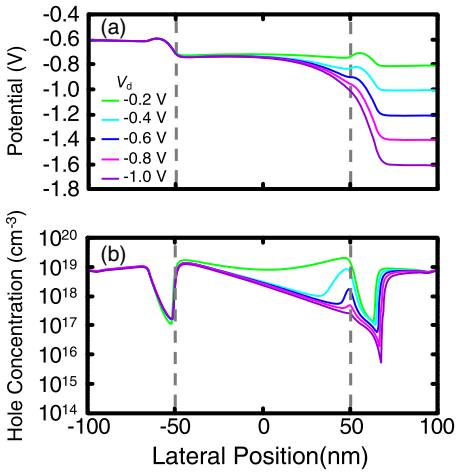

Fig. 9. (a) Potential and (b) hole concentration at gate surface in case of high $|V_d|$ in the range of 0.2–1.0 V. Gray dotted lines represent edges of the gate.

4. Conclusions

We investigated cryogenic I_d–V_g characteristics of bulk PMOS devices by using TCAD simulations, to clarify the experimental conditions leading to misestimation of DIBL parameters and to propose a method to avoid such misestimation in experiments. Misestimation of DIBL parameters at cryogenic temperatures may occur in devices with gate-source/drain underlap because $|V_t|$ undergoes significant changes in the low $|V_d|$ region as $|V_d|$ increases. This variation in $|V_t|$ stems from a notable increase in the carrier concentration in the underlap region with an increase in the $|V_d|$. We showed that the measurement of the $V_{d\text{-low}}$ dependence of the DIBL parameters is an effective method to avoid the misestimation of the DIBL parameter.

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