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# Characterization of the Beetle-1.0 Front End Chip

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**Abstract**

The *Beetle* is a candidate front end chip for the readout of the LHCb vertex detector. Here development and initial performance are described up to the first version *Beetle1.0* of the complete chip.

# 1 Introduction

A radiation hard front end chip for the LHCb vertex detector has to handle analogue information from silicon strip detectors. The data have to be sampled with the LHC bunch crossing frequency into an analogue pipeline with a maximum latency of 4 $\mu$s. To accomplish a dead-time free readout for triggered events at an average rate of 1 MHz, data from one event have to be brought off-chip within 900 ns. In addition, to buffer the natural fluctuations in the trigger rate, a multi-event buffer with a depth of 16 is needed. Details of the specifications can be found in [1].

The design of the chip started in late 1998 with the development of first prototype components. Two test chips containing different sets of analogue input stages with different shaping times and noise behavior, current and voltage digital-to-analogue converters (DACs) as well as different types of current sources have been submitted in May 1999. After successful tests of these prototype components a first version of the complete readout chip, *Beetle1.0*, was assembled and sent for fabrication in April 2000, together with three additional test chips containing components which have not been submitted before. Table (1) summarizes the development steps towards the *Beetle1.0*.

| name | functionality |
|---|---|
| *BeetleFE1.0* | 3 different sets of analogue input stages with different shaping times and noise behavior |
| *BeetleBG1.0* | 10 bit current and voltage DACs, 3 different types of current source |
| *BeetleCO1.0* | front end comparators, current buffer |
| *BeetlePA1.0* | pipeline, pipeline readout amplifier, $I^2C$-interface |
| *BeetleMA1.0* | 3 different sets of analogue input stages for the readout of multi anode photomultiplier tubes |

Table 1: *Test chips in the development towards the* Beetle1.0. *The first two chips were submitted in May 1999, the others in April 2000. All were realized on a die size of* $2 \times 2$ $mm^2$.

# 2 Chip Architecture

Here an overview of the general characteristics of the *Beetle* chip is given. Specific features of actual realizations are then discussed below for the various test chips and the current version 1.0 of the complete chip.

The *Beetle* can be operated as analogue or alternatively as binary pipelined readout chip. It implements the basic RD20 front end electronics architecture [2]. Figure (1) shows a schematic block diagram of the chip.

The chip integrates 128 channels. Each channel consists of a low-noise charge-sensitive preamplifier and an active RC-CR pulse shaper. The required rise time of the shaped pulse is $\leq 25$ ns, the spill-over left 25 ns after the peak at most 30%. A comparator per channel provides a binary signal. It features a configurable polarity and an individual threshold level. Four adjacent comparator channels are ORed together, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signal (LVDS) ports at 80 MHz. Either the shaper- or the comparator output is sampled with the LHC bunch-crossing frequency of 40 MHz into an analogue pipeline with a programmable maximum latency of 160 sampling intervals and an integrated multi-event buffer of 16 stages. Charge stored in the pipeline is transferred to the multiplexer via a resettable charge-sensitive amplifier. Within a readout time of 900 ns current drivers bring the serialized data off chip. The output of a dummy channel is subtracted from the analogue data to compensate common mode effects. All amplifier stages are biased by forced currents. On-chip digital-to-analogue converters (DACs) with 10 bit resolution generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height is implemented for each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard $I^2C$-interface. All digital control and data signals, except those for the $I^2C$-ports, are routed via LVDS ports.

The chip is fabricated in 0.25 $\mu$m standard CMOS technology and has a die size of $6.1 \times 5.5$ $mm^2$. The analogue input pads have a pitch of 41.2 $\mu$m. If no comparator outputs are required, pads on the sides of the chip need not to be bonded. This allows an overall pitch of 50 $\mu$m

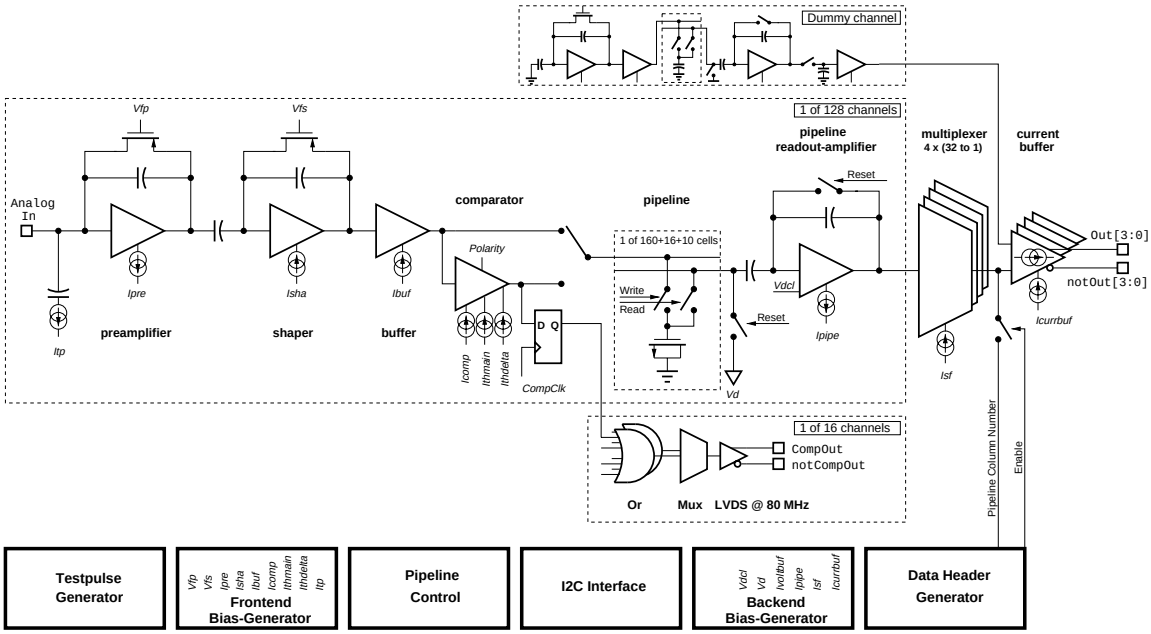


Figure 1: *Schematic block diagram of the* Beetle *readout chip.*

when mounting the chips side by side.

The gate oxide thickness of approximately 60 Å of the chosen 0.25 $\mu$m process already reduces the threshold voltage shift under irradiation. In addition several design measures have been taken to achieve the required radiation hardness [3]. Enclosed gate structures for NMOS transistors have been used to suppress an increase in leakage current under irradiation. A consistent use of guard rings should minimize the rate of single event effects [4]. Forced bias currents are used in all analogue stages instead of fixed node voltages.

# 3 Testchips for Frontend and Biasgenerator

The frontend chip *BeetleFE1.0* [5] contains three different sets of a prototype input stage. Each of the three sets consists of four identical channels. The amplifier channels consist of a charge-sensitive preamplifier, an active CR-RC shaper and a source follower as a buffer. Preamplifier and shaper use the well established folded cascode configuration. Two of the implemented sets use a PMOS transistor as input device, whereas the third one uses a NMOS transistor.

Figure (2) compares the simulation of the transient response of the fastest frontend to an input signal of 11,000 electrons at a capacitive input load of 10 pF to the actual measurement. Both are in good agreement. The equivalent noise charge (ENC) at this setup has been measured to be 303 $e^-$ + 33.6 $e^-$/pF at a bias current of 600 $\mu$A. A higher offset but reduced slope was seen with different setting [6]. The total power consumption of the frontend is 1.88 mW/channel.

The bias generator chip *BeetleBG1.0* [5] contains three different types of current sources, a voltage DAC, a current DAC and test structures that have been used to study the behaviour of several transistor parameters like threshold voltage, leakage current and transconductance under irradiation. The three different types of current sources vary with complexity and performance. One current source uses an operation-amplifier feedback. The second one also uses

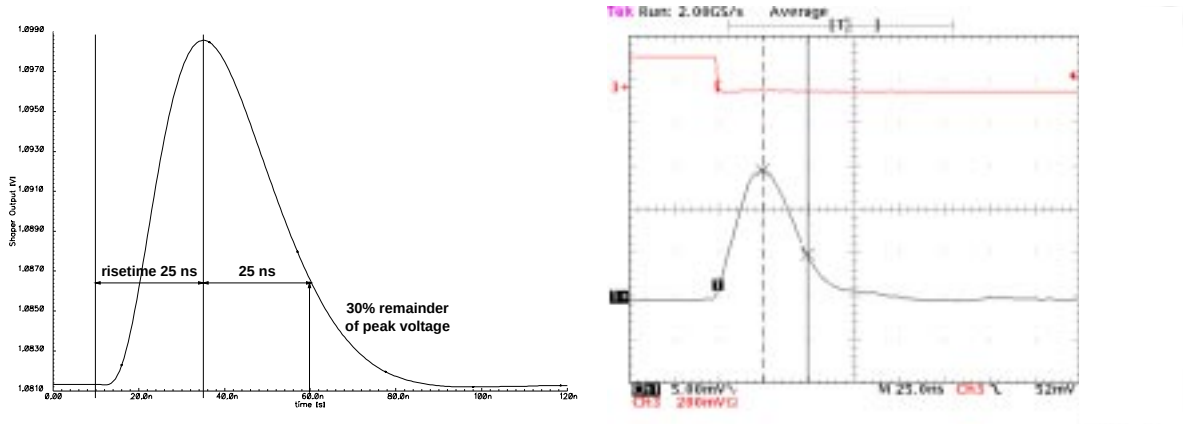


Figure 2: *Simulated (top) and measured (bottom) response to a transient signal of 11,000 electrons at a capacitive input load of 10 pF.*

an operation amplifier feedback but improves the small signal resistance by using a regular cascode at the output. The third one uses only a regular cascode and relies on the fact that the chosen technology has a very low threshold voltage shift and will not require compensation for radiation damage. The voltage DAC uses a R-2R-ladder configuration with a resolution of 10 bits and an output swing covering the full operating voltage. The current DAC consists of 1024 PMOS transistors acting as current sources.

Measurements performed on 20 of these test chips showed a performance in good agreement with the simulations and variations below 5%.

# 4 The *Beetle1.0* Readout Chip

The layout of the *Beetle1.0* [7] with the corresponding floor plan is depicted in fig.(3), showing all the functional blocks required according to the specifications for an LHCb front end chip.

The comparator circuit (fig.(4)) integrated into the *Beetle1.0* consists of an integrator, a threshold generator and a discriminator. The integrator extracts the DC-offset of the shaped pulse with a time constant of 5 $\mu$s. This offset varies from channel to channel and is added to the threshold voltage. The individual threshold levels are adjustable per channel with a resolution of 3 bits. The discriminator itself consists of 2 differential amplifiers. An additional polarity switch allows to use the comparator for positive and negative input signals.

The pipeline is an array of 129 $\times$ 186 analogue memory cells. The sampled voltage is stored on the 1 pF gate-capacitance of an NMOS transistor. For triggered events the stored charge is transferred to the multiplexer's hold capacitance via a resetable charge-sensitive amplifier. The use of a charge-sensitive amplifier provides optimum noise performance. The amplifier is resetable to limit the contribution of the serial noise. The subsequent hold stage ensures an identical integration time for all channels.

The multiplexer is a simple sample- and hold-stage with a source follower. It is structured into four (32:1)-multiplexers, which perform the readout of 128 channels within 900 ns by driving four ports at 40 MHz or two ports at 80 MHz. The former is used for analogue signals, the

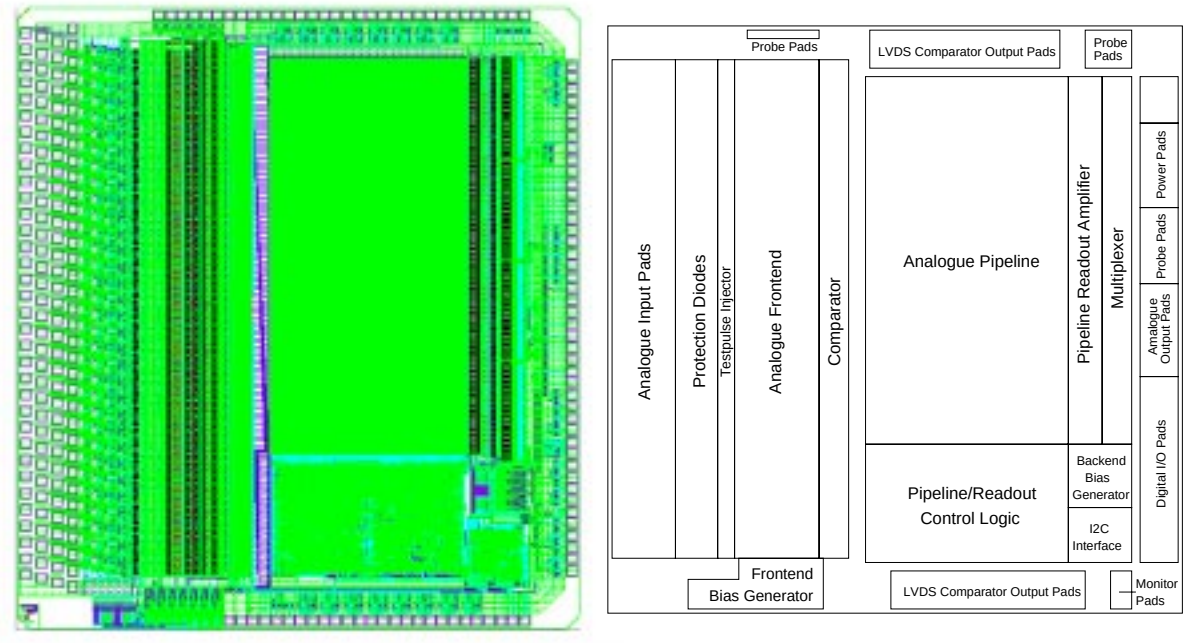


Figure 3: *Layout of the* Beetle1.0 *readout chip with its corresponding floor plan. The die size is* $(6.1 \times 5.5)\, mm^2$.

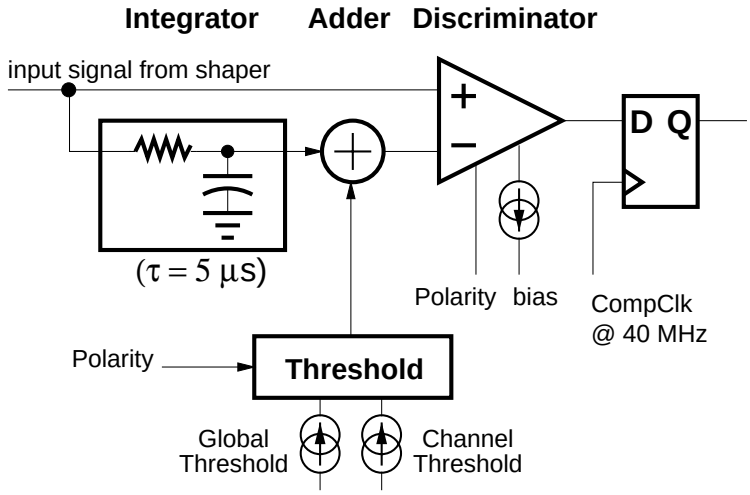


Figure 4: Schematic block diagram of the comparator of the *Beetle1.0*.

latter one in the binary mode of the chip. Alternatively also slow analogue readout on a single port is possible for applications with less demands on speed.

The logic controlling the pipeline and the readout of the chip has been functionally described in the *Verilog* hardware description language, synthesized with the *Synopsys* tool, and placed and routed with the *Silicon Ensemble* software, using 3 metal layers. It is essentially identical to that of the Helix128-3.1 chip [8, 9].

The chip's slow-control interface is a standard mode $I^2C$-slave device performing a transfer rate of 100 kbit/s. The $I^2C$-address of the chip is assigned in a self-programming procedure on power-up. Therefore the chips sharing one $I^2C$ bus line are in addition connected in a daisy chain. All 34 registers of a chips are readable via this interface.

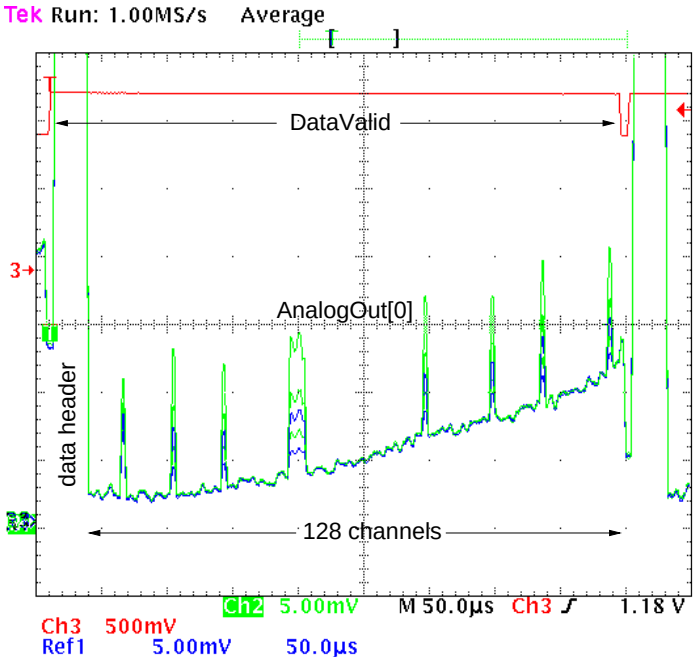


Figure 5: *Output of the complete analogue chain showing test pulse patterns applied to the inputs of the* Beetle1.0 *chip.*

The bias generators are divided into a frontend and a backend bias block (cf. fig.(3)). All digital to analogue converters (DACs) follow the design of the *BeetleBG1.0* testchip. From the three options the current source which provides on chip the reference current of 100 $\mu$A has been choosen.

Figure (5) shows the output signal of the complete analogue chain. All 128 channels are multiplexed on one port. The figure is an overlay of different events with input signals corresponding to 1, 2, 3, 4 and 7 MIPs applied to 7 single and a group of 4 adjacent channels of the chip. On the figure the different input levels are clearly visible on the group of 4 channels. The baseline shift is due to a voltage drop on the bias line of the pipeline readout amplifier, which will be corrected in future versions.

# 5 Summary and Outlook

A first version of the *Beetle* chip has been produced and tested. The individual components work according to specifications, the first prototype of the complete chip has been shown to be working, although the design performance could not be reached. The problems encountered with the *Beetle1.0* are understood and will be fixed in the next version of the chip, which is expected back for May 2001.

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